DATA HANDBOOK

Video and associated systems
Types TDA2658 to μA733C

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Philips Semiconductors

PHILIPS

Video and associated systems

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DEVICE DATA

VERTICAL DEFLECTION CIRCUIT

The TDA2658 is a monolithic integrated circuit for vertical deflection in small screen colour television receivers and monitors.

The circuit incorporates the following functions:

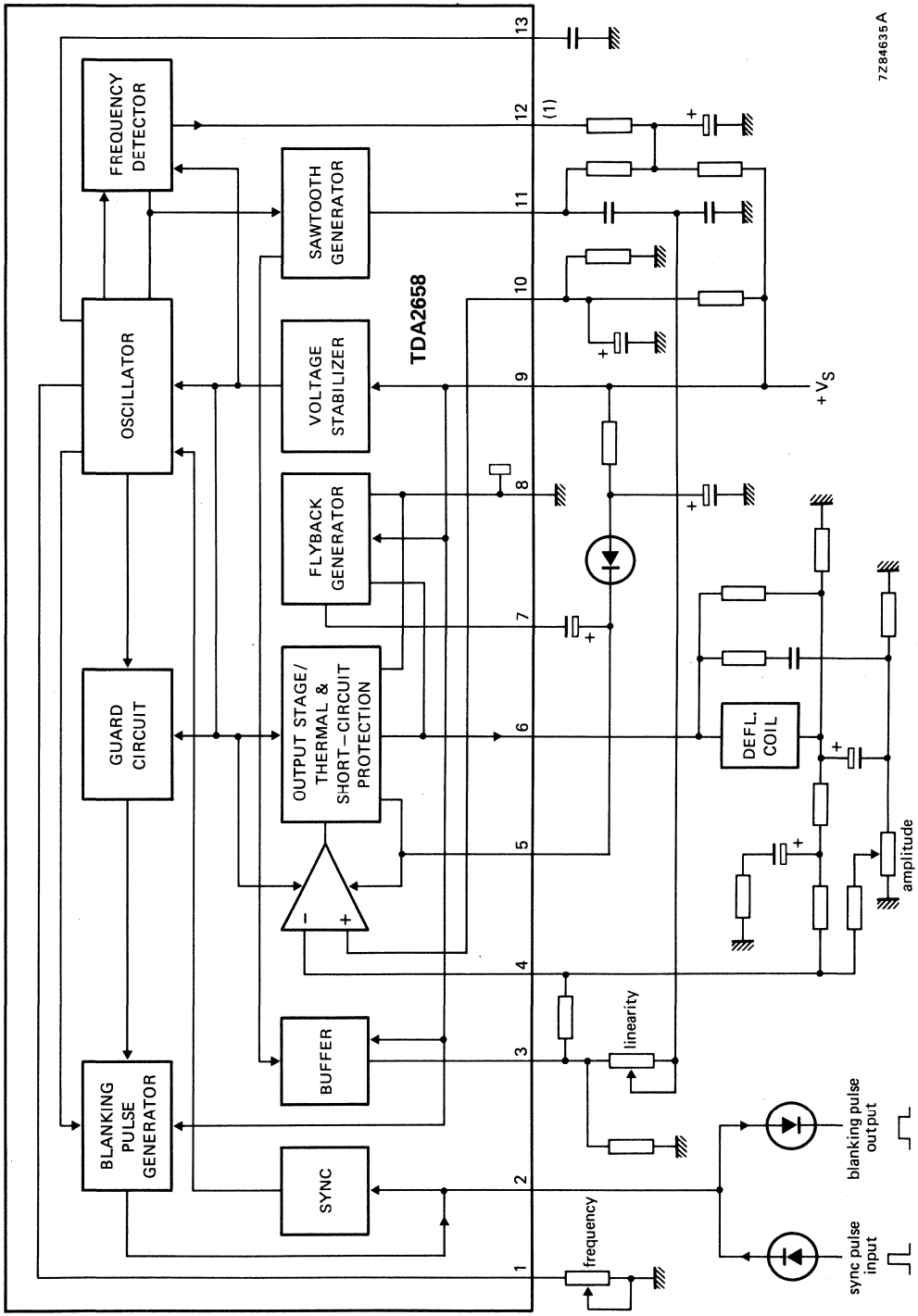
- Oscillator, switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26 V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	250 mA
Output current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1,6 A
Picture frequency	f		50 Hz/60 Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1 V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5 K/W

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141B).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	0,9 A
	$-I_7$	max.	1,1 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

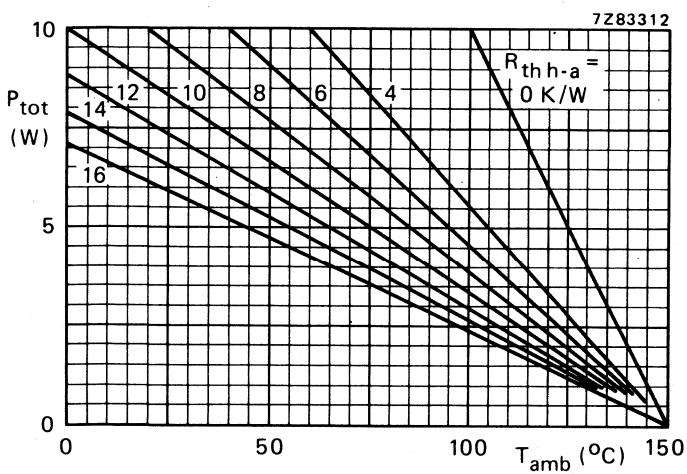


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heat-sink compound is used. $R_{th\ j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C; V_S = 26 V; unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 0,75 A	V_{6-8}	⩾	$V_{5-8} - 2,2$ V
		typ.	$V_{5-8} - 1,9$ V
at I_6 = 0,75 A	V_{6-8}	typ.	1,3 V
		⩽	1,6 V
Flyback generator output voltage at $-I_6$ = 0,75 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	0,9 A
Flyback generator peak current	$\pm I_7$	⩽	0,9 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1,5$ V
	V_{11-8}		0 to $V_S - 1,5$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency			
T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency			
V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage			
at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA (V_S = 26 V).

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

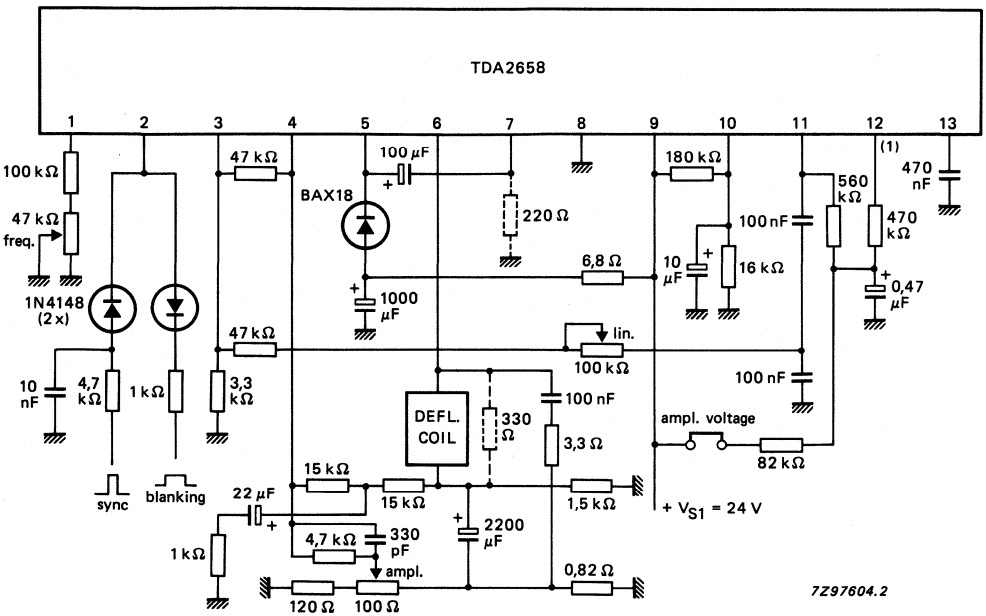
    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Fig. 3

System supply voltages	V_{S1}	typ.	24 V
System supply currents	I_{S1}	typ.	145 mA
Output voltage	V_{6-8}	typ.	14 V
Output voltage (peak value)	V_{6-8}	typ.	44 V
Deflection current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1 A
Flyback time	t_{fl}	typ.	1 ms
Total power dissipation per package	P_{tot}	typ. max.	1,7 W 2,2 W
Oscillator frequency unsynchronized	f	typ.	46,5 Hz



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit.

TV STEREO/DUAL SOUND IDENTIFICATION DECODER

The TDA2795 is a monolithic integrated circuit for stereo/dual sound in television receivers.

The circuit incorporates the following functions:

- Controlled pilot signal amplifier.
- Envelope demodulator.
- Two separate signal paths for processing the identification frequencies: operational amplifier for active filter, integral evaluation circuit with TTL compatible 'open collector' outputs.
- Stereo indicator driver.

QUICK REFERENCE DATA

Supply voltage	V_S	typ.	12 V
Supply current	I_S	typ.	8 mA
Nominal input voltage at f = 54,6875 kHz	V_i	typ.	10 mV
Input impedance	$\|Z_i\|$	$\geqslant$	500 kΩ
Operational amplifier			
open loop voltage gain at 200 Hz	G_o	$\geqslant$	78 dB
input resistance	R_i	$\geqslant$	1 MΩ
output resistance	R_o	$\leqslant$	3,5 kΩ
Supply voltage range	V_S		10,8 to 13,2 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

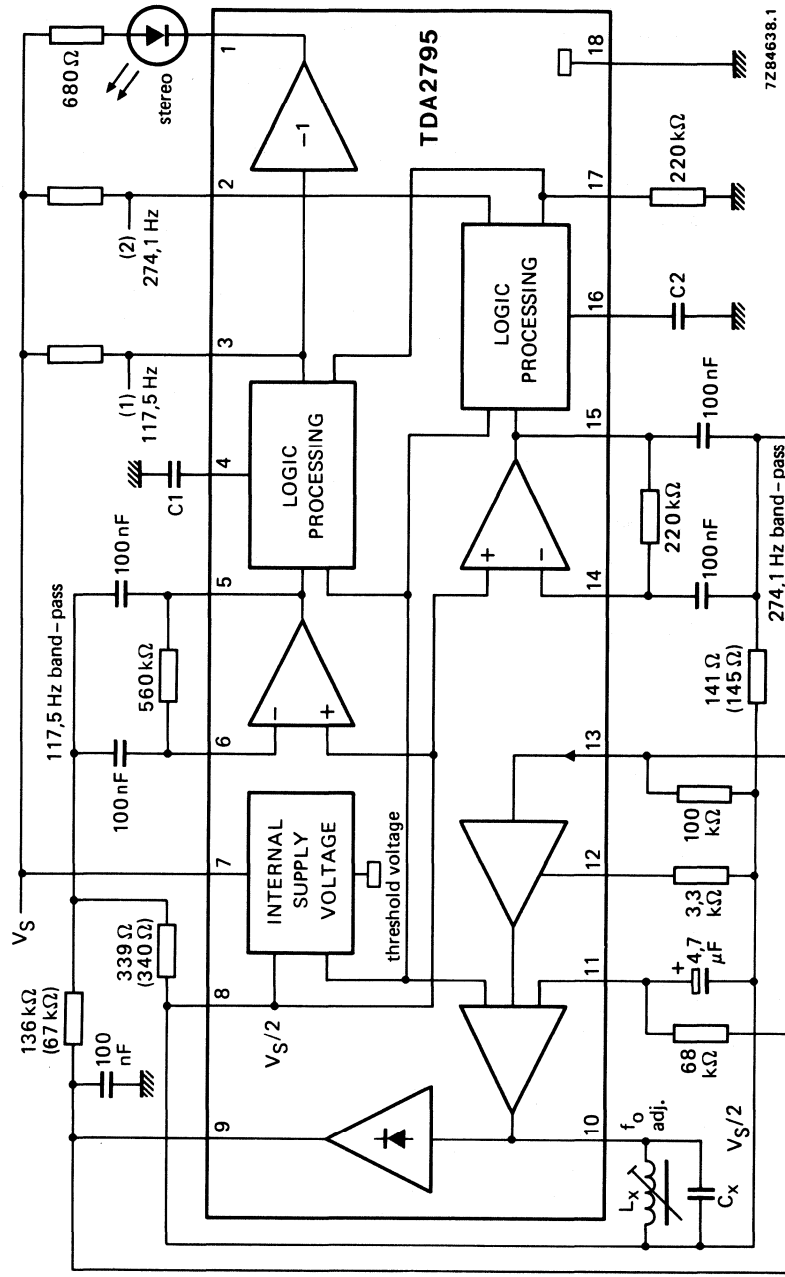


Fig. 1 Block diagram; C1 and C2 values 22 to 150 nF (dependent on switching time); values given in parenthesis are for G = 4 at 117,5/274,1 Hz; C_x = 3,3 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_{7-18} = V_S$	max.	15	V
Signal input (pin 13)	V_{13-18}	max.	V_S	V
	$-V_{13-18}$	max.	0,5	V
Switch outputs (pins 1, 2 and 3)	V_{1-18}	max.	18	V
	I_1	max.	50	mA
	$V_{2;3-18}$	max.	15	V
	$I_{2;3}$	max.	5	mA
	$-V_{1;2;3-18}$	max.	0,5	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to +125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_S = 12 V; T_{amb} = 25 °C, unless otherwise specified; measured in Fig. 1, at V_i = 10 mV; f = 54,6875 kHz amplitude modulated with f_{m1} = 117,5 Hz or f_{m2} = 274,1 Hz; $m_1 = m_2$ = 50%.

Supply voltage range	V_S		10,8 to 13,2	V
Supply current	I_S	typ.	8	mA
		⩽	12	mA

Pilot signal amplifier and envelope demodulator

Maximum input voltage (peak-to-peak value)	$V_{i(p-p)}$	typ.	2	V
Input impedance	$\|Z_{13-18}\|$	⩾	500	kΩ
Voltage gain (V_{9-18}/V_{13-18}) at V_i = 1 mV	G_{v9-13}	typ.	42	dB
Start of control at V_i	see Fig. 3			
Control range	ΔG_v	⩾	40	dB
Controlled output voltage (r.m.s. value) (pin 9)	$V_{o(rms)}$	typ.	550	mV

Operational amplifiers

Input bias current (pins 6 and 14)	$\pm I_6; \pm I_{14}$	⩽	70	nA
Open loop voltage gain at f = 200 Hz	G_o	⩾	78	dB
Available output current (pins 5 and 15)	$\pm I_5; \pm I_{15}$	⩾	1,5	mA
Output resistance (pins 5 and 15)	R_o	typ.	2	kΩ
		⩽	3,5	kΩ
Allowable load capacitance	C_L	⩽	30	pF
Output offset voltage at R_{5-6} = 560 kΩ	$\pm V_{o5-8}$	⩽	70	mV

CHARACTERISTICS (continued)

Evaluation circuitry			
Switch-on threshold voltage (pins 5 and 15)	$V_5; V_{15}$	typ.	1,0 V
Switch hysteresis	$\frac{V_{5on}}{V_{5off}} = \frac{V_{15on}}{V_{15off}}$	typ.	3,8 ± 0,5 dB
Switch outputs (pins 2 and 3)			
allowable output current	$I_3; I_2$	$\leqslant$	2 mA
saturation voltage at $I_3 = I_2 = 1{,}5$ mA	$V_{3;2\text{-}18sat}$	$\leqslant$	0,35 V
leakage voltage at $I_3 = I_2 \leqslant 5\ \mu A$	$V_{3;2\text{-}18}$	$\leqslant$	15 V
Indicator driver (pin 1)			
allowable output current	I_1	$\leqslant$	40 mA
saturation voltage at $I_1 = 20$ mA	$V_{1\text{-}18sat}$	$\leqslant$	0,8 V
leakage voltage at $I_1 < 10\ \mu A$	$V_{1\text{-}18}$	$\leqslant$	18 V
Internal reference voltage			
Reference voltage (pin 8)	$V_{8\text{-}18}$	typ.	6 V
Available output current (pin 8)	$-I_8$	$\geqslant$	2 mA
	$+I_8$	$\geqslant$	0,6 mA
Reference current source			
Reference voltage (pin 17)	$V_{17\text{-}18}$	typ.	5,3 V
Internal bias resistor	R_{i17}	typ.	5 kΩ
Allowable load resistor (pin 17)	R_L		180 to 270 kΩ

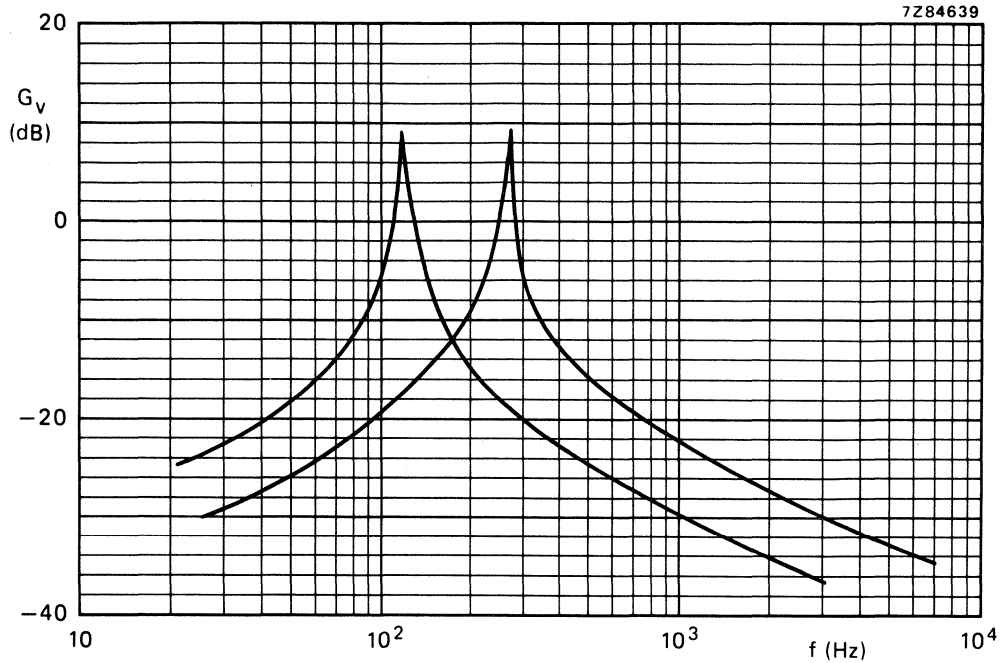


Fig. 2 Band-pass curves for 117,5 Hz and 274,1 Hz.

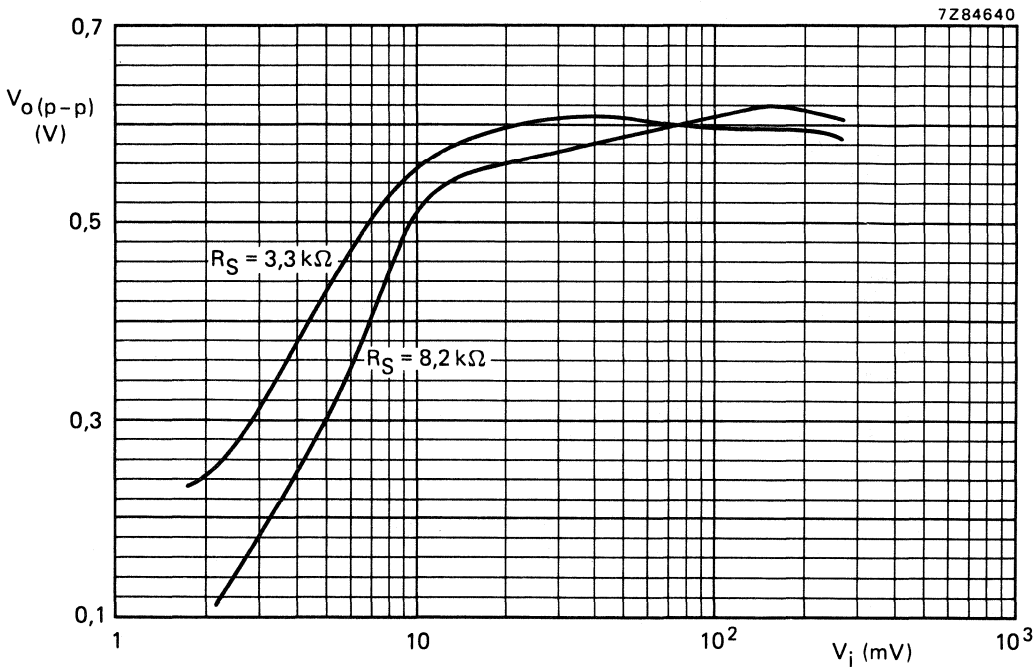


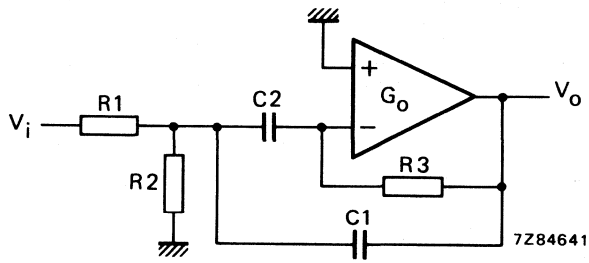
Fig. 3 Controlled output voltage as a function of the input signal (Q_o = 80); pilot frequency f_o = 54,6875 kHz; R_S is source resistance.

GENERAL FILTER CALCULATIONS

1. Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p\frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}, \text{ in which: } p = j\omega; G_v = \frac{V_o}{V_i}$$



2. Resonance frequency

$$\omega_r = \frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$$

3. Gain at $\omega = \omega_r$

$$-G_{vr} = \frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$$

4. Quality

$$Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$$

5. Recommended components

C1 and C2: 5% MKC (metallized polycarbonate film capacitor)
R1, R2 and R3: 2% MR (metal film resistor)

or:

C1 and C2: 5% MKT (metallized polyester film capacitor)
R1, R2 and R3: 2% CR (carbon film resistor)

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

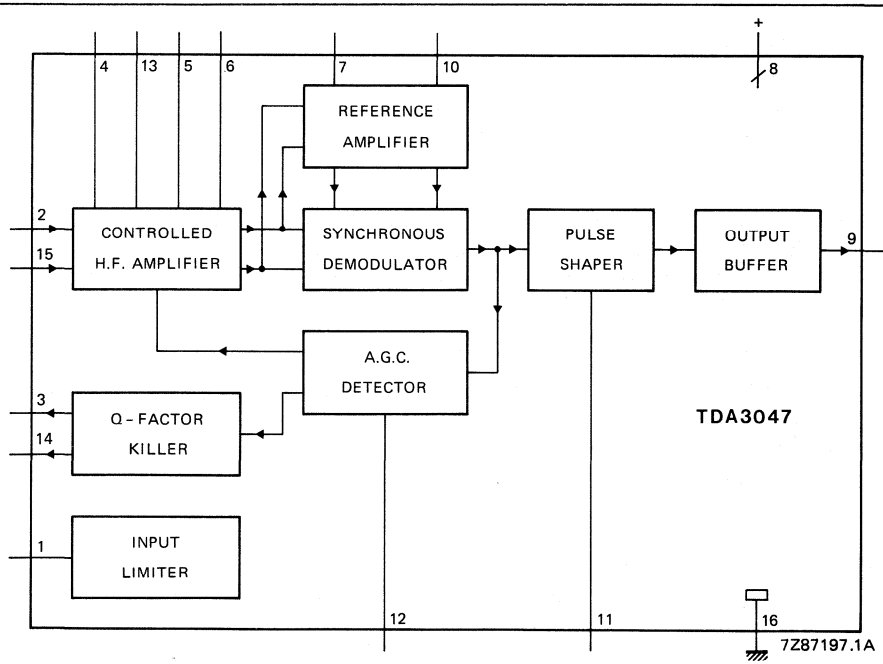


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at V_{9-16} = 4,5 V	$-I_9$	75	120	–	μA
at V_{9-16} = 3,0 V	$-I_9$	75	130	–	μA
at V_{9-16} = 1,0 V	$-I_9$	75	140	–	μA
Output current; output voltage *low* at V_{9-16} = 0,5 V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

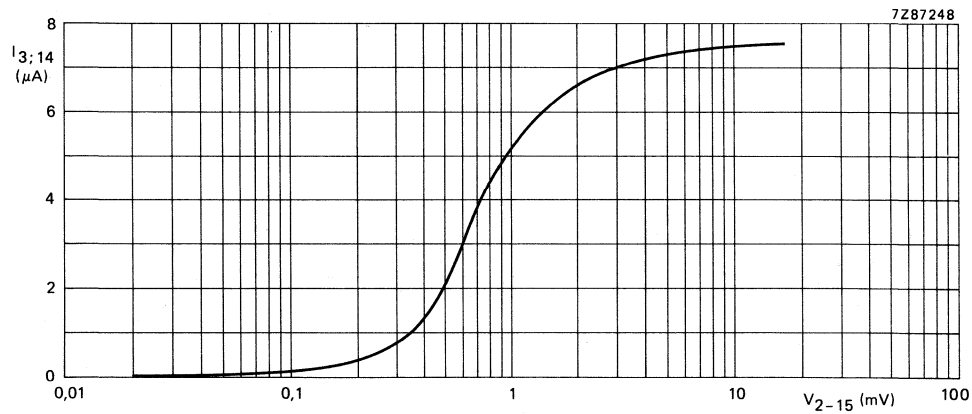
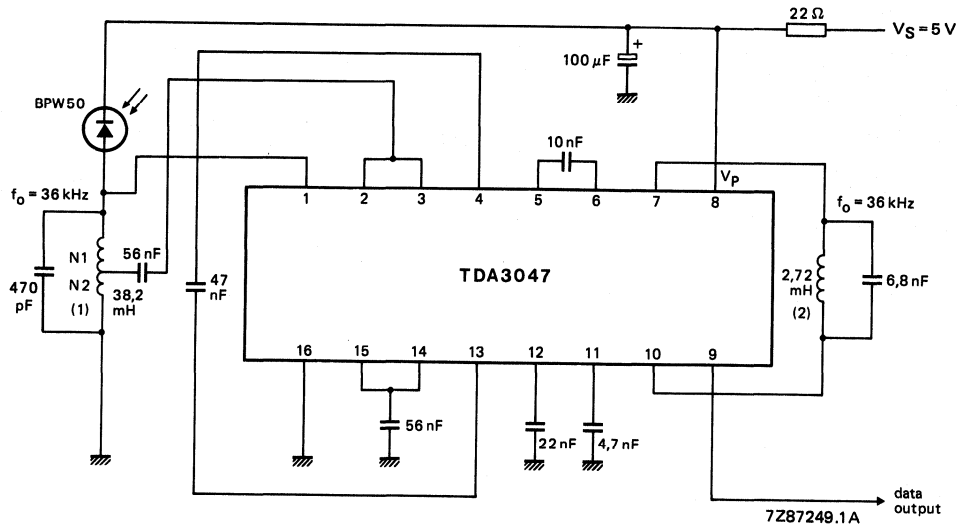


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

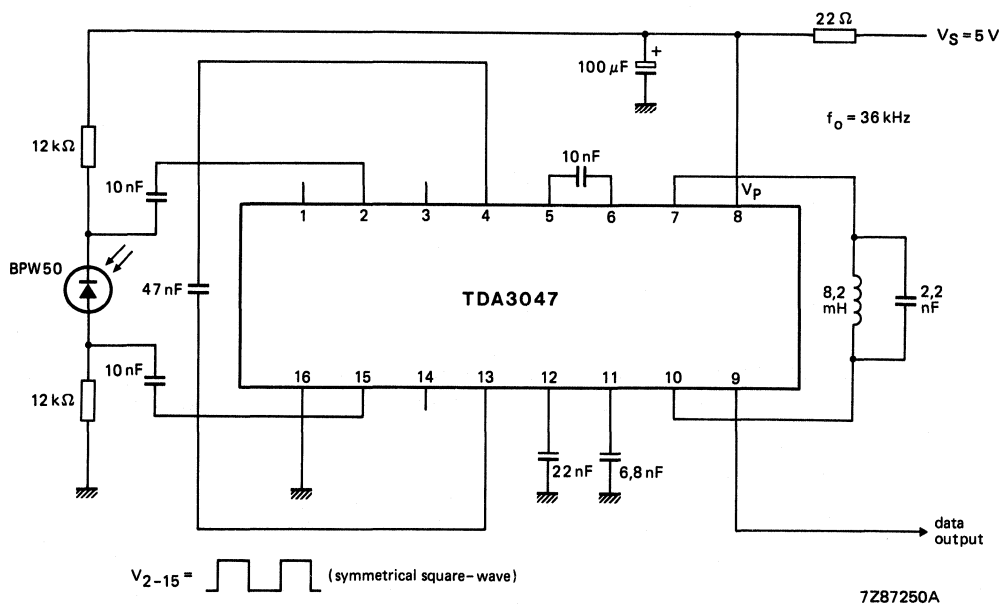


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$	0,03 to	200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

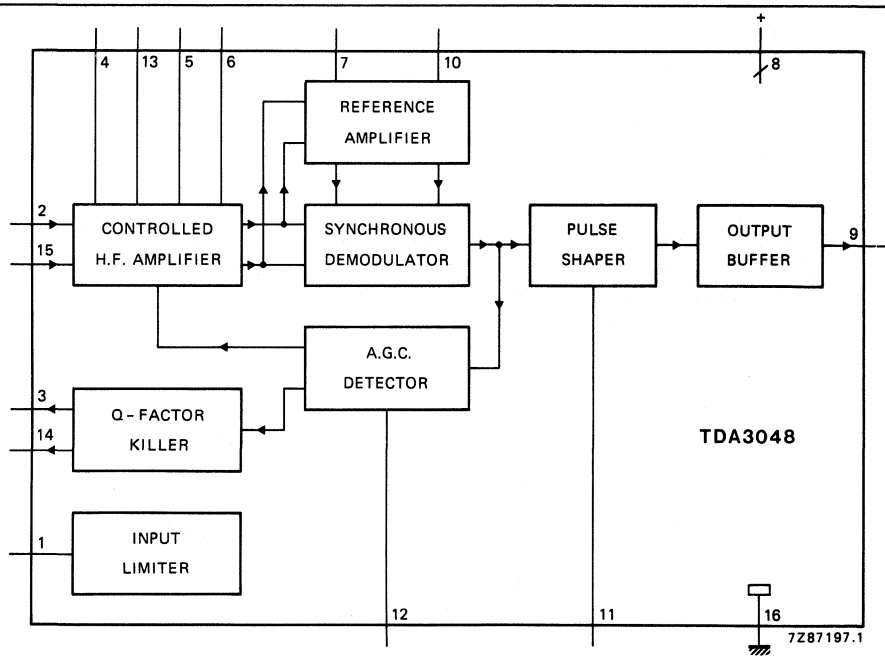


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 μA with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9$ = 75 μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at I_9 = 75 μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8}$ = 4,5 V	I_9	75	120	–	μA
$-V_{9-8}$ = 3,0 V	I_9	75	130	–	μA
$-V_{9-8}$ = 1,0 V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8}$ = 0,5 V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; I_9 = 75 μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

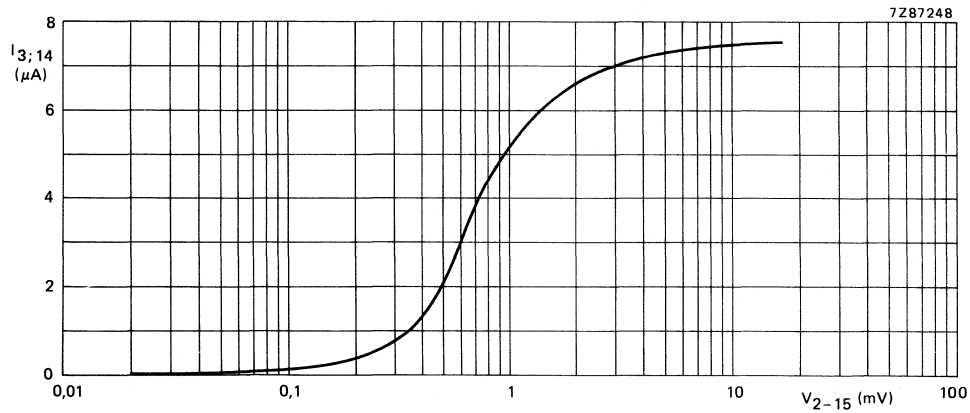
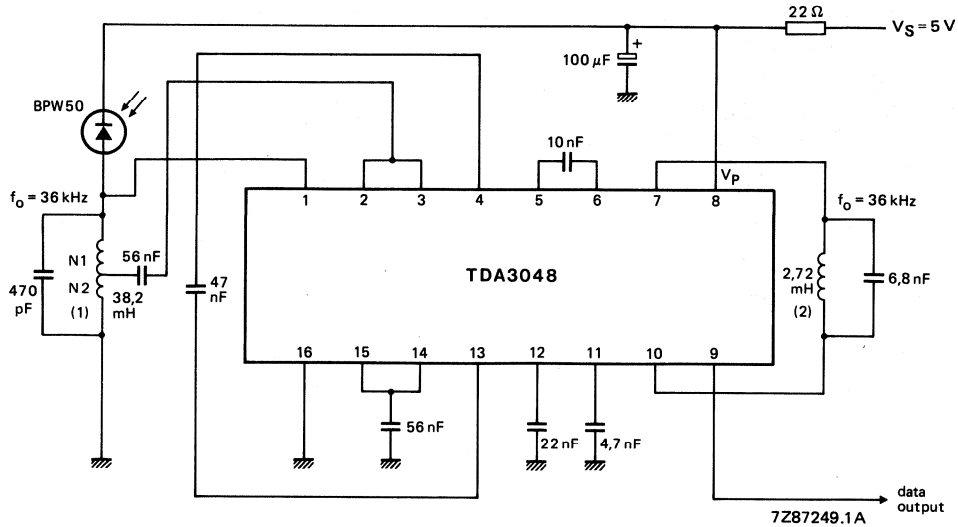


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

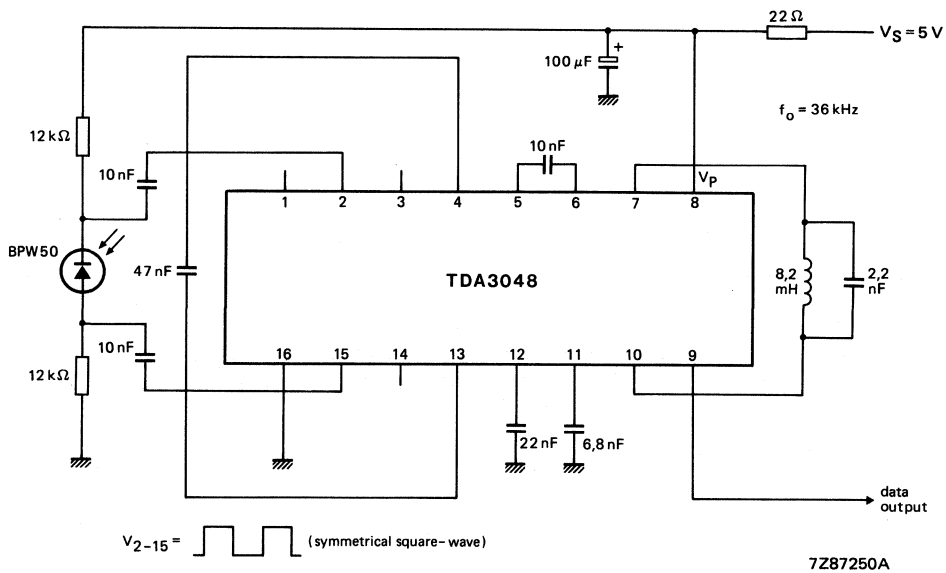


Fig. 4 Wide-band receiver with TDA3048.

For better sensitivity both 12 kΩ resistors may have a higher value.

VIDEO CONTROL COMBINATION CIRCUIT

GENERAL DESCRIPTION

The TDA3504 is an integrated circuit which performs video control functions in a PAL/SECAM decoder for negative colour difference signals −(R-Y) and −(B-Y).

The required input signals are: luminance and colour difference and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 2)		$V_P = V_{2\text{-}18}$	–	12	–	V
Supply current		$I_P = I_2$	–	95	–	mA
CVBS input signal (peak-to-peak value)		$V_{11\text{-}18(p\text{-}p)}$	–	0.45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y)		$V_{15\text{-}18(p\text{-}p)}$	–	1.33	–	V
−(R-Y)		$V_{14\text{-}18(p\text{-}p)}$	–	1.05	–	V
Inserted RGB signals (black-to-white value)		$V_{10,9,8\text{-}18}$	–	1.0	–	V
Three-level sandcastle pulse		$V_{6\text{-}18}$	–	2.5	–	V
			–	4.5	–	V
			–	8.0	–	V
Control voltage ranges						
brightness		$V_{17\text{-}18}$	1.0	–	3.0	V
contrast		$V_{16\text{-}18}$	2.0	–	4.2	V
saturation		$V_{12\text{-}18}$	2.0	–	4.2	V

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

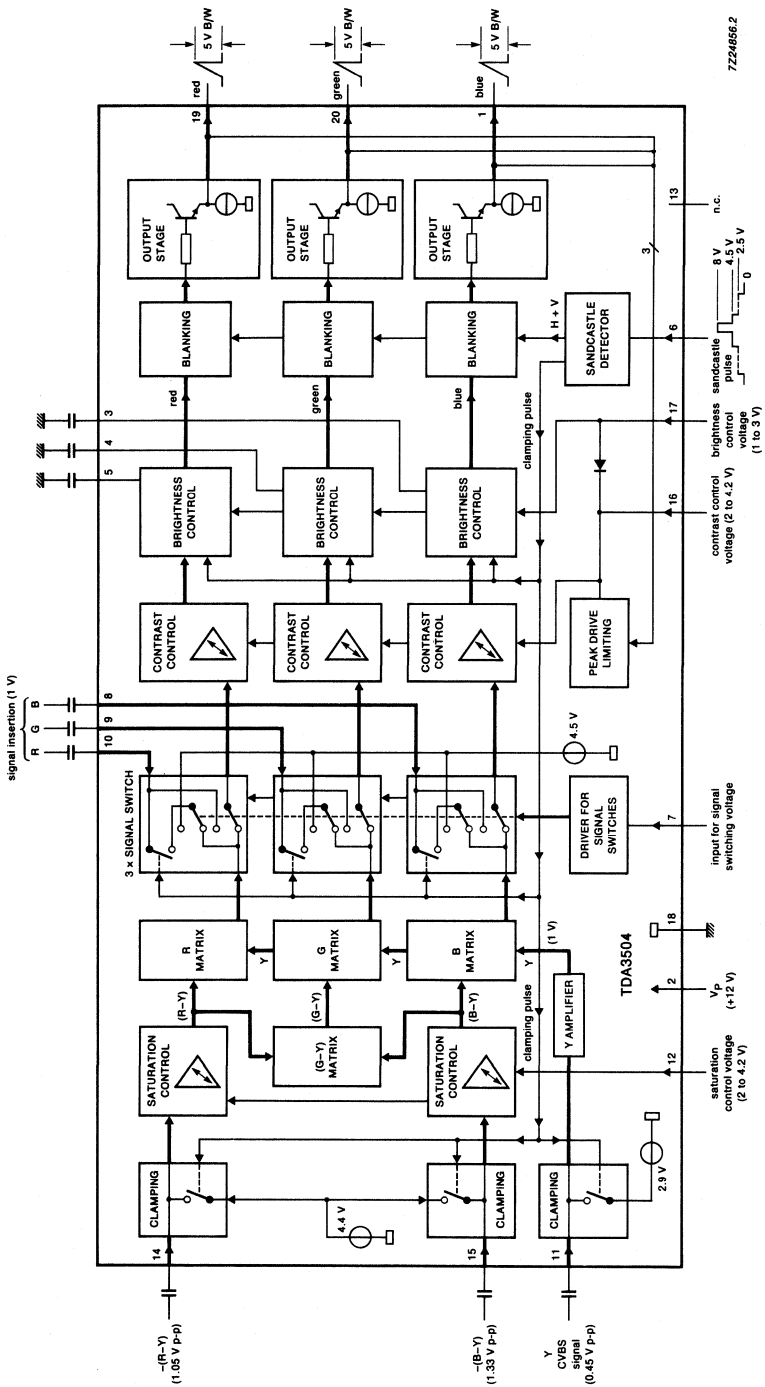


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

pin	description
1	blue output
2	positive supply voltage (+ 12 V)
3	blue storage for brightness
4	green storage for brightness
5	red storage for brightness
6	sandcastle pulse input
7	fast switch for RGB inputs
8	blue input (external signal)
9	green input (external signal)
10	red input (external signal)
11	luminance input
12	saturation control input
13	not connected
14	colour difference input −(R-Y)
15	colour difference input −(B-Y)
16	contrast control input
17	brightness control input
18	ground (0 V)
19	red output
20	green output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 2)	$V_P = V_{2-18}$	0	13.2	V
Voltage ranges				
at pin 6	V_{6-18}	0	V_P	V
at pin 7	V_{7-18}	−0.5	3.0	V
at pins 12, 16 and 17	$V_{12, 16, 17-18}$	0	$0.5V_P$	V
at pins 1, 3, 4, 5, 8, 9, 10, 11, 14, 15, 19 and 20	no external DC voltage			
Currents				
at pins 1, 19 and 20 (average)	$-I_{1, 19, 20}$	–	3	mA
at pins 1, 19 and 20 (peak)	$-I_{1, 19, 20}$	–	10	mA
at pin 16 (average)	I_{16}	–	10	mA
at pin 17	I_{17}	–	5	mA
Total power dissipation	P_{tot}	–	1.7	W
Storage temperature range	T_{stg}	−25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{2\text{-}18} = 12.0$ V; $V_{8,\ 9,\ 10\text{-}18(p\text{-}p)} = 1.0$ V; $V_{11\text{-}18(p\text{-}p)} = 0.45$ V; $V_{14\text{-}18(p\text{-}p)} = 1.05$ V; $V_{15\text{-}18(p\text{-}p)} = 1.33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig.2; nominal settings of brightness, contrast and saturation; all voltages are referred to pin 18; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 2)						
Supply voltage		$V_P = V_2$	10.8	12.0	13.2	V
Supply current		$I_P = I_2$	–	95	125*	mA
Colour difference inputs (pins 14 and 15)						
–(R-Y) input signal (pin 14) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{14(p\text{-}p)}$	–	1.05	1.48	V
–(B-Y) input signal (pin 15) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{15(p\text{-}p)}$	–	1.33	1.88	V
Input current during scanning		$I_{14,\ 15}$	–	–	0.2	μA
Input resistance		$R_{14,\ 15\text{-}18}$	1.0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{14,\ 15}$	3.8	4.4	4.8	V
Saturation control (pin 12)						
Control voltage for maximum saturation	note 1	V_{12}	4.0	4.2	4.4	V
Control voltage for nominal saturation	note 1; 6 dB below max.	V_{12}	2.9	3.1	3.3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{12}	1.9	2.1	2.3	V
Minimum saturation	$V_{12} = 1.8$ V	d	46	50	–	dB
Input current		I_{12}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G\text{-}Y)} = -0.51\ V_{(R\text{-}Y)} - 0.19\ V_{(B\text{-}Y)}$						
Luminance input (pin 11)						
CVBS input signal (peak-to-peak value)		$V_{11(p\text{-}p)}$	–	450	630	mV
Input resistance		$R_{11\text{-}18}$	1	–	–	MΩ

* < 110 mA after warm-up.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Input current during scanning		I_{11}	–	–	0.4	μA
Linearity	nominal settings	m	0.85	–	–	
Internal DC voltage due to clamping	note 1	V_{11}	2.5	2.9	3.3	V
RGB channels						
Signal switching input (pin 7)						
Normal state; no insertion		V_7	0	–	0.4	V
Level for insertion-on		V_7	0.9	–	3.0	V
Input capacitance		$C_{7\text{-}18}$	–	–	10	pF
Input current	V_7 = 0 to 3 V	I_7	−100	–	+ 450	μA
Signal insertion R: pin 10 G: pin 9 B: pin 8						
External RGB input signals (black-to-white value)		$V_{8, 9, 10}$	–	1.0	1.4	V
Input current during scanning		$I_{8, 9, 10}$	–	–	0.4	μA
Internal DC voltage due to clamping	notes 1 and 2	$V_{8, 9, 10}$	4.0	4.5	5.0	V
Contrast control (pin 16)	note 1					
Control voltage for maximum contrast		V_{16}	4.0	4.2	4.4	V
Control voltage for nominal contrast	3 dB below max.	V_{16}	3.4	3.6	3.8	V
Control voltage for −10 dB below max.		V_{16}	2.6	2.8	3.0	V
Minimum contrast referred to max.	V_{16} = 2 V	d	18	21	29	dB
Difference between RGB channels	contrast −10 dB below max.		–	–	0.6	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Peak drive limiting						
Threshold voltage	note 1	V_{th}	8.7	9.0	9.3	V
Input current at contrast control input	$V_{1, 19, 20} = \geqslant V_{th}$	I_{16}	10	20	30	mA
Brightness control (pin 17)	note 1					
Control voltage range		V_{17}	1	–	3	V
Control voltage for nominal brightness		V_{17}	–	2.0	–	V
Input current		$-I_{17}$	–	–	10	μA
Shift of black level in the control range related to the luminance signal (black/white)	$\Delta V_{17} = 1$ V		–	± 40	–	%
Tracking			95	–	–	%
RGB outputs (emitter follower) (pins 19, 20 and 1)						
Output voltage; black-to-white positive		$V_{19, 20, 1}$	4.0	5.0	6.5	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{19, 20, 1}$	–	–	10	mV
Internal current source		$I_{19, 20, 1}$	2.0	3.0	–	mA
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 11)		$G_{19, 20, 1\text{-}11}$	22	24	26	dB
Frequency response of luminance path	0 to 5 MHz	$d_{19, 20, 1\text{-}11}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 14 and 15)		$G_{1\text{-}15}$ $G_{19\text{-}14}$	11	14	17	dB

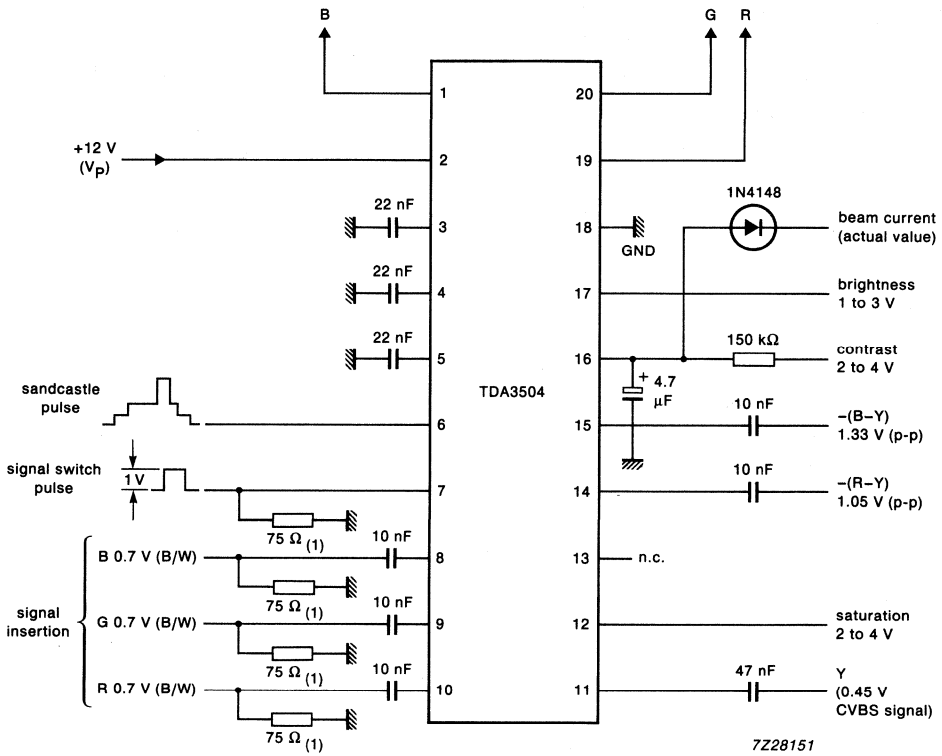
DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response of colour difference paths	0 to 2 MHz	$d_{1\text{-}15}$ $d_{19\text{-}14}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{19\text{-}10}$ $G_{20\text{-}9}$ $G_{1\text{-}8}$	12	14	16	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{19\text{-}10}$ $d_{20\text{-}9}$ $d_{1\text{-}8}$	–	–	3	dB
Difference in transit times between R, G and B channels		$\Delta t_{19,\,20,\,1}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	−25	–	+ 25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{19,\,20,\,1}$	–	–	10	%
Sandcastle pulse detector (pin 6)	note 3					
The following amplitudes are required for separating the various pulses:						
horizontal and vertical blanking pulses	note 4	V_6	2.1	2.5	2.9	V
horizontal pulses		V_6	4.1	4.5	5.0	V
clamping pulses	note 5	V_6	7.6	8.0	12.0	V
no keying		V_6	–	–	1.0	V
Input current		$-I_6$	–	–	110	μA
Delay of leading edge of clamping pulse		t_d	–	0.5	–	μs

Notes to the characteristics

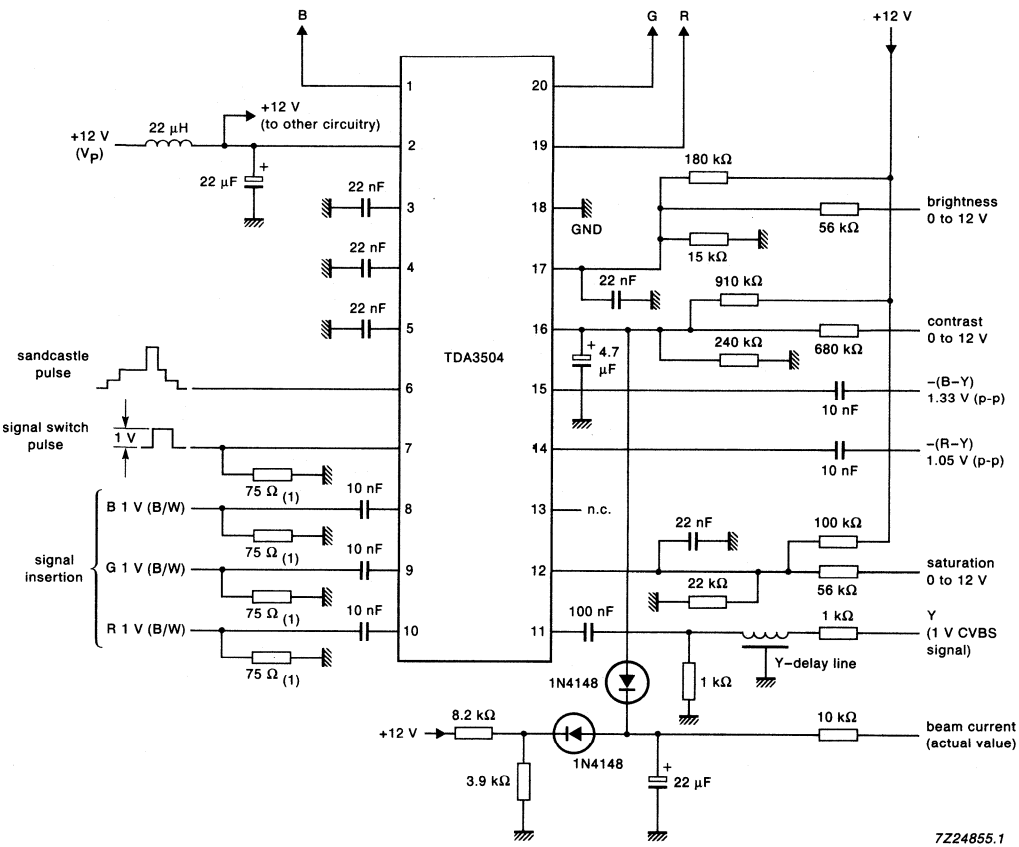
1. Values are proportional to the supply voltage.
2. When $V_{7\text{-}18} < 0.4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{7\text{-}18} > 0.9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
4. Blanked to ultra-black (−25%).
5. Pulse duration $\geqslant 3.5$ μs.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.

Fig.2(a) Basic application circuit diagram.



(1) When applied via a 75 Ω line.

Fig.2(b) Typical application circuit diagram.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3505 and TDA3506 are monolithic integrated circuits which perform video control functions in a PAL/SECAM decoder. The TDA3505 is for negative colour difference signals −(R-Y), −(B-Y) and the TDA3506 is for positive colour difference signals +(R-Y), +(B-Y).

The required input signals are: luminance and colour difference (negative or positive) and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuits provide automatic cut-off control of the picture tube.

Features

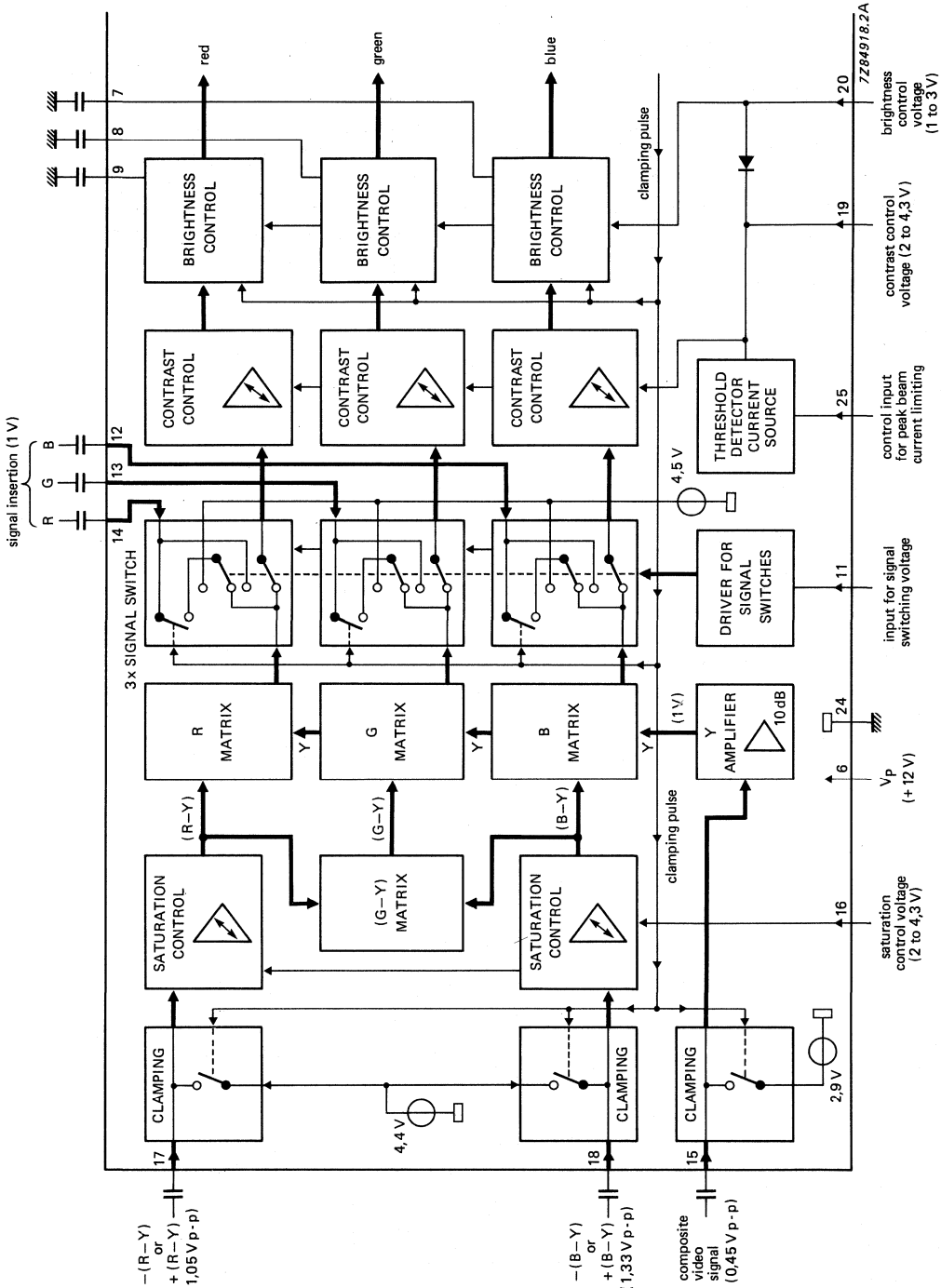
- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	95	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y) or +(B-Y) respectively		$V_{18-24(p-p)}$	–	1,33	–	V
−(R-Y) or +(R-Y) respectively		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12, 13, 14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).



Note Colour difference inputs are negative for TDA3505 or positive for TDA3506.

Fig. 1a Part of block diagram; continued in Fig. 1b.

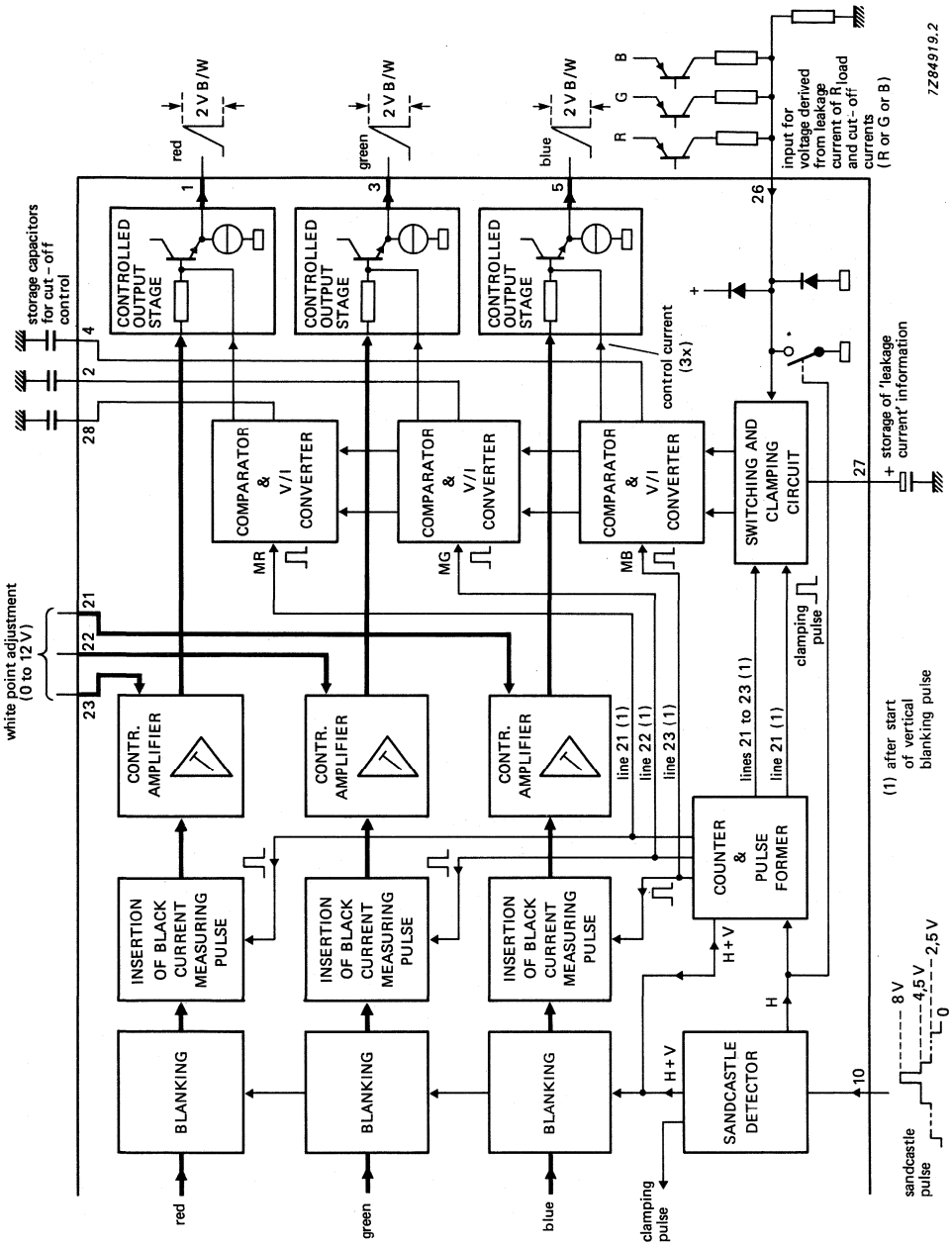


Fig. 1b Part of block diagram; continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	colour difference input −(R-Y) or +(R-Y) respectively
18	colour difference input −(B-Y) or +(B-Y) respectively
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	−	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16, 19, 20-24}$	0	0,5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1, 3, 5}$	−	3	mA
at pin 19	I_{19}	−	10	mA
at pin 20	I_{20}	−	5	mA
at pin 25	$-I_{25}$	−	5	mA
Total power dissipation	P_{tot}	−	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12, 13, 14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	95	125*	mA
Colour difference inputs (pins 17, 18)						
(R-Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
(B-Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17, 18}$	–	–	1,0	μA
Input resistance		$R_{17, 18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17, 18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ

* < 110 mA after warm-up.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input capacitance		$C_{15\text{-}24}$	–	–	5	pF
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12, 13, 14}$	–	1,0	1,4	V
Input current during scanning		$I_{12, 13, 14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12, 13, 14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21, 22, 23}$ = 5,5 V		G_v	–	100	–	%
$V_{21, 22, 23}$ = 0 V		G_v	–35	–40	–	%
$V_{21, 22, 23}$ = 12 V		G_v	+35	+40	–	%
Input resistance		$R_{21,22,23-24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1, 3, 5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1, 3, 5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1, 3, 5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1, 3, 5}$	4,0	4,6	–	V
Internal current source		$I_{1, 3, 5}$	2,0	3,0	–	mA

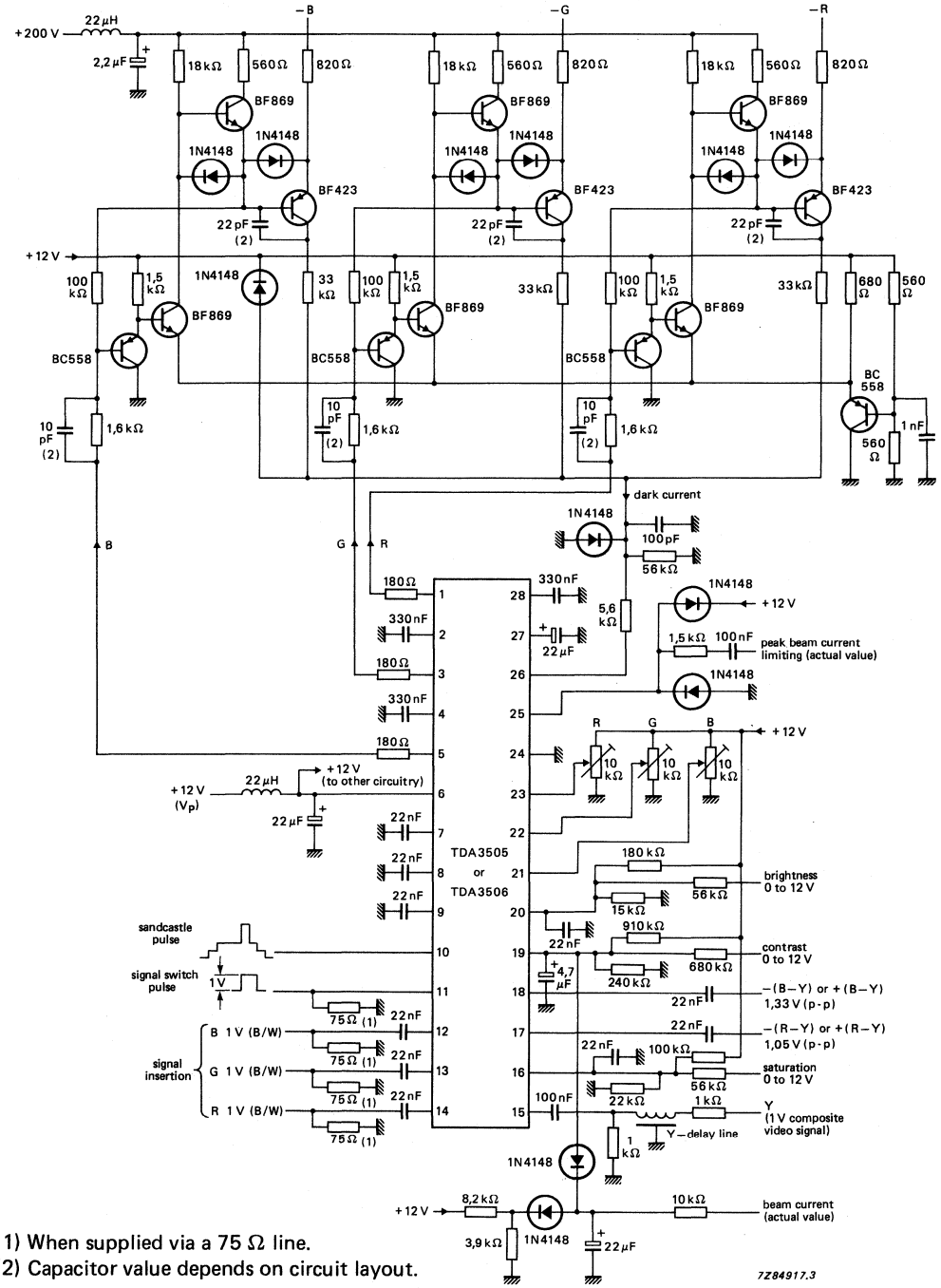
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24} > 0{,}9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with three internal thresholds (proportional to Vp) and the given levels separate the various pulses.
8. Blanked to ultra-black (–25%).
9. Pulse duration $\geqslant 3{,}5$ μs.



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using TDA3505 or TDA3506; colour difference inputs are negative for TDA3505 or positive for TDA3506.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3507 is a monolithic integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference −(R−Y) and −(B−Y), and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

The TDA3507 is the same as the TDA3505 but with RGB channel bandwidths of (typical) 16 MHz and an automatic cut-off cycle that ends in line 15.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G−Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1,33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

DEVELOPMENT DATA

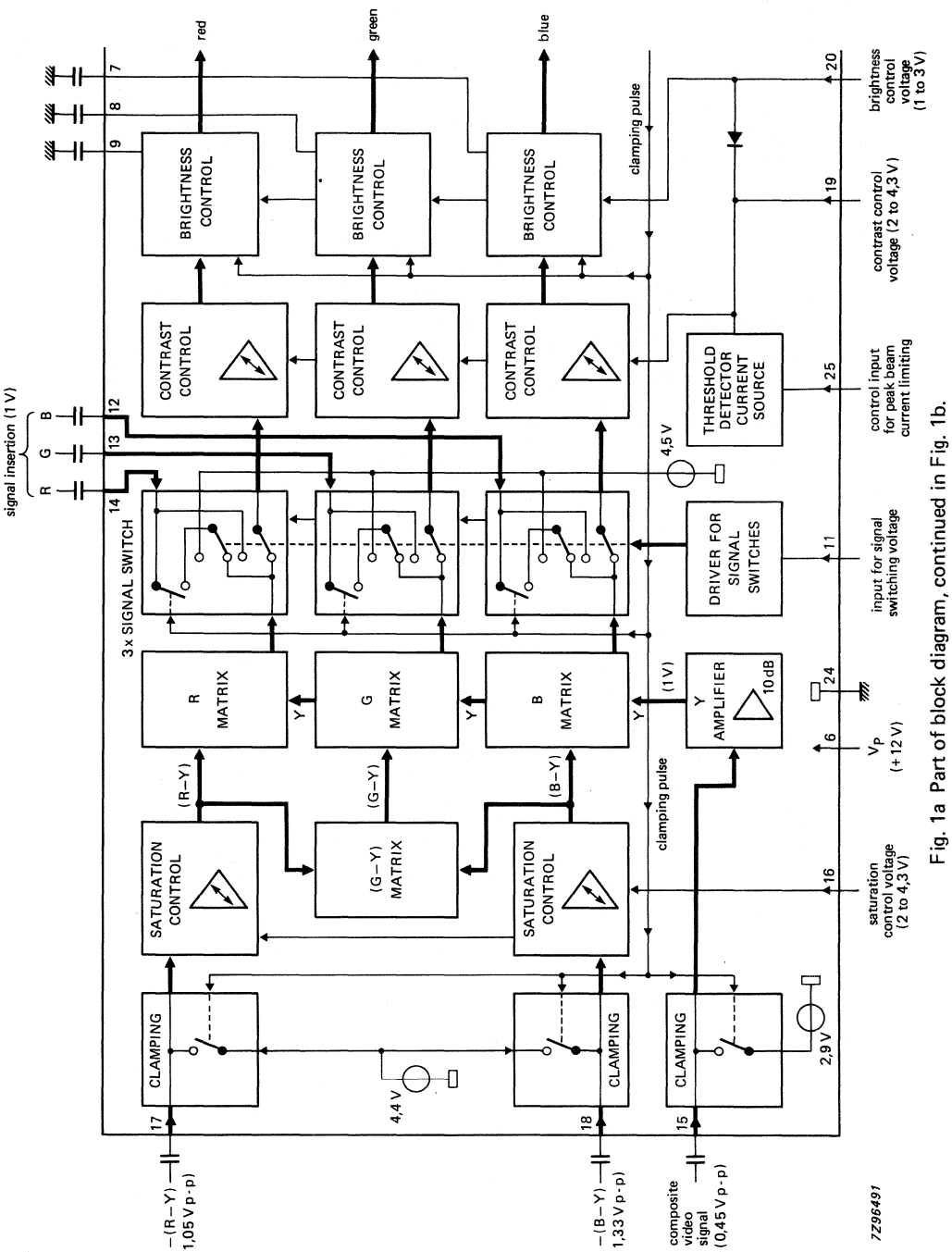


Fig. 1a Part of block diagram, continued in Fig. 1b.

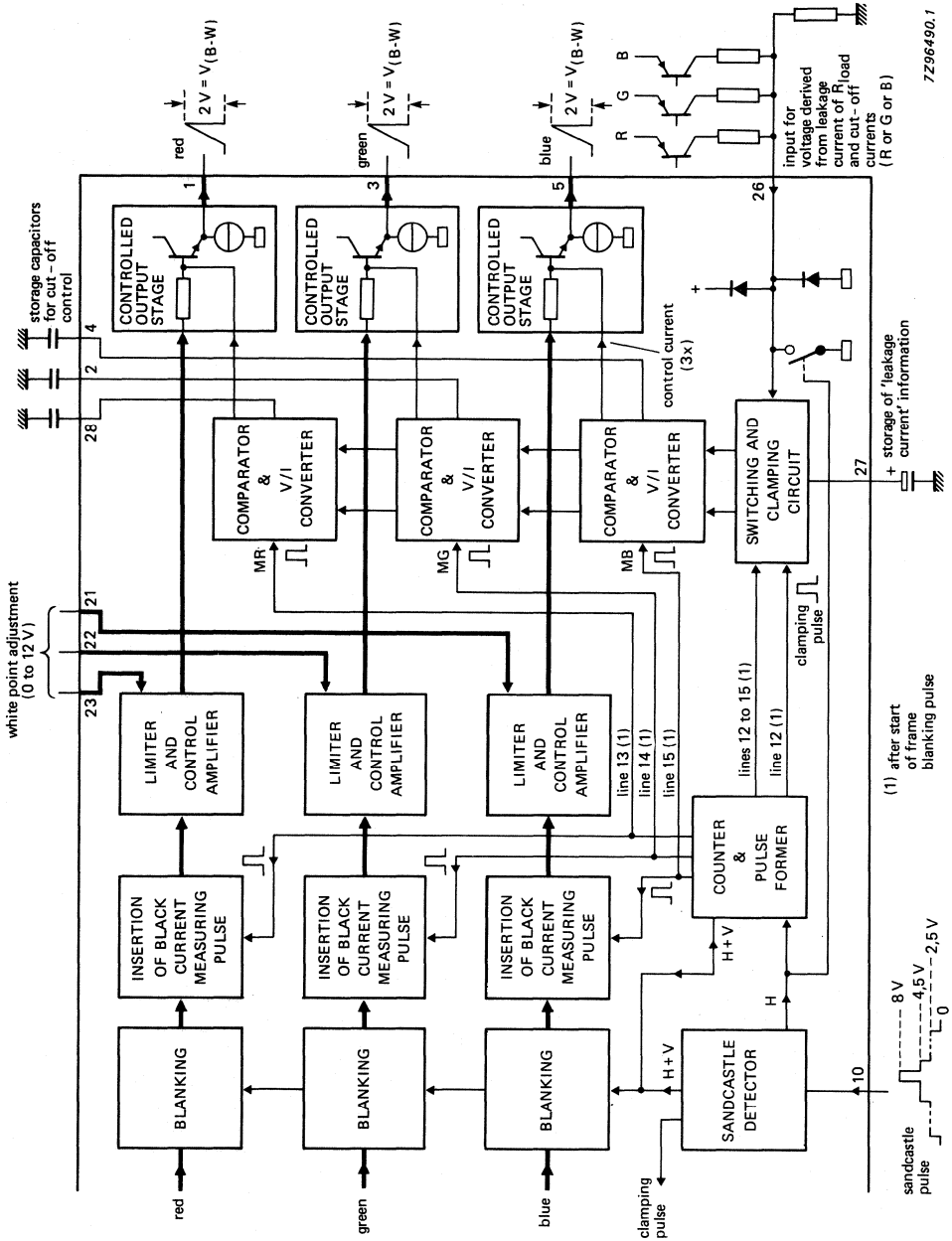


Fig. 1b Part of block diagram, continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	−	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	0,5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	−	3	mA
at pin 19	I_{19}	−	10	mA
at pin 20	I_{20}	−	5	mA
at pin 25	$-I_{25}$	−	5	mA
Total power dissipation	P_{tot}	−	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12,13,14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17,18}$	–	–	1,0	μA
Input resistance		$R_{17,18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* < 115 mA after warm-up

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1,0	1,4	V
Input current during scanning		$I_{12,13,14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5,5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4,0	4,6	–	V
Internal current source		$I_{1,3,5}$	2,0	3,0	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1,4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 16 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	3	–	dB
Frequency response of inserted signal paths	0 to 13 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain data (continued)						
Delay time between signal switching and signal insertion		t_d	−25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

   When $V_{11\text{-}24} > 0{,}9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:

   line 12: measurement of leakage current (R + G + B)
   line 13: measurement of red cut-off current
   line 14: measurement of green cut-off current
   line 15: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.

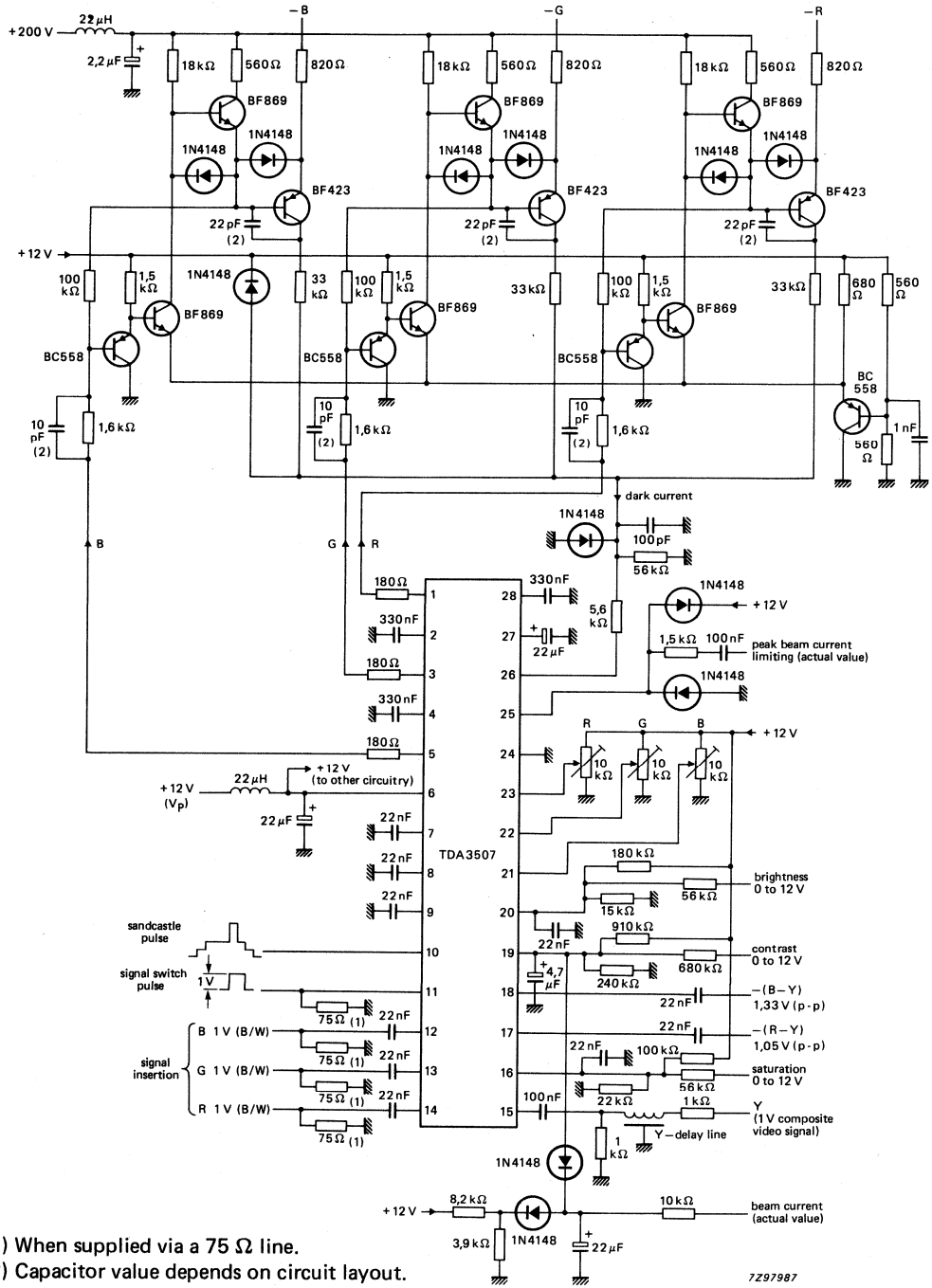
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.

   The internal blanking continues until the end of the last measured line.

   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.

7. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5\ \mu s$.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3507.

PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

QUICK REFERENCE DATA

Supply voltage	V_{1-27}	type.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	5,25	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for data insertion	V_{9-27}	min.	0,9	V
Blanking input voltage	V_{8-27}	typ.	1,5	V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

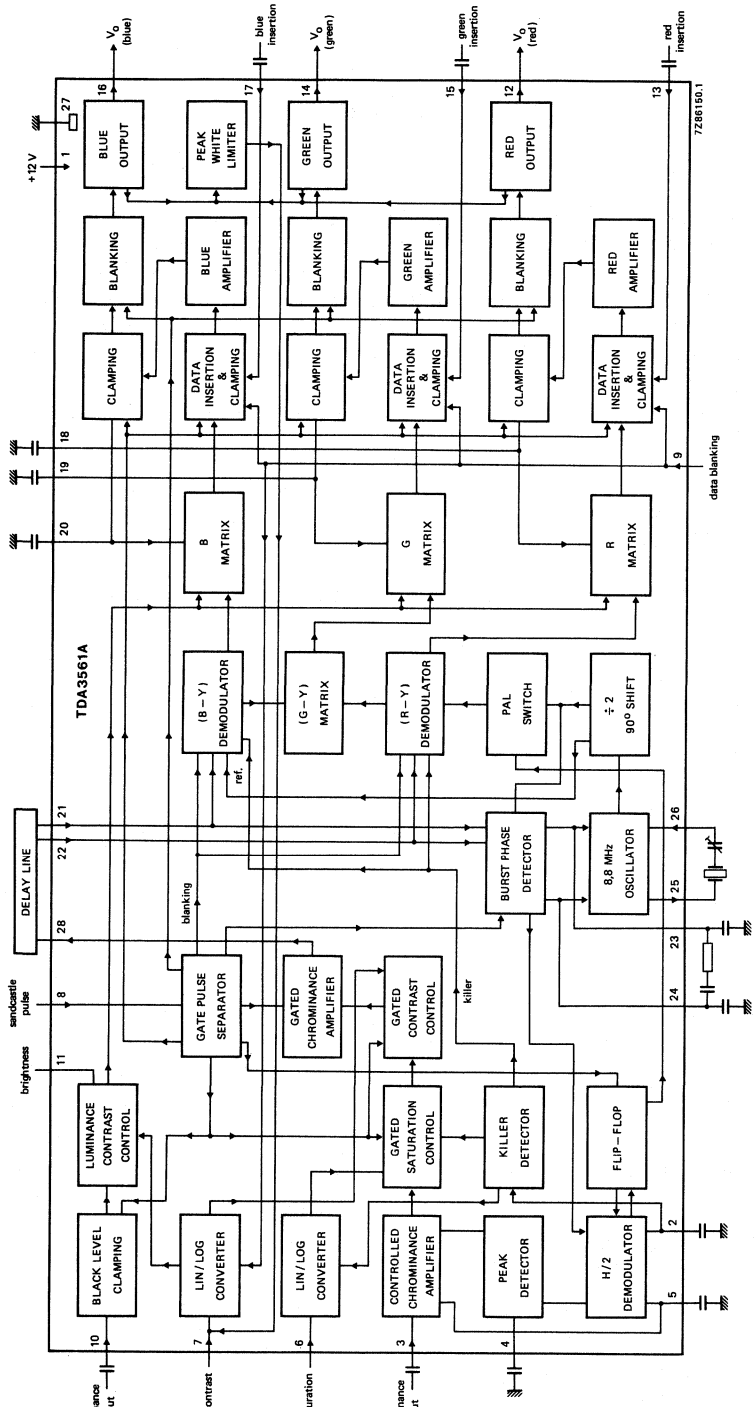


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1-27}$	max.	13,2 V
Total power dissipation; see also Fig. 2	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 65 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{1-27}$	typ.	12 V
			8 to 13,2 V
Supply current		typ.	85 mA
		<	115 mA
Total power dissipation	P_{tot}	typ.	1,0 W
		<	1,4 W
Luminance input (pin 10)			
Input voltage (peak-to-peak value); note 1	$V_{10-27(p-p)}$	typ.	0,45 V
Input level before clipping	V_{10-27}	<	2 V
Input current; input level 2 V, clamp not active	I_{10}	typ.	0,15 μA
		<	1 μA
Contrast control range (see Fig. 3)			−17 to + 3 dB
Control voltage for 40 dB attenuation	V_{7-27}	typ.	1,2 V
Input current contrast control at $V_{7-27} = 3$ V	I_7	<	10 μA
Chrominance amplifier			
Input voltage (peak-to-peak value); note 2	$V_{3-27(p-p)}$	typ.	550 mV
			55 to 1100 mV
Input impedance	$\lvert Z_{3-27}\rvert$	typ.	9 kΩ
			6 to 12 kΩ
Input capacitance	C_{3-27}	typ.	4 pF
		<	6 pF
A.C.C. control range		>	30 dB
Change of the burst signal at the output over the whole control range		<	1,5 dB
Gain at nominal contrast/saturation pin 3 to pin 28; note 3		>	32 dB
Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak	$V_{28-27(p-p)}$	typ.	1,7 V
Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ	$V_{28-27(p-p)}$	typ.	4,0 V

CHARACTERISTICS (continued)

Chrominance amplifier (continued)

Distortion of chrominance amplifier at $V_{28-27(p-p)}$ = 2 V up to $V_{3-27(p-p)}$ = 1 V	d	typ. <	1,5 % 5 %
Frequency response between 0 and 5 MHz			−2 dB
Saturation control range (see Fig. 4)		>	50 dB
Input current saturation control at V_{6-27} = 3 V	I_6	<	15 μA
Tracking between luminance and chrominance with contrast control over a range of 10 dB		<	2 dB
Cross-coupling between luminance and chrominance amplifier; note 10		<	−46 dB
Signal-to-noise ratio at nominal input signal; note 11	S/N	>	56 dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	<	± 5°
Output impedance of chrominance amplifier	$\lvert Z_{28-27}\rvert$	typ.	25 Ω
Maximum output current	I_{28}	<	15 mA

Reference part

Phase locked loop:			
– catching range; note 4		> typ.	500 Hz 700 Hz
– phase shift; note 5		<	5°
Oscillator:			
– temperature coefficient of oscillator frequency; note 4		typ.	−1,5 Hz/K
– frequency deviation for V_P changing from 10 to 13,2 V; note 4		typ.	40 Hz
– input resistance (pin 26)	R_{26-27}	typ. 260 to 420	340 Ω Ω
– input capacitance (pin 26)	C_{26-27}	<	10 pF
– output resistance (pin 25)	R_{25-27}	typ. 100 to 200	150 Ω Ω
– output voltage (peak-to-peak value; pin 25)	$V_{25-27(p-p)}$	typ.	700 mV
A.C.C. generation:			
– reference voltage (pin 4)	V_{4-27}	typ.	4,9 V
– control voltage at nominal input signal (pin 2)	V_{2-27}	typ.	5,1 V
– control voltage without chrominance input (pin 2)	V_{2-27}	typ.	2,65 V
– colour-off voltage (pin 2)	V_{2-27}	typ.	3,15 V
– colour-on voltage (pin 2)	V_{2-27}	typ.	3,4 V
– identification-on voltage (pin 2)	V_{2-27}	typ.	1,9 V
– change in burst amplitude with supply voltage (± 10%)		proportional	
– change in burst amplitude with temperature		typ. <	0,1 %/K 0,25 %/K
– voltage at pin 5 at nominal input signal	V_{5-27}	typ.	5 V

Demodulator part

Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6	$V_{21\text{-}22(p\text{-}p)}$	typ.	100 mV
Input impedance between pins 21 and 22	$\lvert Z_{21\text{-}22}\rvert$	typ.	2 kΩ
Ratio of demodulated signals for equal input signals at pins 21 and 22 (B−Y)/(R−Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78 ± 10%
(G−Y)/(R−Y); no (B−Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	−0,51 ± 10%
(G−Y)/(B−Y); no (R−Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	−0,19 ± 25%
Frequency response between 0 and 1 MHz			−3 dB
Cross talk between colour demodulated signals		>	40 dB
Phase difference between (R−Y) signal and (R−Y) reference signal		<	5°
Phase difference between (R−Y) and (B−Y) reference signals		typ.	90° 85 to 95°

R.G.B. matrix and amplifiers

Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,4 V 4,5 to 6,3 V
Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R−Y) signal	$V_{12\text{-}27(p\text{-}p)}$	typ.	5,25 V 3,7 to 6,7 V
Maximum peak white level; note 7		typ.	9,3 V 9,0 to 9,6 V
Maximum output current	$I_{12,14,16}$	<	15 mA
Black level at the output for a brightness control voltage of 2 V	$V_{12,14,16\text{-}27}$	typ.	2,6 V
Difference in black level between the three channels at an output level of 3 V; note 8	ΔV	<	200 mV
Black level shift with vision contents		<	40 mV
Brightness control voltage range	see Fig. 5		
Input current brightness control	I_{11}	<	50 μA
Variation of black level with temperature	ΔV	typ. <	0,35 mV/K 1,0 mV/K
Variation of black level with contrast control	ΔV	typ. <	10 mV 200 mV
Relative spread between the R, G and B output signals		<	10 %
Relative black-level variation between the three channels during variation of contrast and supply voltage		typ. <	0 mV 20 mV

CHARACTERISTICS (continued)

RGB matrix and amplifier (continued)

Differential black-level drift over a temperature range of 40 °C		typ.	0	mV
		<	20	mV
Blanking level at the RGB outputs		typ.	2,1	V
			1,9 to 2,3	V
Difference in blanking level of the three channels		typ.	0	mV
Differential blanking level drift over a temperature range of 40 °C		typ.	0	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	typ.	1,1	
Signal-to-noise ratio of output signals; note 11	S/N	>	62	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		typ.	40	mV
		<	150	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		typ.	75	mV
		<	150	mV
Output impedance of RGB outputs	$\lvert Z_{12,14,16\text{-}27} \rvert$	typ.	50	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3	dB

Signal insertion (pins 13,15 and 17)

Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	1	V
			0,85 to 1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output; note 9	ΔV	<	260	mV
Output rise time	t_r	typ.	40	ns
		<	80	ns
Differential delay time for the three channels	t_d	typ.	0	ns
		<	40	ns
Input current	$I_{13,15,17}$	<	10	μA

Data blanking (pin 9)

Input voltage for no data insertion	$V_{9\text{-}27}$	<	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	>	0,9	V
Maximum input voltage	$V_{9\text{-}27}$	<	3	V
Delay of data blanking	t_d	<	20	ns
Input current	I_9	<	35	μA
Input impedance	$\lvert Z_{9\text{-}27} \rvert$	typ.	10	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0,9$ V		>	46	dB

Sandcastle input (pin 8)

Level at which the RGB blanking is activated	$V_{8\text{-}27}$	typ.	1,5 V
			1 to 2 V
Level at which burst gating and clamping pulse are separated	$V_{8\text{-}27}$	typ.	7,0 V
			6,5 to 7,5 V
Delay between black level clamping and burst gating pulse	t_d	typ.	0,4 μs
Input current for:			
$V_{8\text{-}27}$ = 0 to 1 V	$-I_8$	<	1 mA
$V_{8\text{-}27}$ = 1 to 8,5 V	I_8	typ.	20 μA
$V_{8\text{-}27}$ = 8,5 to 12 V	I_8	<	2 mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

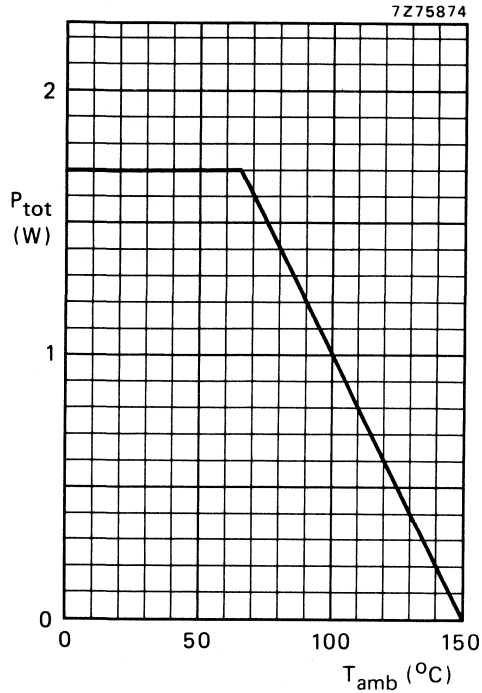


Fig. 2 Power derating curve.

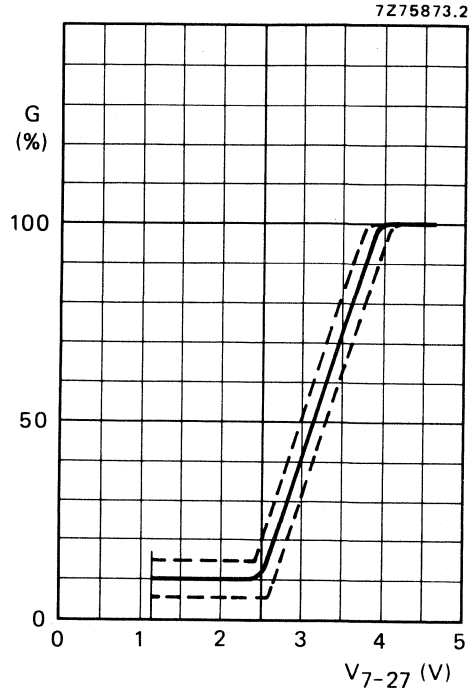


Fig. 3 Contrast control voltage range.

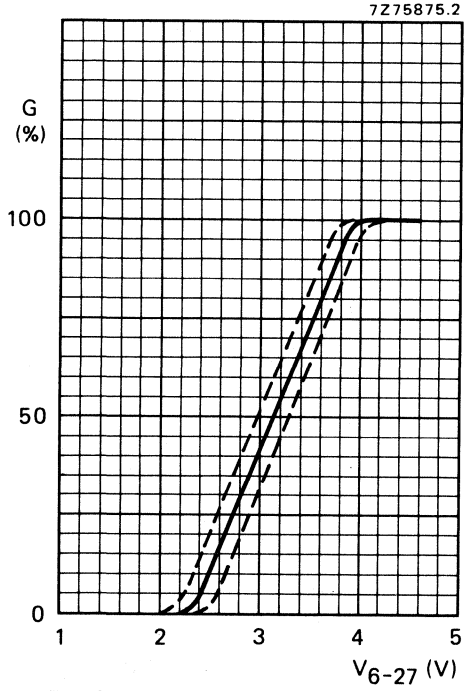


Fig. 4 Saturation control voltage range.

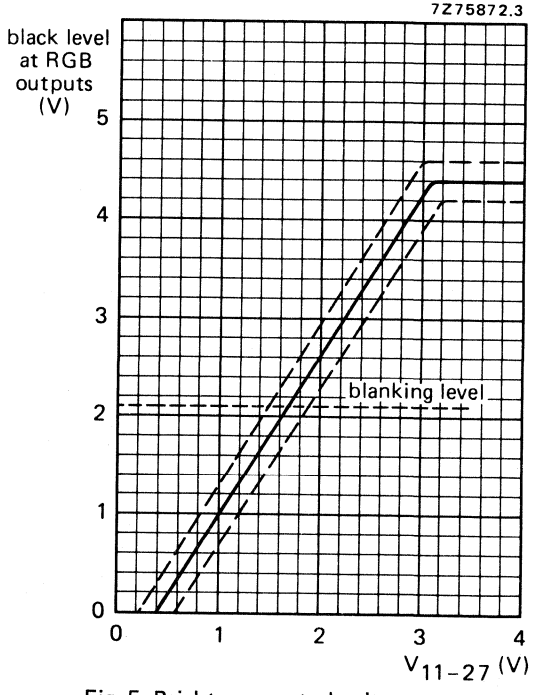


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

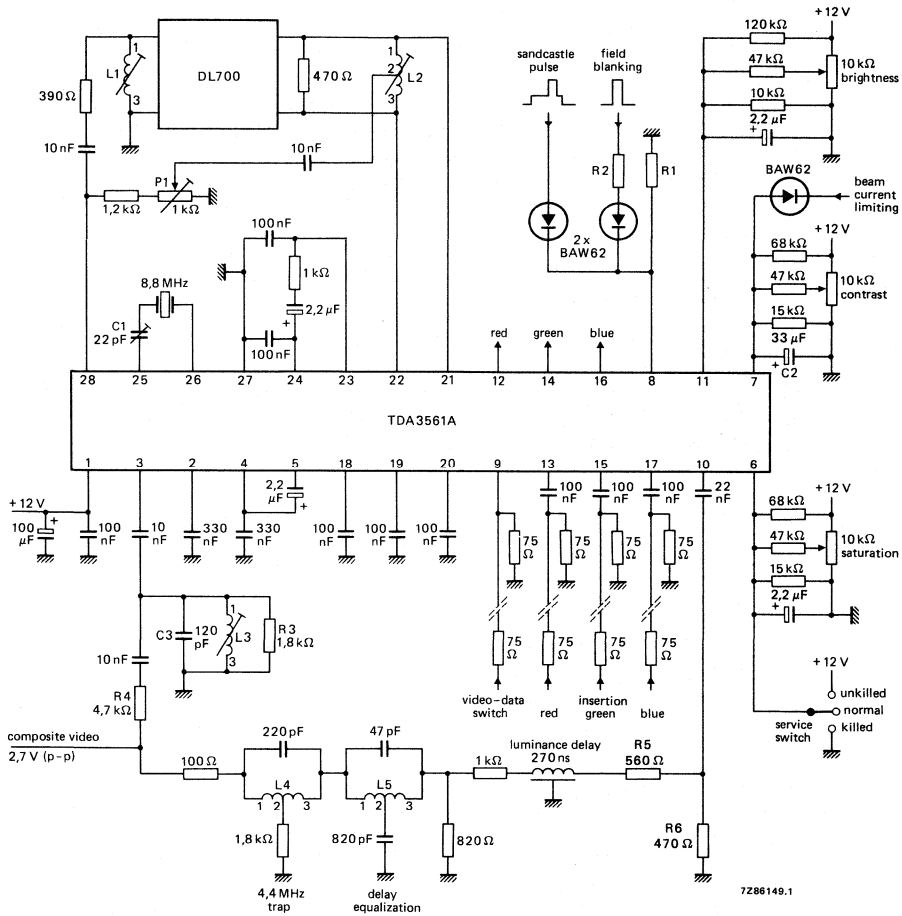


Fig. 6 Application circuit.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 µH
L2	nominal value	= 10,7 µH
L3	4,4 MHz chrominance input filter	= 10,7 µH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 µH
L5	delay equalization	= 66,1 µH
P1	amplitude of direct chroma singal	
R1 R2	field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short ($<$ 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

PAL DECODER

GENERAL DESCRIPTION

The TDA3565 PAL decoder contains all the functions required for PAL signal decoding and colour matrixing and is contained within an 18-pin package. The oscillator, a.c.c. detector and burst phase detector each have single-pin outputs and the coupling capacitor for the luminance input at pin 8 doubles as a storage capacitor for the black level clamping circuit. Black level clamping of the three colour channels is performed using feedback proportional to the red channel black level. This feedback (variable with the brightness control) controls the input level of the luminance amplifier and therefore the clamping levels of all three colour signal outputs.

QUICK REFERENCE DATA

Supply voltage	$V_p = V_{1-17}$	typ.	12 V
Supply current	$I_p = I_1$	typ.	85 mA
Luminance input signal (peak-to-peak value)	$V_{8-17(p-p)}$	typ.	0,45 V
Chrominance input signal (peak-to-peak value)	$V_{3-17(p-p)}$	typ.	550 mV
RGB output signal amplitudes (peak-to-peak value) at nominal luminance and contrast	$V_{10,11,12-17(p-p)}$	typ.	5 V
Contrast control range			−17 to +3 dB
Saturation control range		>	50 dB
A.C.C. control range		>	30 dB
Level at which RGB blanking is activated	V_{7-17}	typ.	1,5 V
Level at which burst gate/clamping pulse are separated	V_{7-17}	typ.	7 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

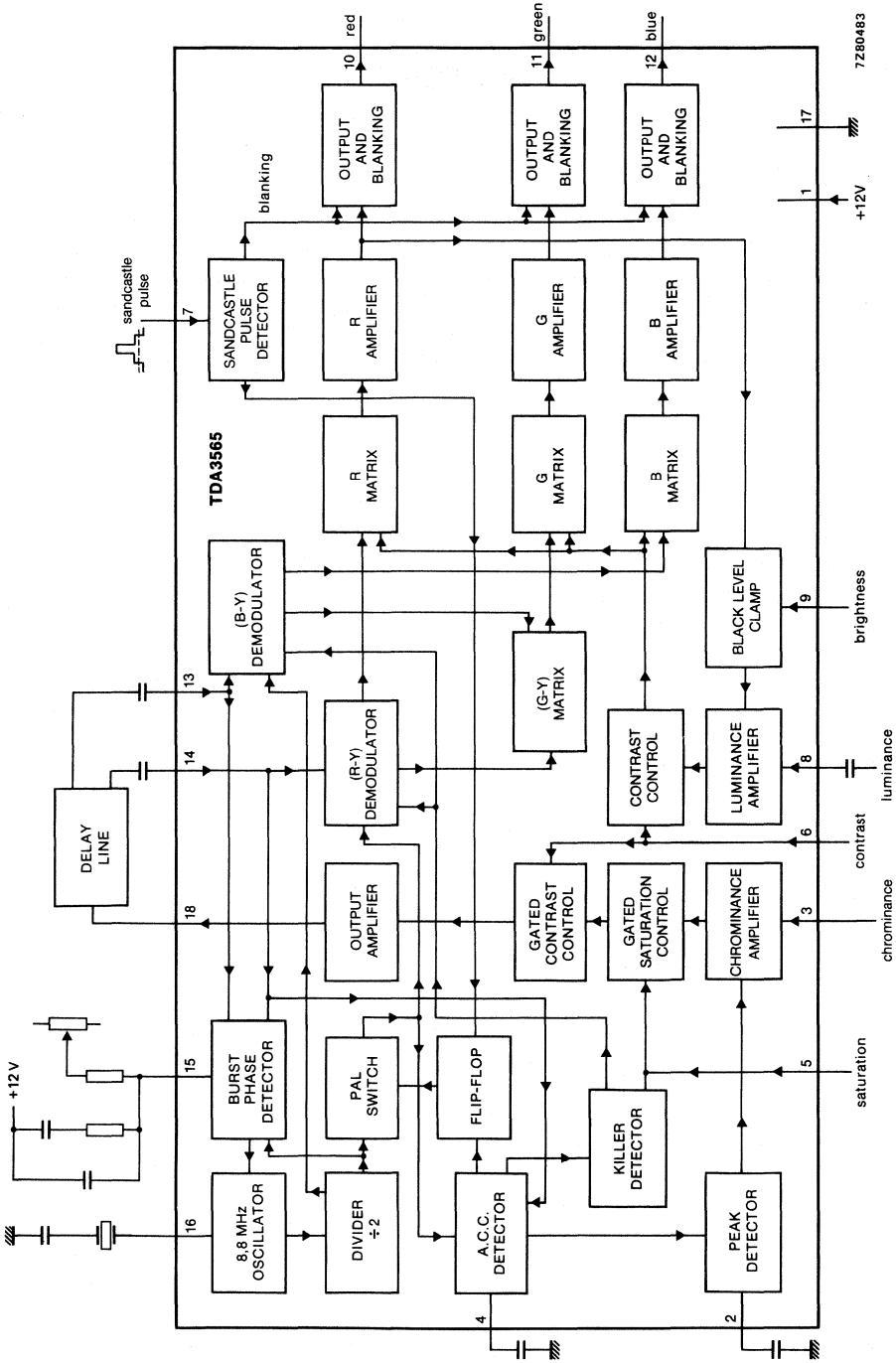


Fig. 1 Block diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	max.	50	K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	V_{1-17}	9,0	12,0	13,2	V
Supply current	I_1	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier					
Input signal amplitude (note 1) (peak-to-peak value)	$V_{8-17(p-p)}$	–	0,45	–	V
Input level before clipping occurs *	$V_{8-17(p-p)}$	–	–	0,7	V
Input current at $V_{8-17} = 2$ V; clamp not active	I_8	–	0,15	1,0	μA
Contrast control range (Fig. 2)		–	−17 to +3	–	dB
Input current when peak white limiter is active ($V_{6-17} = 2{,}5$ V)	I_8	–	5,5	–	mA
Input resistance $V_{6-17} > 6$ V	R_i	1,4	2,0	2,6	kΩ
Chrominance amplifier					
Input signal amplitude (note 2)	$V_{3-17(p-p)}$	55	550	1100	mV
Minimum burst signal amplitude within the control range (peak-peak)		30	–	–	mV
Input impedance	Z_{3-17}	–	8,0	–	kΩ
Input capacitance	C_{3-17}	–	4,0	6,0	pF
A.C.C. control range		30	–	–	dB
Change of burst signal at output over whole a.c.c. control range		–	–	1	dB
Amplification pin 3 to pin 18 at nominal contrast/saturation (note 3)		32	–	–	dB

* At nominal contrast and nominal brightness.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Chroma to burst ratio (note 3)		–	3,8	–	dB
Max. output voltage range (pin 18) $R_L = 2\ k\Omega$		4,0	4,5	–	V
Chrominance amplifier distortion at $V_{8\text{-}17(p\text{-}p)} = 2$ V (output) up to $V_{3\text{-}17(p\text{-}p)} = 1$ V (input)	$d_{8\text{-}3}$	–	3,0	5,0	%
Frequency response between 0 and 5 MHz		–	–	–2	dB
Saturation control range (Fig. 3)		50	–	–	dB
Saturation control input current at $V_{5\text{-}17} < 6$ V	I_5	–	1	20	μA
Input impedance for V_5 between 6 and 10 V	Z_i	1,4	2,0	2,6	kΩ
Input impedance when colour killer is active	Z_i	1,4	2,0	2,6	kΩ
Input impedance for $V_5 > 10$ V (adjustment procedure)	Z_i	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance over 10 dB of contrast control range		–	–	2	dB
Cross coupling between luminance and chrominance amplifiers (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Burst phase shift with respect to chrominance at nominal contrast/saturation (note 3)	$\Delta\varphi$	–	–	±5	deg
Chrominance amplifier output impedance	$Z_{18\text{-}17}$	–	25	–	Ω
Output current (pin 18)	I_{18}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of oscillator frequency	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency	TC_{osc}	–	2	3	Hz/K
Frequency deviation when supply voltage changes from 10 to 13,2 V	Δf_{osc}	–	200	300	Hz

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Input resistance	$R_{16\text{-}17}$	250	290	330	Ω
Input capacitance	$C_{16\text{-}17}$	–	–	10	pF
A.C.C. generation					
Voltage with nominal input signal	$V_{4\text{-}17}$	–	5,0	–	V
Voltage without chrominance input	$V_{4\text{-}17}$	–	2,5	–	V
Colour-off voltage	$V_{4\text{-}17}$	–	3,2	–	V
Colour-on voltage	$V_{4\text{-}17}$	–	3,5	–	V
Identification-on voltage	$V_{4\text{-}17}$	–	2,5	–	V
Pin 2 voltage at nominal input signal	$V_{2\text{-}17}$	–	5,1	–	V
Demodulator part					
Burst signal amplitude (peak-to-peak value) at pins 13 and 14 (note 6)	$V_{13\text{-}17(p\text{-}p)}$ $V_{14\text{-}17(p\text{-}p)}$	–	80	–	mV
Input impedance of pins 13 or 14 to pin 17	$Z_{13,\,14\text{-}17}$	–	1,0	–	kΩ
Ratios of demodulated signals with equal signal inputs to pins 13 and 14 and no luminance input signal:					
(B-Y)/(R-Y)	$\frac{V_{12\text{-}17}}{V_{10\text{-}17}}$	–	1,78±10%	–	
(G-Y)/(R-Y) (no (B-Y) signal)	$\frac{V_{11\text{-}17}}{V_{10\text{-}17}}$	–	−0,51±10%	–	
(G-Y)/(B-Y) (no (R-Y) signal)	$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,19±10%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
Separation of colour difference channels		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output signal amplitudes (peak-to-peak value) at nominal luminance signal and contrast inputs (black-white) (note 3)	$V_{10\text{-}17(p\text{-}p)}$ $V_{11\text{-}17(p\text{-}p)}$ $V_{12\text{-}17(p\text{-}p)}$	4,5	5,0	5,5	V
Red channel output amplitude (peak-to-peak value) at nominal contrast/saturation (note 3) and no luminance signal to (R-Y)	$V_{10\text{-}17(p\text{-}p)}$	3,7	5,25	7,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Maximum peak white level (note 7)		9,0	9,3	9,6	V
Maximum output current	$I_{10,11,12}$	–	–	15	mA
Red channel black level output when brightness control $V_{9-17} = 2$ V	V_{10-17}	–	2,7	–	V
Difference between black levels in R, G and B outputs		–	–	600	mV
Black level shift with picture content		–	–	40	mV
Brightness control voltage range	V_{9-17}		see Fig. 3		
Brightness control input current at $V_{9-17} = 2$ V	I_9	–	–	–50	μA
Variation of black level with temperature		–	+0,35	1,0	mV/K
Variation of black level with contrast control		–	10	100	mV
Relative spread between the three channel outputs		–	–	10	%
Relative variation in black level between the three channels during normal variations of contrast and supply voltage		–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		–	0	20	mV
Blanking level at the three channel outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channel outputs		–	0	–	mV
Differential drift of blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black levels with variation of supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz component in output signals (peak-to-peak value)		–	25	50	mV
Residual 8,8 MHz and higher harmonic components in output signals (peak-to-peak value)		–	25	50	mV
Output impedance	$Z_{10,11,12-17}$	–	50	–	Ω
Frequency response of total luminance/RGB amplifier circuits for 0 to 5 MHz		–	–	–3	dB

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector					
Level at which RGB blanking is activated	V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate and clamping pulse are separated	V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		–	0,4	–	μs
Input current at:					
V_{7-17} = 0 to 1 V	I_7	–	–	−1	mA
V_{7-17} = 1 to 8,5 V	I_7	–	20	40	μA
V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync pulse, amplitude includes sync pulse amplitude.
2. The signal indicated is for a colour bar with 75% saturation, so the chroma burst ratio of 2,2 : 1.
3. Nominal contrast is defined as (maximum contrast −3 dB) and nominal saturation is (maximum saturation −12 dB).
4. Cross coupling is measured under the following condition; input signals nominal and contrast/saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded the amplitude of the output signal is reduced via a discharge of the capacitor at pin 6 (contrast control). The discharge current is 5,5 mA.

DEVELOPMENT DATA

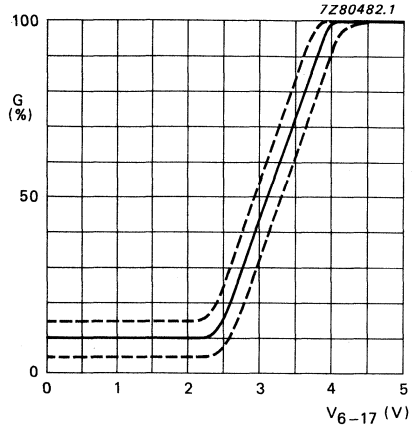


Fig. 2 Luminance contrast control voltage range.

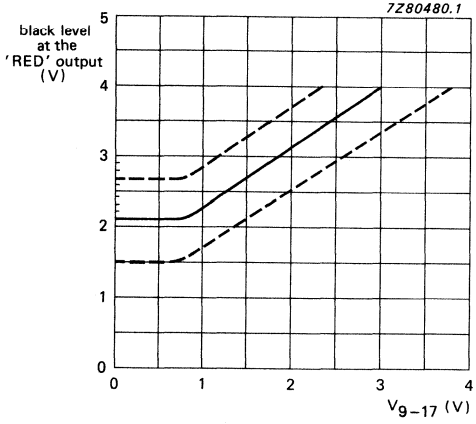


Fig. 3 Brightness control voltage range.

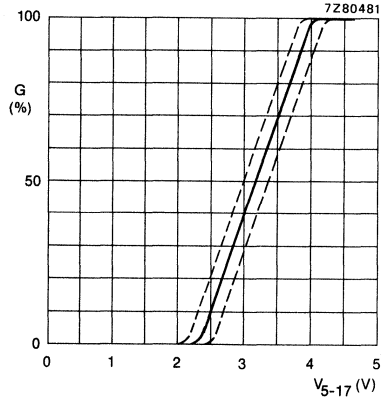


Fig. 4 Saturation control voltage range.

APPLICATION INFORMATION

DEVELOPMENT DATA

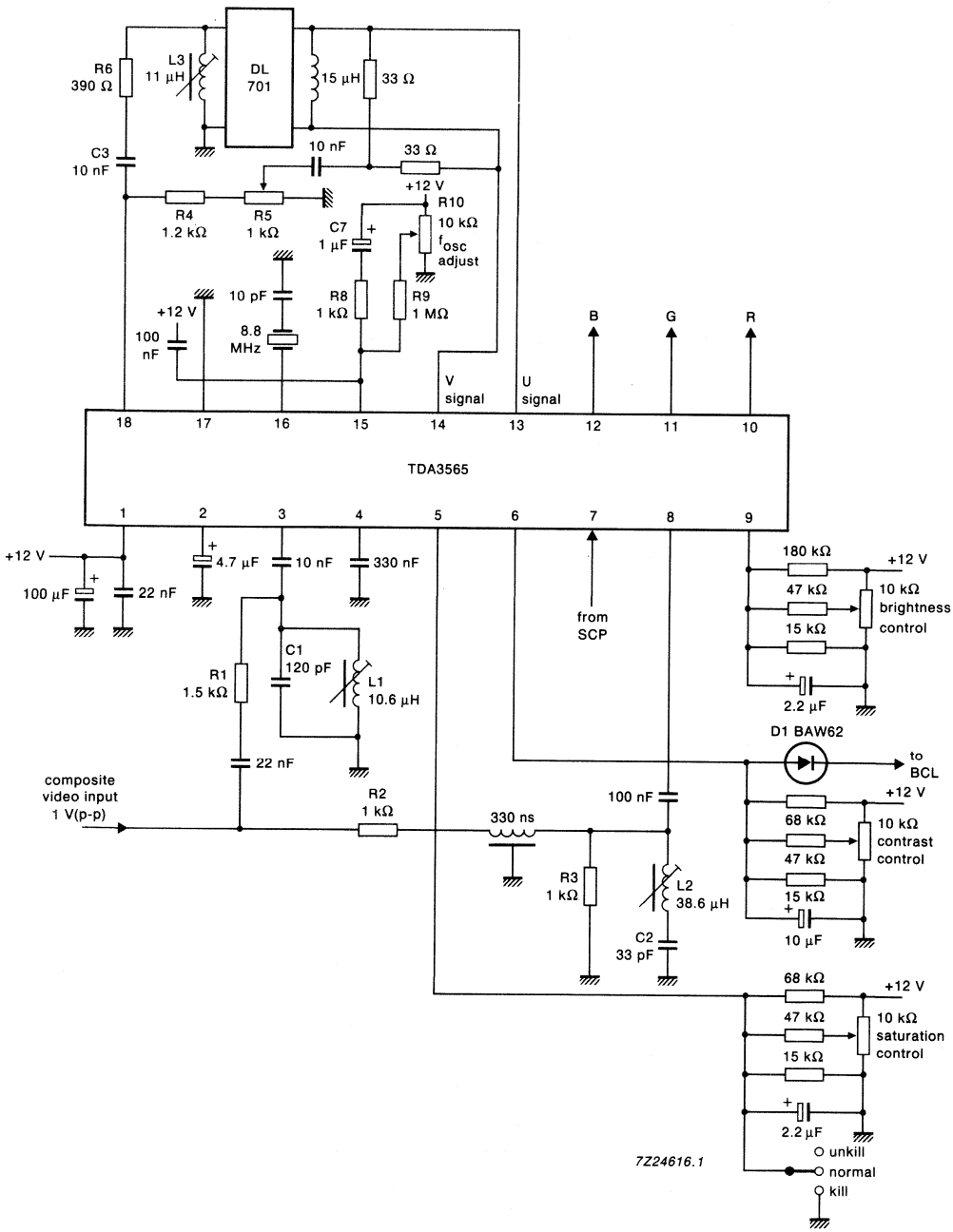


Fig. 5 Application diagram

PAL/NTSC DECODER

GENERAL DESCRIPTION

The TDA3566 is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	80 mA
Luminance amplifier (pin 8)			
Input voltage (peak-to-peak value)	$V_{8-27(p-p)}$	typ.	450 mV
Contrast control range		typ.	20 dB
Chrominance amplifier (pin 4)			
Input voltage range (peak-to-peak value)	$V_{4-27(p-p)}$	40 to	1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13, 15, 17-27(p-p)}$	typ.	4 V
Data insertion			
Input signals (peak-to-peak value)	$V_{12, 14, 16-27(p-p)}$	typ.	1 V
Data blanking (pin 9)			
Input voltage for data insertion	V_{9-27}	min.	0,9 V
Sandcastle input (pin 7)			
Blanking input voltage	V_{7-27}	typ.	1,5 V
Burst gating and clamping input voltage	V_{7-27}	typ.	7 V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

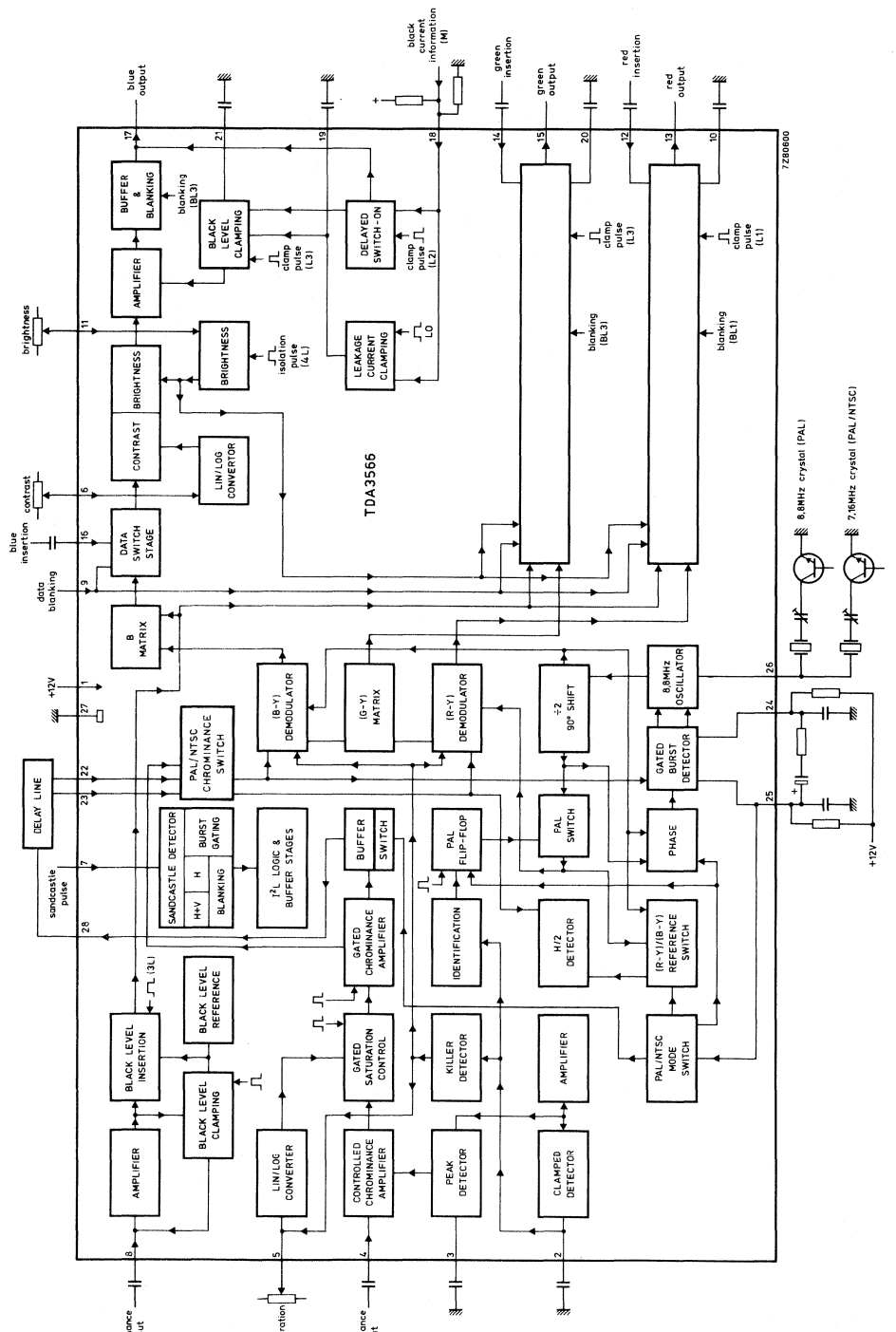


Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC-application has largely been simplified. In the case of NTSC the chroma signal is now internally coupled to the demodulators, ACC and phase detectors. The chroma output signal (pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566.
  Furthermore there is no difference between the amplitude of the colour output signals in the PAL or NTSC mode. The PAL/NTSC-switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behaviour of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the pins 10, 20 and 21 can be reduced to 100 nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10 pF.

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. Form the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.
In the case of NTSC the chroma signal is internally coupled to the demodulators, ACC and phase detector.

FUNCTIONAL DESCRIPTION (continued)

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90^{o} phase shift between them.
The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.
Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3566 is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)
Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 V and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is + 3 dB to −17 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).
During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.
The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs.
To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.
The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.
The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.
Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.
To prevent parasitic oscillations on the third overtone of the crystal the optimal tuning capacitance should be 10 pF.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to	+ 150 °C
Operating ambient temperature range	T_{amb}	−25 to	+ 70 °C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	40 K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10,8	12	13,2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0,95	1,3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8-27(p-p)}$	–	0,45	0,63	V
Input level before clipping	V_{8-27}	–	–	1.4	V
Input current	I_8	–	0,1	1	μA
Contrast control range (see Fig. 2)		−15	–	+5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4-27(p-p)}$	40	390	1100	mV
Input impedance (pin 4)	$\lvert Z_{4-27}\rvert$	–	10	–	kΩ
Input capacitance	C_{4-27}	–	–	6,5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range	ΔV	–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)	G	34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	$V_{28-27(p-p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	α_{28-4}	–	–	−2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	−46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA
Reference part					
Phase-locked-loop catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\varphi$	–	–	5	deg
Oscillator temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–2	–3	Hz/K
frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	100	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	280	400	520	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2) control voltage at nominal input signal	$V_{2\text{-}27}$	–	4,5	–	V
control voltage without chrominance input	$V_{2\text{-}27}$	–	2	–	V
colour-off voltage	$V_{2\text{-}27}$	–	2,8	–	V
colour-on voltage	$V_{2\text{-}27}$	–	3	–	V
identification-on voltage	$V_{2\text{-}27}$	–	1,7	–	V
change in burst amplitude with temperature		–	0,1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5,1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	68	80	95	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	0,7	1	1,3	kΩ
Ratio of demodulated signals (note 8)					
(B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1,78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	–0,51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	–0,19 ± 10%	–	

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Demodulator part (continued)					
Frequency response between 0 and 1 MHz	α_{17}	–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signals	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) signal and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17-27(p-p)}$	3,5	4	4,5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13-27(p-p)}$	–	4,2	–	V
Maximum peak-white level	$V_{13,15,17\ (m)}$	9,7	10	10,3	V
Available output current (pins 13, 15 17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17-27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)	ΔV	–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; V_{11-17} = 2 V		–	–	± 2	V
Black level shift with vision contents	ΔV	–	–	40	mV
Brightness control voltage range		see Fig. 4			
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)*	ΔV	–	0	20	mV
Differential black-level drift over a temperature range of 40 °C	ΔV	–	0	20	mV
Blanking level at the RGB outputs	V_{bl}	–	0,95	1,1	V

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Difference in blanking level of the three channels	V_{bl}	–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C	V_{bl}	–	0	10	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	0,9	1	1,1	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0,5	dB
Output signal during the clamp pulse (3L) after switch-on	V_O	7,5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	50	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17-27} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 9 MHz	α	–	–1	–3	dB
Current source of output stage	I_O	2	3	–	mA
Difference of black level at the three outputs at nominal brightness*	ΔV	–	–	10	mV
Tracking of brightness control		–	–	2	%
Signal insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for and RGB output voltage of 3.5 V (peak-to-peak) at nominal contrast	$V_{12,14,16-27(p-p)}$	0,9	1	1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	50	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA

* With respect to the measuring pulses.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	$R_{9\text{-}27}$	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V		46	–	–	dB
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	$V_{7\text{-}27}$	1	1,5	2	V
Level at which the horizontal pulses are separated	$V_{7\text{-}27}$	3	3,5	4	V
Level at which burst gating and clamping pulse are separated	$V_{7\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,6	–	μs
Input current					
at $V_{7\text{-}27}$ = 0 to 1 V	$-I_7$	–	–	1	mA
at $V_{7\text{-}27}$ = 1 to 8,5 V	I_7	–	–	50	μA
at $V_{7\text{-}27}$ = 8,5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
Bias voltage (d.c.)	$V_{18\text{-}27}$	3,5	5	7,0	V
Difference between input voltage for 'black' current and leakage current	ΔV	0,35	0,5	0,65	V
Input current during 'black' current	I_{18}	–	–	1	μA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	$V_{18\text{-}27}$	8,5	9	9,5	V
Switching threshold for 'black' current control ON	$V_{18\text{-}27}$	7,6	8	8,4	V
Input resistance during scan	$R_{18\text{-}27}$	1	1,5	2	kΩ
Input current during scan at pins 10, 20 and 21 (d.c.)	$I_{10,\ 20,\ 21}$	–	–	tbf	nA
Maximum charge/discharge current during measuring time		–	1	–	nA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	$V_{24\text{-}25}$	–	8,8	9,2	V
Average output current (note 12)	$I_{24+25(AV)}$	75	90	105	μA
Hue control		see Fig. 5			

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

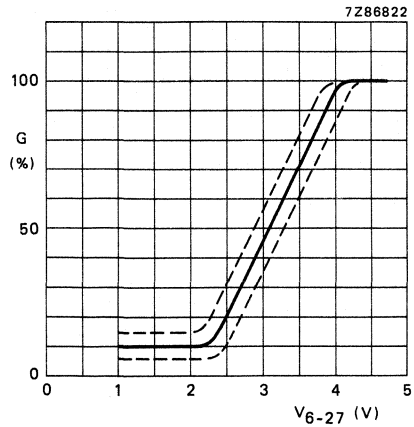


Fig. 2 Contrast control voltage range.

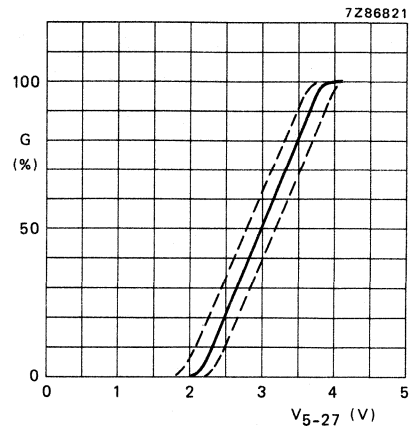


Fig. 3 Saturation control voltage range.

DEVELOPMENT DATA

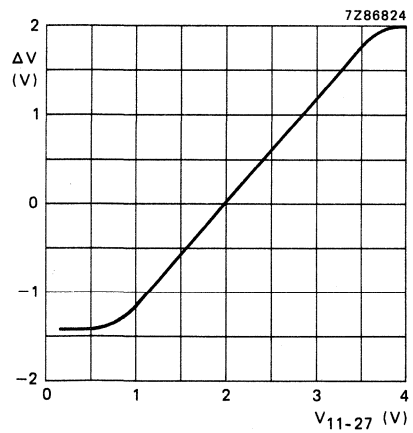


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

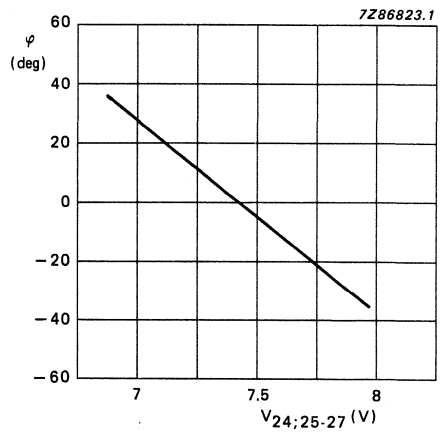


Fig. 5 Hue control voltage range.

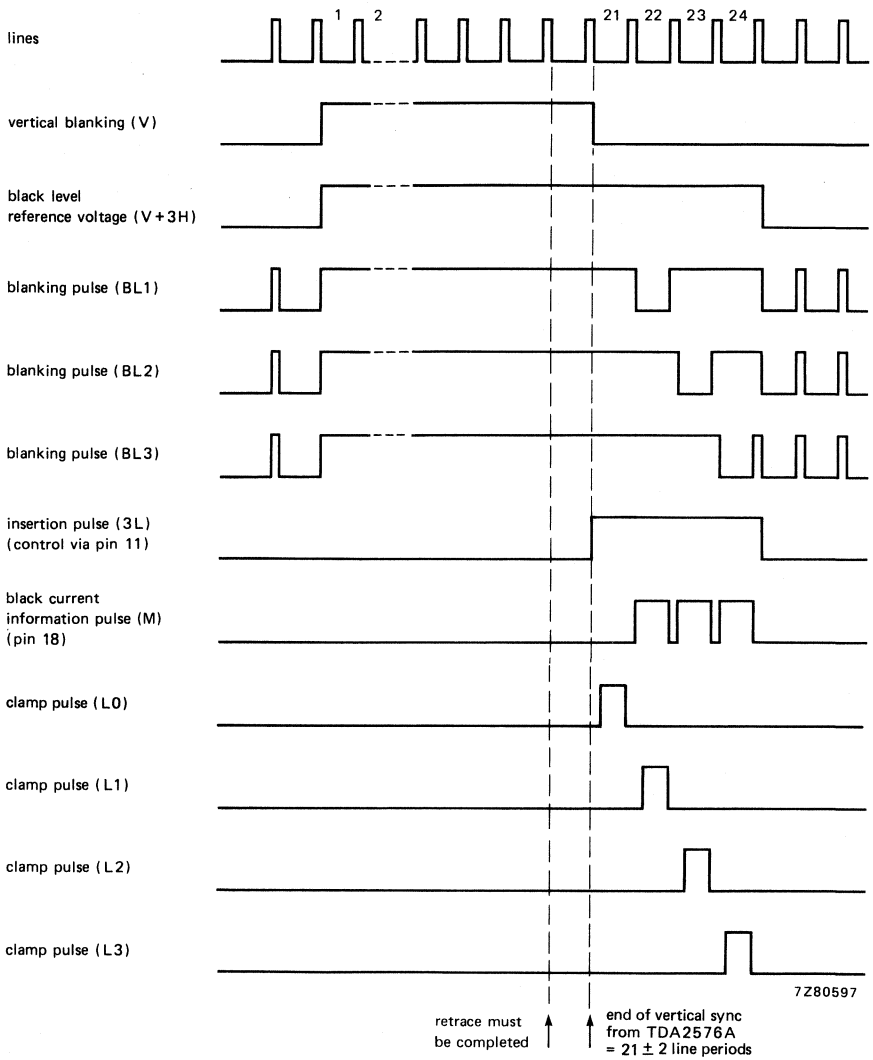


Fig. 6 Timing diagram for black-current stabilizing.

DEVELOPMENT DATA

APPLICATION INFORMATION

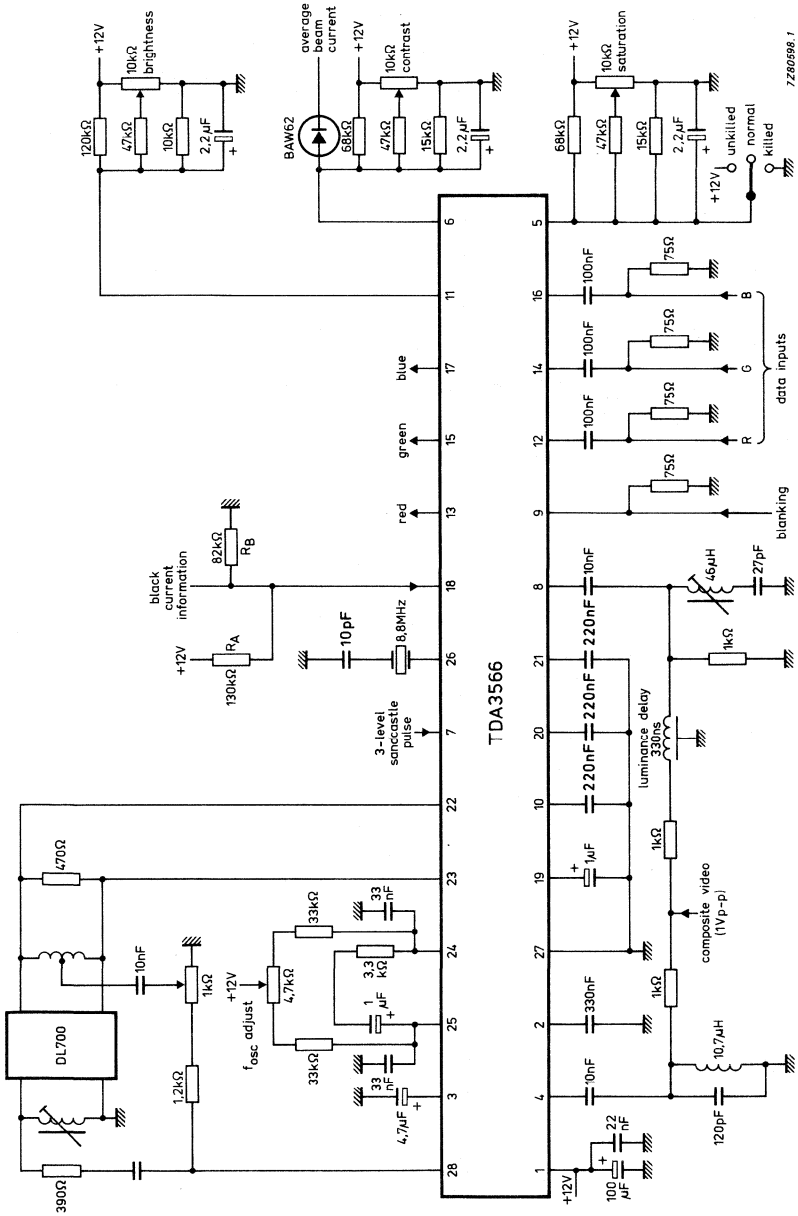


Fig. 7 Application diagram showing the TDA3566 for a PAL decoder.

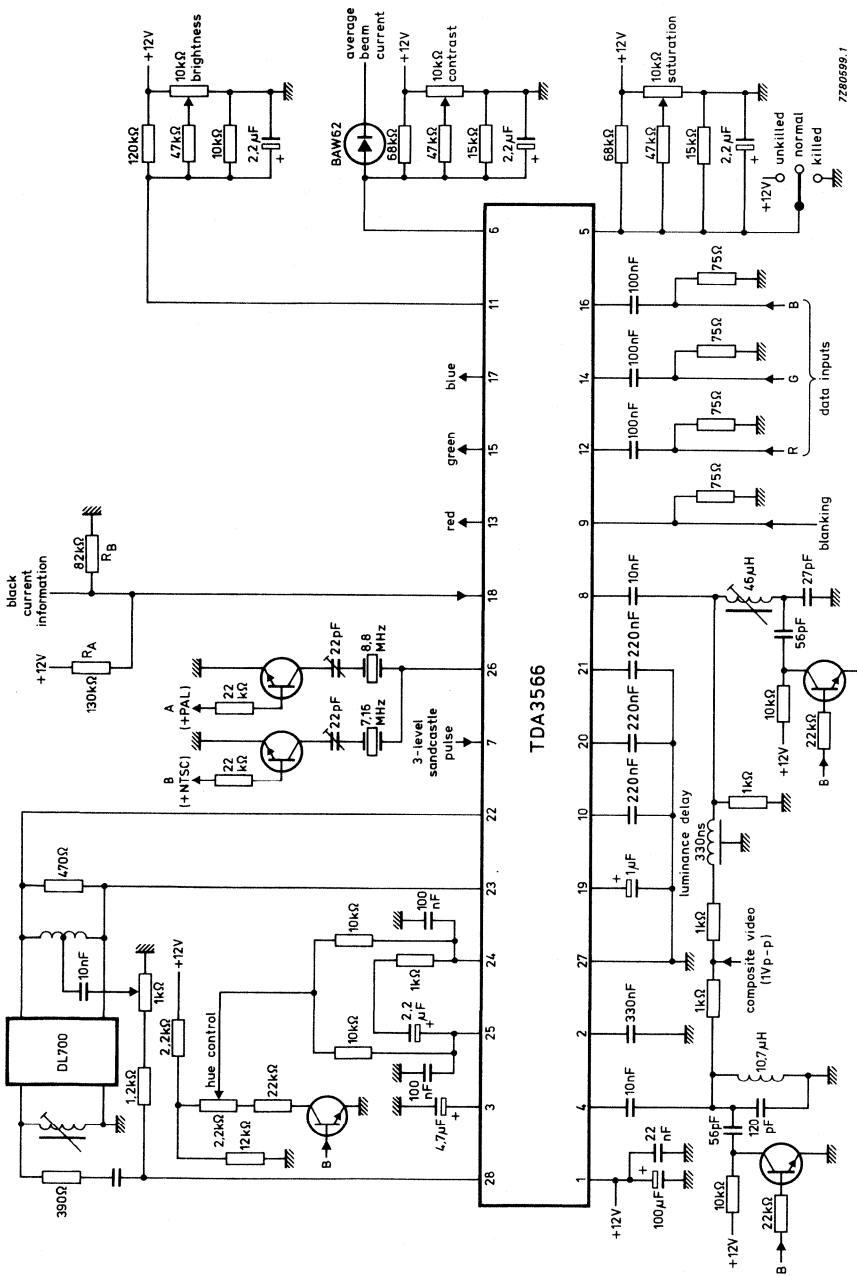


Fig. 8 Application diagram showing the TDA3566 for a PAL/NTSC decoder.

DEVELOPMENT DATA

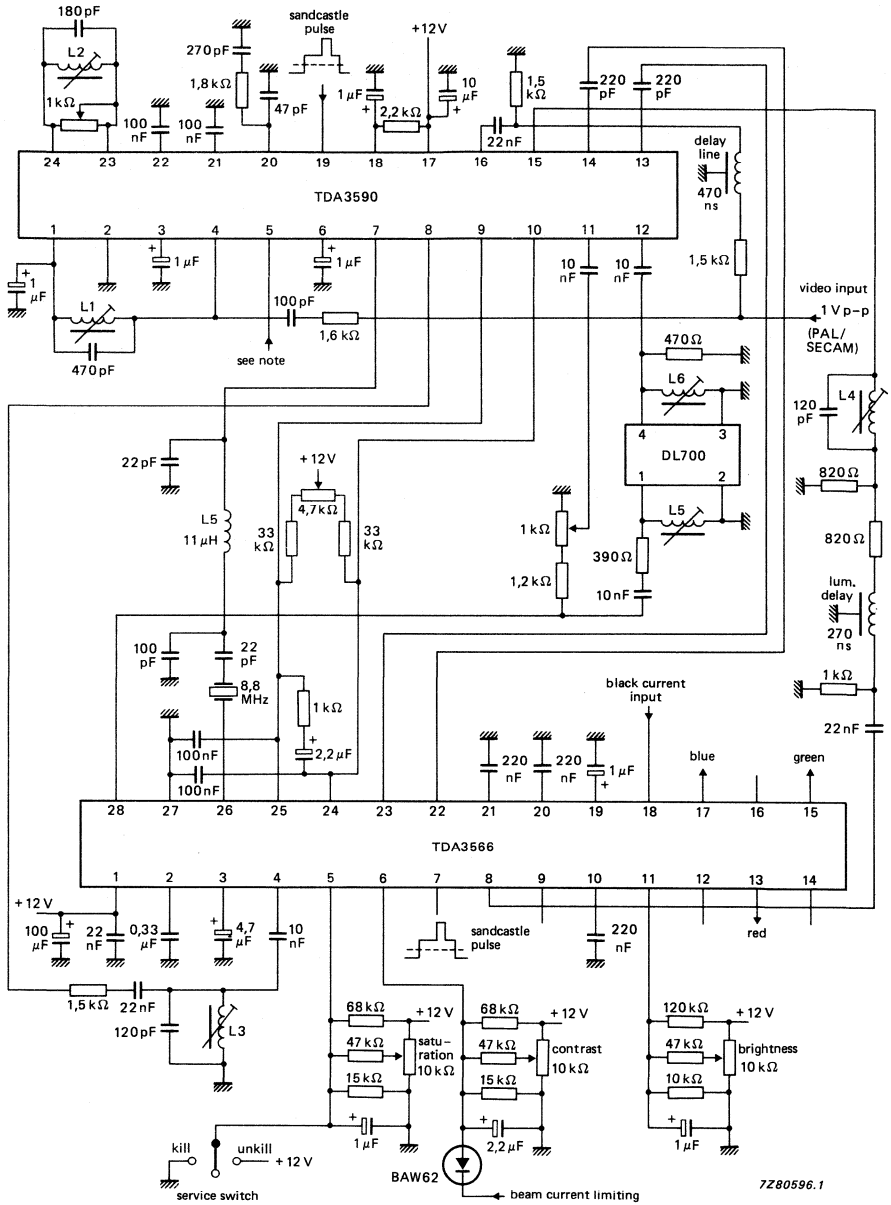


Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3566.

Note to pin 5 TDA3590:

$V_{5-2} < 1$ V; horizontal identification and black level clamping.
$V_{5-2} > 11$ V; vertical identification and artificial black level.
V_{5-2} = 5 to 7 V; horizontal identification and artificial black level.

NTSC DECODER

GENERAL DESCRIPTION

The TDA3567 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Further more it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-17}$	9	12	13,2	V
Supply current	pin 1	$I_P = I_1$	–	65	–	mA
Luminance input signal	pin 8					
Input voltage (peak-to-peak value)		$V_{8-17(p-p)}$	–	0,45	–	V
Contrast control range			–	20	–	dB
Chrominance amplifier	pin 3					
Input voltage (peak-to-peak value)		$V_{3-17(p-p)}$	–	550	–	mV
Saturation control range			50	–	–	dB
RGB matrix and amplifiers						
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)		$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Sandcastle input	pin 7					
Blanking input voltage		V_{7-17}	1,0	1,5	2,0	V
Burst gating and clamping input voltage		$V_{7-17(p-p)}$	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heatspreader (SOT102).

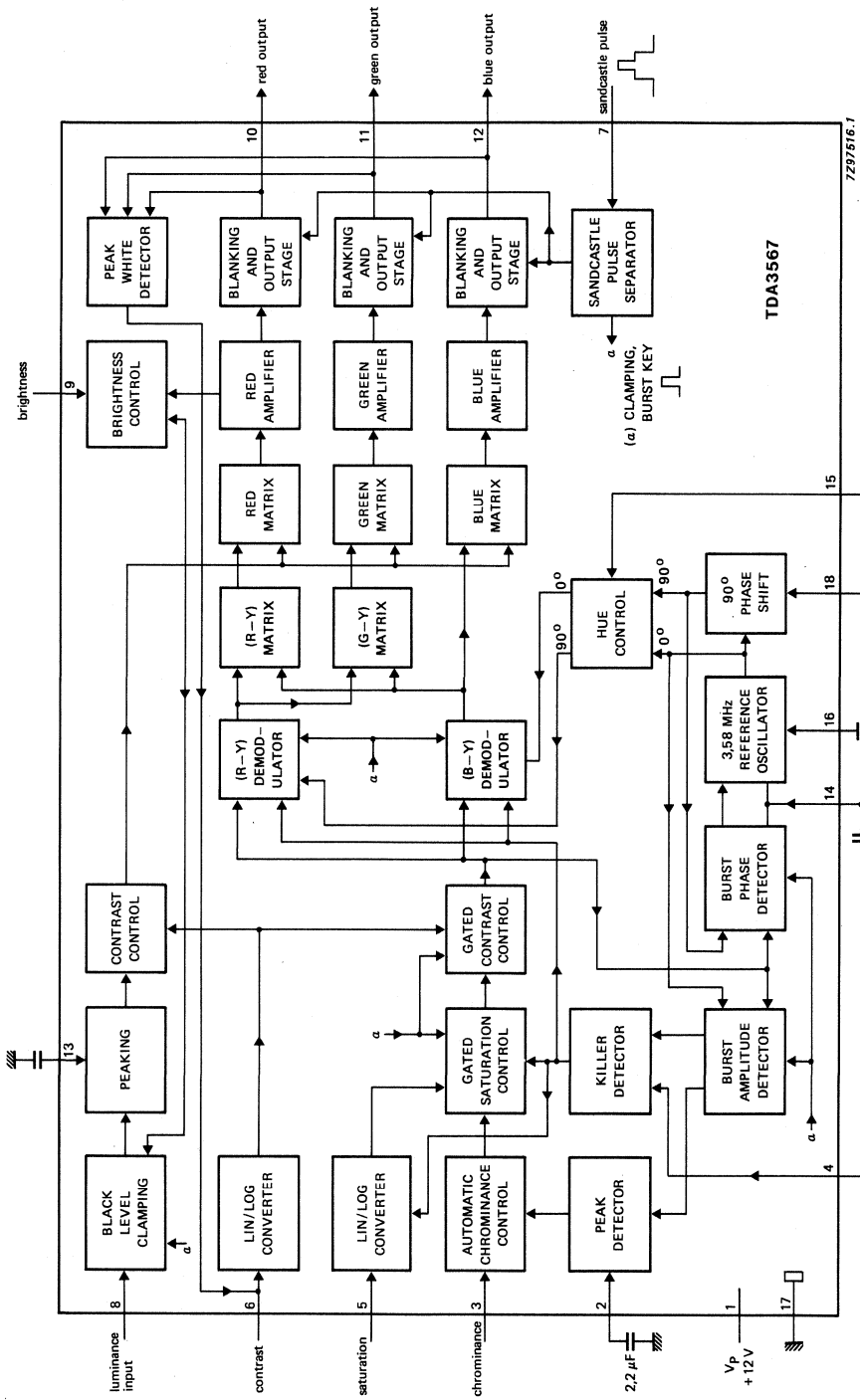


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak*. The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal must be a.c. coupled to the input pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping the signal is fed to a peaking stage. The RC network connected to pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally −17 to + 3 dB. The linear curve of the contrast control voltage is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be a.c. coupled, and must have an amplitude of 550 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V. The impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and a.c.c. detectors.

DEVELOPMENT DATA

Oscillator and a.c.c. circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free running frequency of the oscillator can be checked by connecting the saturation control (pin 5) to the positive supply line. Then the loop is opened, so that the frequency can be measured. The oscillator has an internal gain limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0^{o} reference signal by the burst amplitude detector and is then amplified and fed to a peak detector for a.c.c. and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90^{o} phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0^{o} and 90^{o} before they are fed to the (R-Y) and (B-Y) demodulators. The 90^{o} phase shifted signal is provided by a miller integrator (biased by pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

* Signal with negative going sync; amplitude includes sync pulse amplitude.

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 0°, the phase angle of the (B-Y) reference signal is 90°.

For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$

$(G\text{-}Y)_{matrixed} = 0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$

$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes, when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio B-Y/R-Y = 1,78.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input 1 : 2.2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{1-17}$	9	12	13,2	V
Supply current		$I_P = I_1$	–	65	–	mA
Total power dissipation		P_{tot}	–	0,78	–	W
Luminance input signal						
Input voltage (peak-to-peak value)	note 1 pin 8	$V_{8-17(p-p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_{8-17}	–	–	1	V
Input current		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		−17	–	+ 3	dB
Input current contrast control	for $V_{6-17} < 6$ V	I_7	–	0,5	15	μA
Input current when the peak-white limiter is active	$V_{6-17} = 2,5$ V	I_7	–	5,5	–	mA
Input resistance	$V_{6-17} > 6$ V	R_{7-17}	1,4	2,0	2,6	kΩ
Peaking of luminance signal						
Output impedance	pin 13	$\lvert Z_{13-17} \rvert$	–	200	–	Ω
Ratio of internal/external current when pin 13 is short-circuited			–	3	–	

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier						
Input signal amplitude (peak-to-peak value)	note 2 pin 3	$V_{3\text{-}17(p\text{-}p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3\text{-}17(p\text{-}p)}$	–	–	1,1	V
Minimum burst signal amplitude within the a.c.c. control range (peak-to-peak)			35	–	–	mV
A.C.C. control range			30	–	–	dB
Change of the burst signal at the output for the complete control range		ΔV	–	–	+ 1	dB
Input impedance	pin 3	$\lvert Z_{3\text{-}17}\rvert$	6	8	10	kΩ
Input capacitance	pin 3	$C_{3\text{-}17}$	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Input current saturation control	for $V_{5\text{-}17} > 6$ V	I_5	–	1	20	μA
Input impedance	$V_{5\text{-}17} = 6$ V to 10 V	$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance when the colour killer is active		$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance	for $V_{5\text{-}17} > 10$ V	$\lvert Z_{5\text{-}17}\rvert$	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB
Cross coupling between luminance and chrominance amplifier	note 4		–	–50	–46	dB
Reference part						
Phase locked loop						
Catching range		Δf	±400	±500	–	Hz
Phase shift for 400 Hz deviation of the carrier frequency		Δ	–	–	5	deg

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	$\Delta V_P = \pm 10\%$	Δf_{osc9}	–	150	250	Hz
Input resistance	pin 16	$R_{16\text{-}17}$	260	360	460	Ω
Input capacitance	pin 16	$C_{22\text{-}17}$	–	–	10	pF
A.C.C. generation						
Voltage at pin 4 nominal input signal		$V_{4\text{-}17}$	–	4,0	–	V
Voltage at pin 4 without burst input		$V_{4\text{-}17}$	–	1,9	–	V
Colour-off voltage		$V_{4\text{-}17}$	–	2,5	–	V
Colour-on voltage		$V_{4\text{-}17}$	–	2,8	–	V
Change in burst amplitude with temperature			–	0,1	–	%/K
Change in burst amplitude with 10% supply voltage change			–	0	–	%/V
Voltage at pin 2 at nominal input signal		$V_{2\text{-}17}$	–	5,0	–	V
Hue control						
Control voltage range			see Fig. 5			
Input current	for $V_{15\text{-}17} < 5$ V	I_{14}	–	0,5	20	μA
Input impedance	for $V_{15\text{-}17} > 5$ V	$\lvert Z_{14\text{-}17}\rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Ratio of demodulation signals (measured at the various outputs)	note 7					
(R-Y)/(B-Y); no (R-Y) signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	−0,42	–	
(R-Y)/(B-Y); colour bar signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	1,4	–	
(G-Y)/(R-Y); no (B-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,25	–	
(G-Y)/(B-Y); no (R-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,11	–	
Frequency response	0 to 0,7 MHz		–	–	−3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifier						
Output signal amplitude	at nominal luminance input signal and nominal contrast (peak-to-peak value) note 3 black-white	$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)	$V_{12-17(p-p)}$	–	3,8	–	V
Maximum peak-white level	note 6	$V_{10,11,12-7}$	9,0	9,3	9,6	V
Maximum output current		$I_{10,11,12-17}$	–	–	10	mA
Difference in the black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range			see Fig. 4			
Brightness control input current		I_9	–	–	–50	μA
Black level variation with temperature		V/T	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{b1}	1,95	2,15	2,35	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 5	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
RGB output impedance		$\lvert Z_{10,11,12-17} \rvert$	–	–	50	
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which the RGB blanking is activated		V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input currents	V_{7-17} = 0 to 1 V	I_7	–	–	–1	mA
	V_{7-17} = 1 to 8,5 V	I_7	–	–20	–40	μA
	V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Noted to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as maximum contrast –3 dB and nominal saturation as maximum saturation –10 dB.
4. Cross coupling is measured under the following condition:
   - input signals nominal;
   - contrast and saturation such that nominal output signals are obtained;
   - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
6. When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 7 (contrast control). Discharge current is 5,5 mA.
7. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

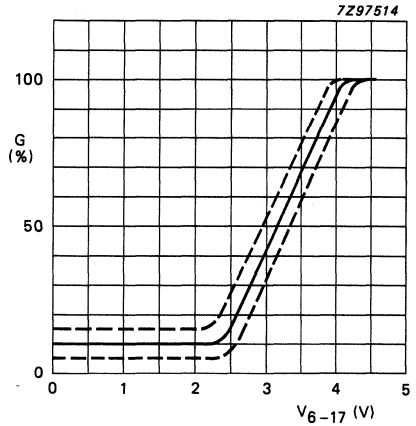


Fig. 2 Contrast control voltage range.

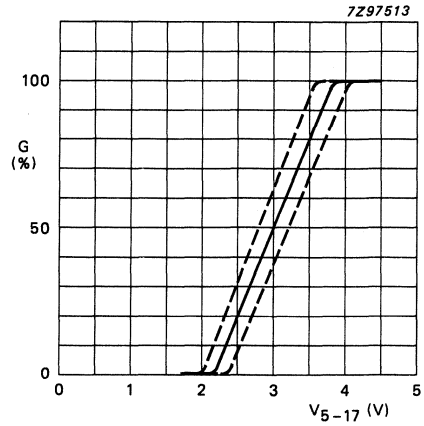


Fig. 3 Saturation control voltage range.

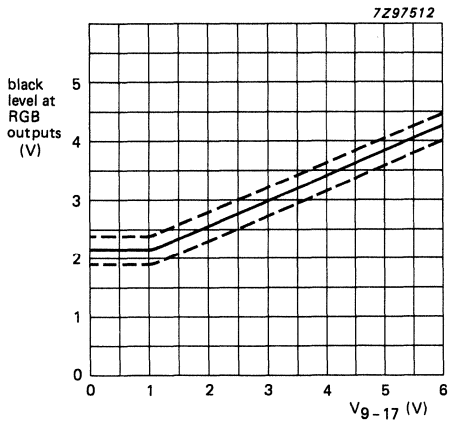


Fig. 4 Brightness control voltage range.

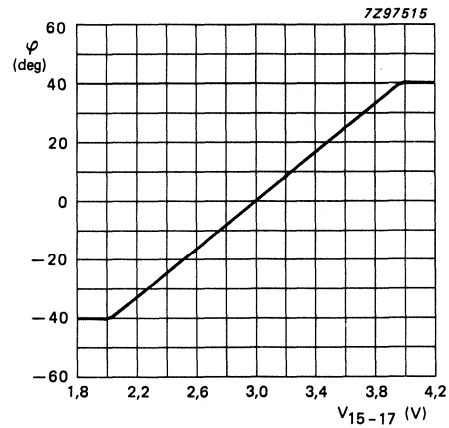


Fig. 5 Hue control voltage range.

APPLICATION INFORMATION

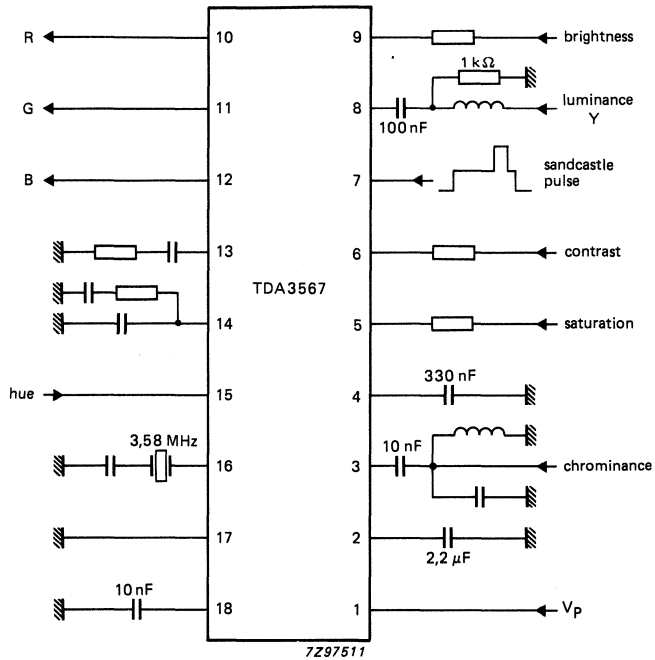


Fig. 6 Application diagram.

DEVELOPMENT DATA

NTSC DECODER WITH FAST RGB BLANKING

GENERAL DESCRIPTION

The TDA3569 NTSC decoder combines luminance amplifier, RGB matrix and RGB amplifiers to provide NTSC demodulation and direct drive of discrete output stages. A facility for fast blanking of the RGB outputs is included.

Features

- Automatic chrominance levelling (avoids saturation at chrominance input)
- Peaking circuit with d.c. control
- Fast RGB output blanking

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{1-19}$	10,8	12	13,2	V
Supply current		I_1	–	80	–	mA
Luminance input signal						
Input voltage (peak-to-peak value)		$V_{8-19(p-p)}$	–	450	–	mV
Contrast control range			–	−17 to +3	–	dB
Chrominance amplifier						
Input voltage (peak-to-peak value)		$V_{3-19(p-p)}$	–	550	–	mV
Saturation control range			50	–	–	dB
RGB matrix						
Output voltage (peak-to-peak value)	nominal luminance signal and nominal contrast (black-white)	$V_{12,13,14-19}$	4	5	6	V
Sandcastle input						
RGB slicing level		V_{7-19}	1,0	1,5	2,0	V
Burst gate/clamping pulse separation level		V_{7-19}	6,5	7,0	7,5	V

PACKAGE OUTLINE

20-lead DIL; plastic with internal heat-spreader (SOT146EE7).

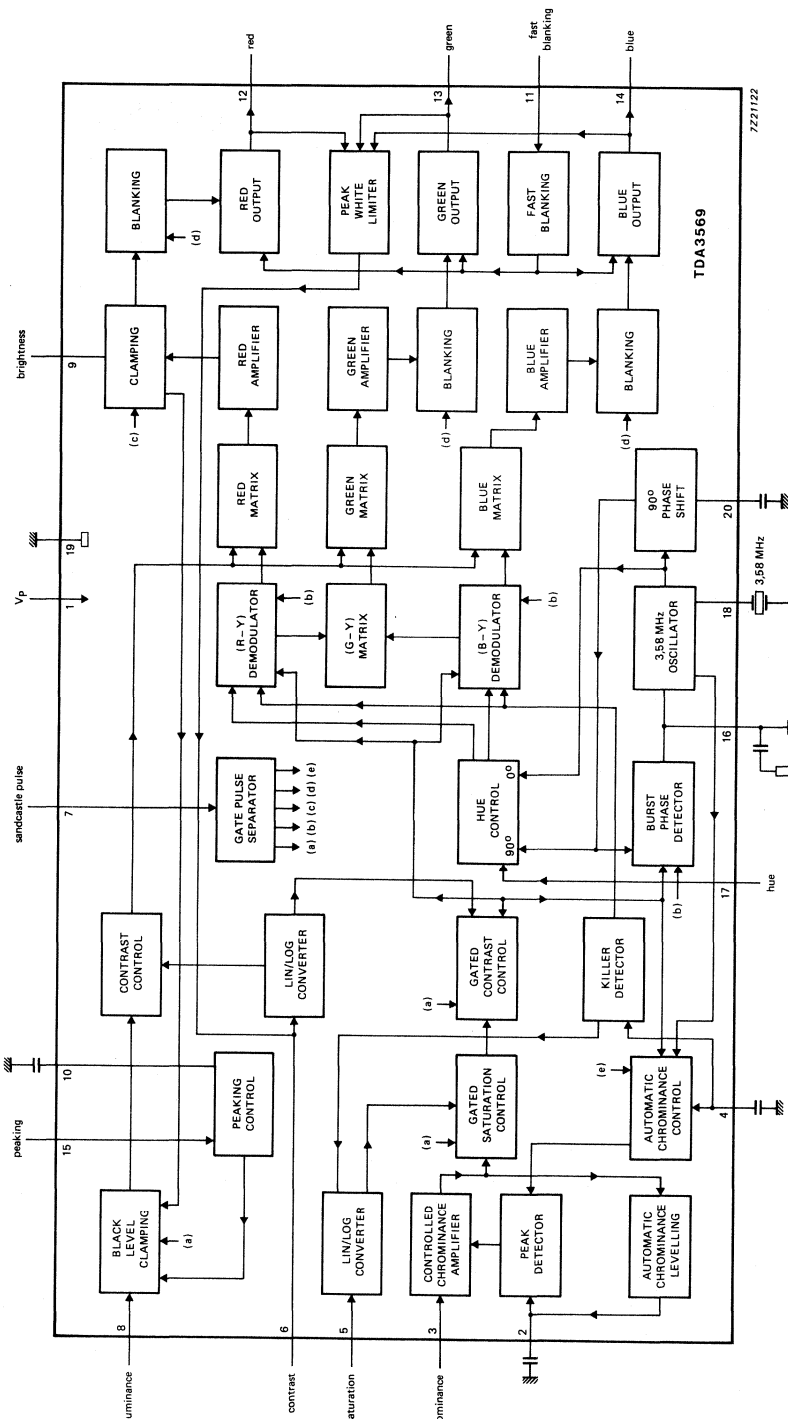


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires a positive video input signal of 450 mV peak-to-peak, a.c. coupled to pin 8. The coupling capacitor provides storage for the black level clamping circuit. After clamping the signal is fed to a peaking circuit in which the amount of overshoot is controlled from the voltage on pin 15.

Then next stage controls luminance signal contrast. Adjusted by the voltage on pin 6, the contrast control range is nominally −17 to +3 dB. The curve is linear as shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input and requires a.c. coupling to pin 3. The minimum peak-to-peak signal amplitude at the input is 55 mV (colour bar signal with 75% saturation; burst signal is 25 mV (peak-to-peak)). The gain control has a range greater than 30 dB but to avoid clipping, the input signal should not exceed 1,1 V (peak-to-peak).

After gain control, the chrominance signal is fed to an automatic chrominance levelling (ACL) circuit which avoids over-saturation when the incoming chrominance/burst ratio exceeds 2,2 : 1. The ACL circuit controls the chrominance amplitude via the automatic chrominance control (ACC) circuit.

The controlled chrominance signal is then fed to the saturation and contrast control stages. The chrominance and luminance contrast stages are directly coupled to ensure good tracking. Saturation is controlled via pin 5. This has a high impedance and a control range of 2 to 4 V, giving a linear saturation control greater than 50 dB. The burst signal is not affected by contrast or saturation controls.

After the amplification and control stages the chrominance signal is fed to the (R-Y) and (B-Y) demodulators, the burst phase detector and the ACC detector.

Oscillator and ACC circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal is connected between pin 18 and ground. The oscillator does not require adjustment due to the small spreads of the IC. To check the free running frequency of the oscillator the loop is opened by connecting the saturation control (pin 5) to the positive supply line. The oscillator has an internal gain-limiting stage which holds the gain at unity. This ensures internal signals remain sinusoidal thus preventing higher harmonics of subcarrier signals and allowing hue control to be obtained by mixing two signals with phases of 0^{o} and 90^{o}. The 90^{o} phase shift is obtained via a Miller integrator and the bias capacitor for this is connected at pin 20.

The ACC detector compares the burst signal with the 0^{o} reference signal. After detection, the ACC signal is fed via a peak detector to control the chrominance amplifier and to a sample-and-hold circuit to drive the colour killer circuit.

The reference signal for the burst phase detector is provided by the 90^{o} phase-shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing the 0^{o} and 90^{o} oscillator signals before they are fed to the (R-Y) and (B-Y) demodulators. This means that the hue control reacts to control voltage changes without delay as it is not dependent on the PLL.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals being from the hue control circuit. With nominal hue control, the phase angle of the (R-Y) reference signal is 0^{o} and that for the (B-Y) reference signal is 90^{o}.

For flesh tone correction the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$

$(G\text{-}Y)_{matrixed} = -0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$

$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes when the chrominance signal is demodulated with a phase difference of 90^{o} between the R-Y and B-Y demodulators and gain ratio B-Y/R-Y = 1,78 : 1.

RGB matrix and amplifier circuits

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst/chrominance ratio of the input = 1 : 2,2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak).

The black level of the red channel is compared with a variable external reference level (pin 9) which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level, therefore the green and blue outputs follow any variation of the red output. The output of the black level control can be varied between 2 V and 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal approaches the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

The circuit also has a fast blanking input (pin 11) which blanks the RGB outputs within 50 ns.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 1)		$V_P = V_{1-19}$	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	−25	+150	°C
Operating ambient temperature range		T_{amb}	−25	+65	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 50 K/W

CHARACTERISTICS

$V_P = V_{1-19} = 12$ V; $T_{amb} = 25$ °C; all voltages refer to pin 19; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 1)		$V_P = V_1$	10,8	12	13,2	V
Supply current		I_1	–	80	–	mA
Total power dissipation		P_{tot}	–	0.96	–	W
Luminance input signal						
Input voltage (pin 8) (peak-to-peak value)	note 1	$V_{8(p\text{-}p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_8	–	–	1	V
Input current (pin 8)		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		–	−17 to +3	–	dB
Contrast control input current (pin 6)	$V_6 < 6$ V	I_6	–	0,5	15	μA
	peak white limiter active, $V_6 = 2{,}5$ V	I_6	–	7	–	mA
Input resistance (pin 6)	$V_6 > 6$ V	R_6	1,4	2,0	2,6	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Peaking of luminance signal						
Input impedance (pin 15)		$\|Z_{10}\|$	–	10	–	kΩ
Output impedance (pin 10)		$\|Z_{15}\|$	–	75	–	Ω
Ratio of internal/ external current	pin 10 AC short-circuit to ground		–	10	–	
Chrominance amplifier						
Input signal amplitude (peak-to-peak value) (pin 3)	note 2	$V_{3(p\text{-}p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3(p\text{-}p)}$	–	–	1,1	V
Minimum burst signal amplitude within the ACC control range (peak-to-peak value)			35	–	–	mV
ACC control range			30	–	–	dB
Change of the colour signal at the output for the complete control range		ΔV	–	–	+ 2	dB
Input impedance (pin 3)		$\|Z_3\|$	6	8	10	kΩ
Input capacitance (pin 3)		C_3	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Saturation control input current (pin 5)	$V_5 < 6$ V	I_5	–	1	20	μA
Input impedance (pin 5)	$V_5 = 6$ to 10 V	$\|Z_5\|$	1,5	2,1	2,7	kΩ
	colour killer active	$\|Z_5\|$	1,5	2,1	2,7	kΩ
	$V_5 > 10$ V	$\|Z_5\|$	0,7	1,0	1,5	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
ACL circuit						
Chrominance/burst ratio at which ACL commences	note 3		–	2,2	–	
Reference part						
Phase-locked loop						
Catching range		Δf	± 400	± 500	–	Hz
Phase shift for 400 Hz carrier frequency deviation		$\Delta\phi$	–	–	5	deg
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	ΔV_P = ± 10%	Δf_{osc}	–	150	250	Hz
Input resistance (pin 18)		R_{18}	260	360	460	Ω
Input capacitance (pin 18)		C_{18}	–	–	10	pF
ACC generation						
Voltage at pin 4 with nominal input signal		V_4	–	5,8	–	V
Voltage at pin 4 without burst input		V_4	–	2	–	V
Colour-off voltage (pin 4)		V_4	–	3,1	–	V
Δ colour-off-colour-on		ΔV_4	100	300	500	mV
Voltage at pin 2 with nominal input signal		V_2	5,2	5,8	6,4	V
Hue control						
Control voltage range	see Fig. 5					
Input current (pin 17)	$V_{17} < 5$ V	I_{17}	–	0,5	20	μA
Input impedance (pin 17)	$V_{15} > 5$ V	$\lvert Z_{17}\rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Demodulation signal ratios	note 4					
(R-Y)/(B-Y)	no (R-Y)	V_{12}/V_{14}	–	–0,42	–	
(R-Y)/(B-Y)	colour bar	V_{12}/V_{14}	–	1,4	–	
(G-Y)/(R-Y)	no (B-Y)	V_{13}/V_{14}	–	–0,25	–	
(G-Y)/(B-Y)	no (R-Y)	V_{13}/V_{14}	–	–0,11	–	
Frequency response	0 to 0,7 MHz		–	–	–3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers						
Output signal amplitude (peak-to-peak value) (pins 12, 13 and 14)	with nominal luminance input and nominal contrast; note 5; black-white	$V_{12,13,14(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel; (B-Y) signal (pin 14) (peak-to-peak value)	with nominal contrast and saturation; no luminance input	$V_{14(p-p)}$	–	3,8	–	V
Maximum peak-white level (pins 12, 13 and 14)	note 6	$V_{12,13,14}$	9,0	9,3	9,6	V
Available output current (pins 12, 13 and 14)	per pin	$I_{12,13,14}$	10	–	–	mA
Difference in black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range	see Fig. 4					
Brightness control input current (pin 9)		$-I_9$	–	–	50	μA
Black level variation with temperature		$\Delta V/\Delta T$	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{bl}	1,95	2,15	2,35	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 7	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
RGB output impedances		$\lvert Z_{10,11,12} \rvert$	–	–	50	Ω
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which RGB blanking is activated		V_7	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_7	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input current (pin 7)	V_7 = 0 to 1 V	I_7	–	–	–1	mA
	V_7 = 1 to 8,5 V	I_7	–	–20	–40	μA
	V_7 = 8,5 to 12 V	I_7	–	–	2	mA
Fast blanking						
Level at which fast blanking is activated		V_{11}	–	2	–	V
Allowable voltage at blanking input		V_{11}			5	V
Delay between fast blanking input and output		t_d			50	ns

Notes to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Signal amplitude indicated is for colour bar with 75% saturation, thus the chrominance/burst ratio is 2,2 : 1.
3. The ACL circuit limits the chrominance signal to a particular value as soon as the chrominance/burst ratio exceeds 2,2 : 1. Limiting is performed via the ACC function.
4. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the 'FUNCTIONAL DESCRIPTION'.
5. Nominal contrast is specified as maximum contrast −3 dB; nominal satuarion is specified as maximum saturation −10 dB.
6. When this level is exceeded, the amplitude of the output signal is reduced with a discharge of the capacitor on pin 7 (contrast control), the discharge current is 7 mA.
7. The signal-to-noise ratio is specified as peak-to-peak signal amplitude with respect to the r.m.s. value of noise.

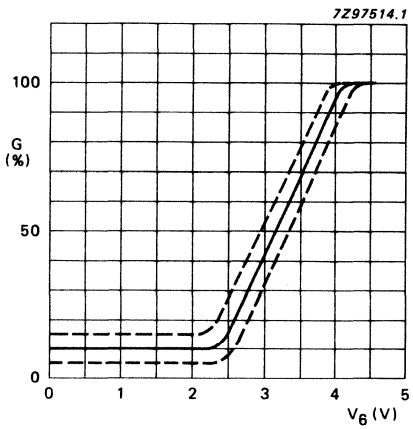


Fig. 2 Contrast control voltage range.

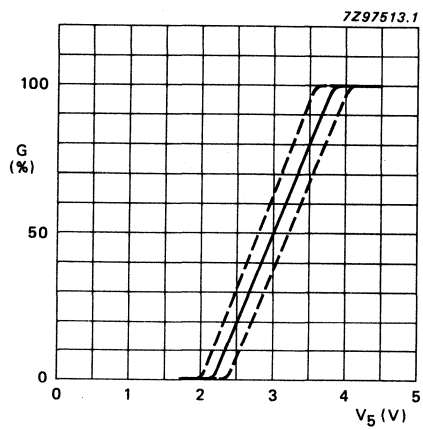


Fig. 3 Saturation control voltage range.

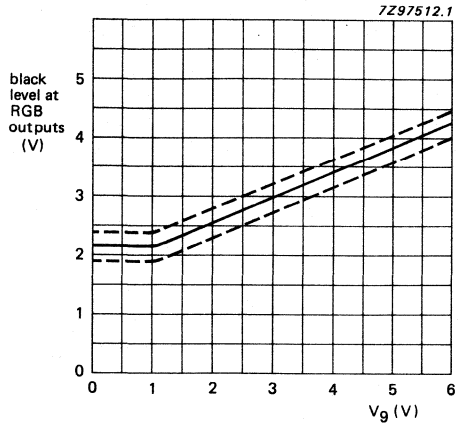


Fig. 4 Brightness control voltage range.

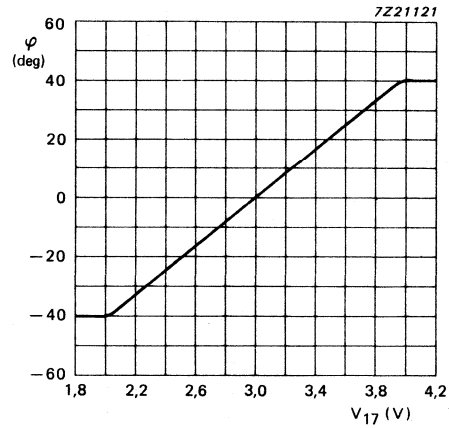


Fig. 5 Hue control voltage range.

DEVELOPMENT DATA

APPLICATION INFORMATION

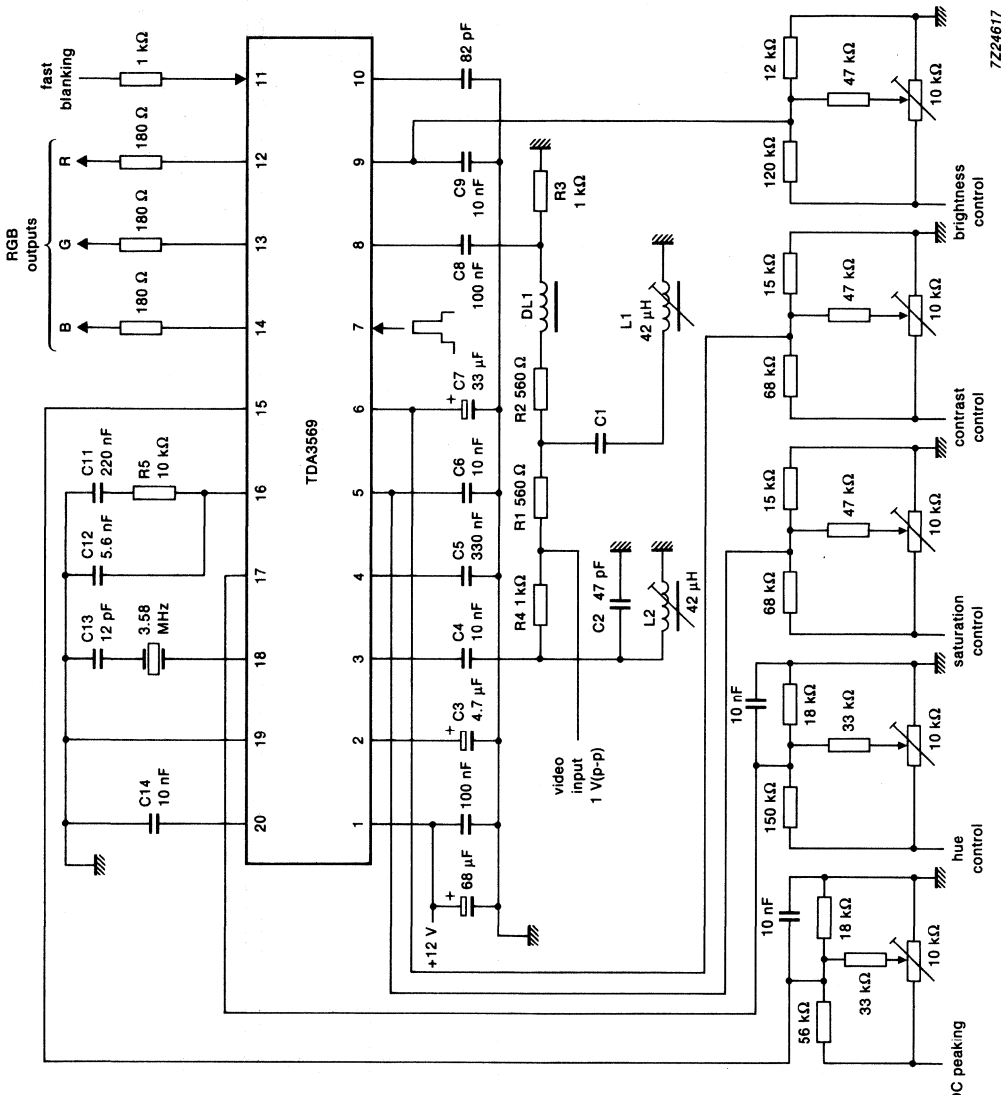


Fig. 6 Application diagram.

SECAM PROCESSOR CIRCUIT

GENERAL DESCRIPTION

The TDA3590A processor circuit converts SECAM signals into sequential phase-modulated (quasi-PAL) signals. It combines all the functions of the TDA3590, TDA3591 and TDA3591A to provide a complete SECAM processor system. The circuit is intended for use in conjunction with TDA3560, TDA3561, TDA3561A, TDA3562A or TDA3566 to provide SECAM/PAL/NTSC/black-and-white processor combinations.

Features

- Limiter/amplifier for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to convert colour difference signals into sequential, phase-modulated signals
- Identification circuit for horizontal, vertical or combined horizontal and vertical SECAM identification
- Divider circuit to provide 4,4 MHz carrier from 8,8 MHz signals generated in TDA3560/61/61A/62A/66
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier
- Pin compatibility with TDA3590, TDA3591 and TDA3591A when application requires SECAM ident priority (does not apply with PAL ident priority)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17-2}$	typ.	12 V
Supply current	$I_P = I_{17}$	typ.	100 mA
Chrominance amplifier and demodulator			
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	550 mV
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	100 mV
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1,2$ V	$V_{8-2(p-p)}$	typ.	900 mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	typ.	500 mV
Identification			
Input voltage range for horizontal identification (pin 5)	V_{5-2}		0 to 8 V
Input voltage range for vertical identification (pin 5)	V_{5-2}		10,5 to 12,0 V
Voltage at pin 6 for PAL	V_{6-2}	typ.	10,2 V
Voltage at pin 6 for SECAM	V_{6-2}	typ.	7,0 V
Sandcastle pulse detector			
Vertical blanking level	V_{19-2}	typ.	1,5 V
Horizontal blanking level	V_{19-2}	typ.	3,5 V
Burst gating level	V_{19-2}	typ.	7,2 V
Luminance amplifier			
Luminance input signal (peak-to-peak value)	$V_{16-2(p-p)}$	typ.	1,2 V
Luminance output signal (peak-to-peak value)	$V_{15-2(p-p)}$	typ.	3,0 V
PAL matrix and SECAM switch			
Burst signal amplitude (peak-to-peak value)	$V_{11;12-2(p-p)}$	typ.	60 mV
Amplification for PAL		typ.	0,5 dB
Amplification for SECAM		typ.	6 dB

PACKAGE OUTLINE

24-lead DIL; plastic (with internal heat spreader) (SOT101B).

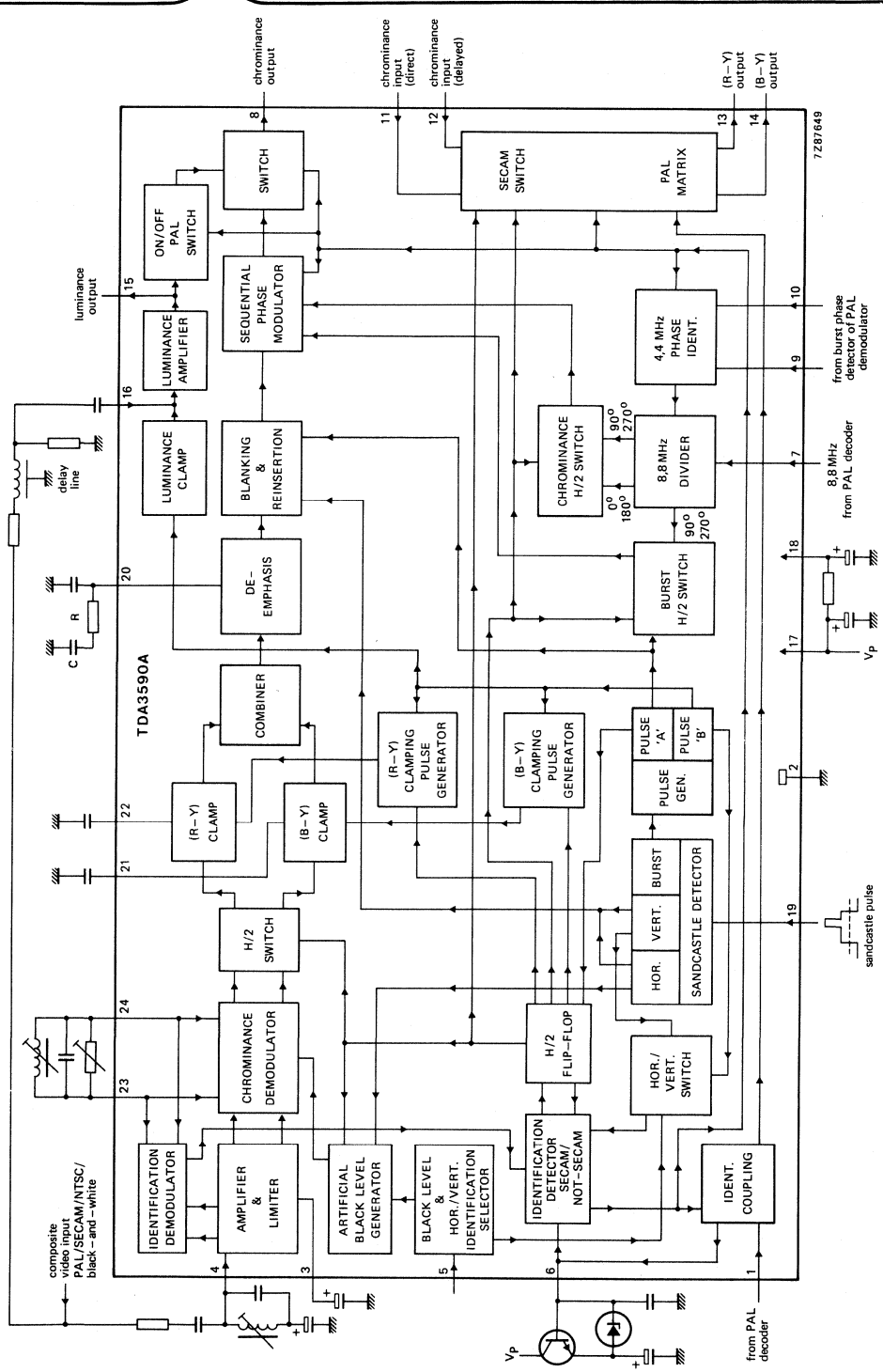


Fig. 1 Block diagram.

PINNING

1. Identification coupling input for PAL/not-PAL identification using half the saturation voltage of the PAL decoder.
2. Ground.
3. Limiter feedback.
4. SECAM video input.
5. Identification selection input using a d.c. level to preset the identification mode of horizontal/vertical detection + black level clamping/insertion.
6. Storage circuit input to SECAM/not-SECAM identification detector.
7. Divider circuit input of 8,8 MHz from the PAL decoder.
8. Chrominance signal output comprising PAL or processed SECAM (quasi-PAL).
9. Carrier signal phase identification input from the burst phase detector of the PAL decoder.
10. As for pin 9.
11. Direct chrominance input to SECAM switch/PAL matrix.
12. Delayed chrominance input to SECAM switch/PAL matrix.
13. Colour difference output (R-Y).
14. Colour difference output (B-Y).
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection.
21. Storage capacitor connection for (B-Y) clamp.
22. Storage capacitor connection for (R-Y) clamp.
23. Connection for reference tuned circuit for SECAM chrominance and identification demodulators.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3590A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or not-SECAM.

When the incoming signals are not-SECAM (PAL/NTSC/black-and-white) they are diverted via pin 16 to the chrominance output at pin 8 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM processor circuitry. When SECAM signals are received the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 4 via an external bell filter. The signals are amplified, limited and then demodulated. The limiters give optimum i.f. interference suppression. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R-Y) and (B-Y) clamp is determined by the last 1,45 μs of the burst gate pulse.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits.

The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78. The external de-emphasis components of R = 1 kΩ and C = 470 pF give a spread at the internal de-emphasis network $< 20\%$.

FUNCTIONAL DESCRIPTION (continued)

If artificial black level reinsertion is required the burst gating pulse (Fig. 2) is used to time black level clamping. Artificial black levels are inserted during the horizontal blanking period when $V_{5\text{-}2} > 2$ V. The clamp circuits then react to the artificial levels instead of the demodulated burst signals (this is necessary when no horizontal burst signals are available). The inserted signals may not be identical to the demodulated signals because of circuitry spread but this can be corrected by detuning the demodulator reference tuned circuit.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the sequential phase modulator. The nominal duration of this burst is 2,85 μs which approximates to the duration of the PAL burst and, in combination with the horizontal blanking pulse (used as keying pulse in the SECAM switch), minimizes interference in the a.c.c. loop of the TDA3560/61/62.

At the input to the modulator the (R-Y) and (B-Y) signals have a positive phase position for magenta colour. The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; the burst is modulated in the + (R-Y) direction and is only present during an (R-Y) line, the modulated (R-Y) component has the same phase position as the (R-Y) burst for magenta colour.

The chrominance output from pin 8, in the SECAM mode, is a quasi-PAL signal with alternate line, sequential modulation. Odd and even harmonics of the 4,4 MHz carrier introduced by the modulator are suppressed by internal filters. A correction is made to the burst-chrominance ratio of the quasi-PAL signals for equal saturation of PAL and SECAM signals.

Identification

Identification of the SECAM signal is performed using the fact that only SECAM has a line-to-line difference in demodulated voltage level. This is detected during the last 1,5 μs of the burst gate pulse. A flip-flop, which is switched by the leading edge of the sandcastle time blanking pulse, provides the reference input to the identification detector. Here the phase of the flip-flop is compared with that of the changing voltage levels from the demodulator. The SECAM identification circuits operate when selected by the voltage on pin 5; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 5. An internal voltage divider presets pin 5 to 6 V to give automatic selection of horizontal identification plus black level re-insertion. Vertical identification is selected by taking the voltage on pin 5 above 10,5 V, then the system compares the demodulator output voltage only during line scanning of the vertical blanking.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Luminance amplification

The luminance amplifier input at pin 16 can be up to 1,2 V (peak-to-peak value) which equates to a peak-to-peak voltage of 2,7 V −7 dB. The amplifier gain is typically 8 dB. The luminance clamping circuit is activated during the SECAM identification timing (see Fig. 2).

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detected burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL burst modulator. Pulse 'B' provides the timing of the (R-Y) clamp (present only during a red line); the (B-Y) clamp (present only during a blue line); the luminance clamp (present every line); and the SECAM horizontal identification circuit.

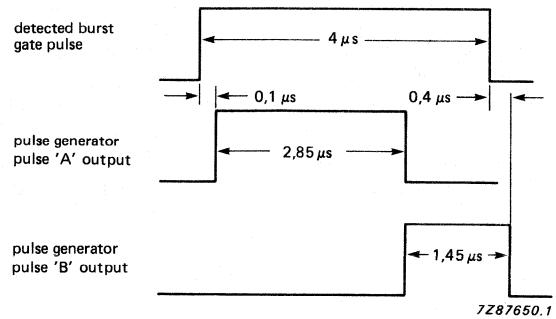


Fig. 2 Burst gate timing pulse generation.

PAL matrix and SECAM switch

The PAL matrix and SECAM switch is included in the TDA3590A to facilitate handling of the two chrominance signal types, PAL and SECAM. For PAL, the direct chrominance signal and the chrominance signal delayed by the PAL delay line are used by the PAL matrix to separate the two colour difference signals. Phase accuracy is not critical for this operation as the colour difference signals are not mixed. For SECAM, the quasi-PAL sequential colour difference signals are separated by switching. The gain of the switching circuit is two times that for normal PAL reception to maintain signal balance between the two systems. The (B-Y) output from the SECAM switch is a signal with no burst; the (R-Y) output has a burst modulated in the + (R-Y) direction during the + (R-Y) line. There is minimal crosstalk between the colour difference signals in the SECAM switch.

Carrier generation

The carrier for the sequential phase modulator is obtained using the 8,8 MHz input from the PAL decoder. This input is divided by two to provide two 4,4 MHz signals with a phase relationship of 90°. Correct phasing between the 4,4 MHz and the PAL decoder is ensured by the 4,4 MHz phase identifier circuit which resets the divider if the phasing is wrong (see Figs 3 and 4 for inter-connections). The inputs/outputs to the phase identifier have internal current sources in the case of SECAM.

Coupling of identification systems

Coupling of system identification between TDA3590A and a PAL decoder is performed using the functions of pins 1 and 6. The voltage level at pin 1 is controlled by the PAL/not-PAL detection of the PAL decoder; the voltage level at pin 6 is a function of SECAM/not-SECAM detection of the TDA3590A modified by the action of pin 6 external circuit.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V) by the external circuit. This corresponds to the not-SECAM mode of the TDA3590A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3590A when it recognizes the signal as not-SECAM. An internal current source keeps pin 6 voltage high, locking the TDA3590A in the not-SECAM mode. This condition is maintained even if reflected PAL signals are present. The PAL decoder recognizes the signal as PAL and takes pin 1 of TDA3590A to a voltage of between 0,5 and 2,6 V, depending on the setting of the saturation voltage. The system is thus locked in the PAL mode.

FUNCTIONAL DESCRIPTION (continued)

SECAM

The initial high voltage level (± 10,2 V) at pin 6 caused by channel switching sets the TDA3590A in the not-SECAM mode and during this time the PAL decoder detects a not-PAL signal. This causes a voltage at pin 1 of $< 0{,}4$ V which prevents the internal current source of TDA3590A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3590A to detect SECAM. The initiation of SECAM detection is delayed by the action of pin 6 external circuit and commences when pin 6 approaches 9,1 V. The SECAM signals are converted by TDA3590A to quasi-PAL signals at pin 8 which are detected by the PAL decoder as PAL signals. The resulting modes of operation are SECAM for the TDA3590A and PAL for the PAL decoder, together giving a system operation in the SECAM mode.

Black-and-white

The TDA3590A is initially set in the not-SECAM mode as previously described. The PAL decoder detects not-PAL and the TDA3590A detects not-SECAM which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3590A mode	PAL decoder mode	system operating mode
SECAM	PAL	SECAM
SECAM	not-PAL	condition not used
not-SECAM	PAL	PAL
not-SECAM	not-PAL	black-and-white

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17\text{-}2}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,88 W
Operating ambient temperature range	T_{amb}	−25	to + 65 °C
Storage temperature range	T_{stg}	−25	to + 150 °C

CHARACTERISTICS

$V_P = V_{17-2} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified. The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range (pin 17)	V_{17-2}	10,8	12,0	13,2	V
Supply current (pin 17)	I_{17}	–	100	–	mA
Input current (pin 18)	I_{18}	–	–	170	μA
Total power dissipation	P_{tot}	–	1,2	–	W
Chrominance amplifier and demodulator					
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	–	–	1,1	V
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	15	100	300	mV
Input resistance (pin 4)	R_{4-2}	–	10	–	kΩ
Input capacitance (pin 4)	C_{4-2}	–	–	5	pF
(R-Y)/(B-Y) ratio before modulation (pin 20)		–	1,78	–	
Relative black level deviation of colour difference signals before modulation (note 2)					
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1,2$ V	$V_{8-2(p-p)}$	–	900	–	mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	–	500	–	mV
Output impedance	$\lvert Z_{8-2} \rvert$	–	50	–	Ω
Input voltage for clamping on back porch of colour difference signals	V_{5-2}	–	–	0,5	V
Input voltage for artificial black level insertion after demodulation	V_{5-2}	2	–	–	V
Input resistance between pins 23 and 24	R_{23-24}	–	4	–	kΩ
Input capacitance between pins 23 and 24	C_{23-24}	–	15	–	pF
Linearity of (B-Y) signal (pin 8) (note 3)		85	92	–	%
Linearity of (R-Y) signal (pin 8) (note 4)		93	100	–	%
Input resistance (pin 5)	R_{5-2}	–	10	–	kΩ
Chrominance demodulator zero point stability (pin 20) (note 5)	f_0	–	5	–	kHz
Offset (B-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−15	–	kHz
Offset (R-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−25	–	kHz

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification SECAM/not-SECAM					
Input voltage range for horizontal identification (pin 5)	V_{5-2}	0	–	8	V
Input voltage range for vertical identification (pin 5)	V_{5-2}	10,5	–	V_P	V
Voltage at pin 6 for PAL	V_{6-2}	–	10,2	–	V
Voltage at pin 6 for SECAM	V_{6-2}	–	7,0	–	V
Identification ON for SECAM	V_{6-2}	–	10,6	–	V
Colour OFF for SECAM	V_{6-2}	–	9,7	–	V
Colour ON for SECAM	V_{6-2}	–	9,0	–	V
Voltage at pins 9 and 10 for SECAM	$V_{9-2;\ 10-12}$	–	10,5	–	V
Voltage between pins 9 and 10 for SECAM	V_{9-10}	–	–	3	mV
Permissible voltage range at pins 9 and 10 for PAL	$V_{9-2;\ 10-2}$	6,8	–	10,2	V
Sandcastle pulse detector and clamping pulse generator					
Voltage level at which the vertical blanking pulse is separated	V_{19-2}	1,0	1,5	2,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	2,1	–	2,9	V
Voltage level at which the horizontal blanking pulse is separated	V_{19-2}	3,0	3,5	4,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	4,1	–	6,6	V
Voltage level at which the burst gating pulse is separated	V_{19-2}	6,7	7,2	7,7	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	7,8	–	V_P	V
Input current at $V_{19-2} = 7$ V	I_{19}	–	–	40	μA
Carrier generator (note 6)					
Input signal from TDA3560/61/61A/62A/66 (peak-to-peak value)	$V_{7-2(p-p)}$	150	–	–	mV
Input resistance	R_{7-2}	–	4	–	kΩ
Input capacitance	C_{7-2}	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
Luminance amplifier					
Input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	1,2	1,7	V
Chrominance input signal when no luminance information is present (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	–	1	V
Gain (pin 16 to 15) at f_{16} = 4,4 MHz	$G_{16\text{-}15}$	–	8	–	dB
Input current (pin 16)	I_{16}	–	–	1	μA
Input resistance during clamping (pin 16)	$R_{16\text{-}2}$	–	2,9	–	kΩ
Output impedance (pin 15) at I_{15} = 2 mA	$\lvert Z_{15\text{-}2}\rvert$	–	20	–	Ω
Frequency response at –3 dB (pin 16 to 15)	f	6	–	–	MHz
Gain (pin 16 to 8) at f_{16} = 4,4 MHz; not-SECAM condition	$G_{16\text{-}8}$	–	7	–	dB
Frequency response at –3 dB (pin 16 to 8) not-SECAM condition	f	–	5	–	MHz
PAL matrix and SECAM switch					
Burst signal amplitude (peak-to-peak value)	$V_{11;\,12(p\text{-}p)}$	–	60	–	mV
Input resistance	$R_{11;\,12\text{-}2}$	–	900	–	Ω
Input capacitance	$C_{11;\,12\text{-}2}$	–	3	–	pF
Amplification for PAL	A	–	0,5	–	dB
Amplification for SECAM	A	–	6	–	dB
Difference in amplification from inputs to one output for PAL	ΔA	–	–	0,5	dB
Line-to-line phase error in (R-Y) output for zero error in (B-Y) output for PAL		–	–	3,5	deg
Output impedance	$\lvert Z_{13;\,14\text{-}2}\rvert$	–	50	–	Ω
Identification PAL/not-PAL					
Input condition for PAL (pin 1)	$V_{1\text{-}2}$	0,8	–	2,1	V
Input conditions for not-PAL (pin 1): lower voltage level	$V_{1\text{-}2}$	–	–	$<0,4$	V
upper voltage level	$V_{1\text{-}2}$	$>2,6$	–	V_P	V

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 4 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 8 to the PAL decoder is minimum during scan (PAL black colour information).
2. When an artificial black level is inserted after demodulation the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of 0%.
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz; $V_{5\text{-}2}$ = 2,0 V.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz; $V_{5\text{-}2}$ = 2,0 V.
5. When the input signal to the limiter (pin 4) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz.
6. The phase delay between the oscillator output of TDA3560/61/61A/62A/66 and the input to TDA3590A pin 7 must be adjusted for minimum burst amplitude at pin 28 of the PAL decoder.

APPLICATION INFORMATION

The pin-to-pin functions of the application shown in Fig. 3 are described against the corresponding pin numbers.

Pin 4. Chrominance input

Typical input signal values (peak-to-peak) are: SECAM 100 mV; PAL 0,55 V. The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which has the bell-shaped bandpass required for SECAM signals.

Pin 5. Horizontal/vertical identification

Selection of horizontal or vertical identification depends on the external voltage applied to pin 5. When the d.c. level on pin 5 changes with time (pulse information) a combination of horizontal and vertical identification is possible.

Horizontal identification

When the voltage at pin 5 is $< 0,5$ V horizontal identification and black level clamping occur. The clamping is during the back porch of the colour difference signals. If artificial black level insertion is required the voltage at pin 5 should be between 2 and 8 V.

Vertical identification

When the voltage on pin 5 is $> 10,5$ V vertical identification occurs (identification on 9 lines in the vertical blanking period). In this mode the black level is artificially inserted after demodulation.

Pin 6. System identification

During PAL reception the typical voltage at pin 6 is 10,2 V. This causes the luminance stage to be connected internally to the chrominance output at pin 8 and also activates the PAL matrix for normal PAL signals. During SECAM reception the typical voltage at pin 6 is 7 V. This changes the internal connection of the output from the luminance stage to the sequential phase modulator and enables the SECAM switch. Noisy SECAM signals cause the voltage at pin 6 to increase, colour killing occurs at 9,8 V and colour is reinstated at 9.1 V.

Pin 7. Carrier generation

An 8,8 MHz signal from the PAL decoder is applied via pin 7 to the divider circuit in the TDA3590A. From this two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The delay of the 8,8 MHz input must be adjusted for minimum burst amplitude of the chrominance signal at pin 28 of the PAL decoder. With this condition the burst generated by the TDA3590A is in phase with the (R-Y) reference signal for the PAL decoder demodulator (the a.c.c. of the PAL decoder operates in the + (R-Y) direction).

Pin 8. Chrominance output

During PAL reception this output is connected internally to the luminance stage and a composite PAL video signal is present at pin 8. During SECAM reception the sequential phase modulator is connected to this output to give a quasi-PAL signal from pin 8. Typical peak-to-peak amplitudes of the signal from pin 8 are 900 mV for PAL (with peak-to-peak input at pin 16 of 1,2 V) and 500 mV for SECAM. The output signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier input of the PAL decoder.

Pins 9 and 10. Divider resetting

The output of the PAL decoder burst phase detector is connected to pins 9 and 10 of TDA3590A. During SECAM reception this signal carries differential a.c. current information about the phase relationship of the 4,4 MHz dividers of both ICs. The TDA3590A generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,5 V. This overrules the PAL decoder oscillator control function causing the oscillator to run at 2 x 4,43 MHz.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

The PAL matrix circuit is enabled by system identification of PAL reception. The signal inputs to the matrix are the (direct) a.c.c. composite video output from the PAL decoder via an attenuator to pin 11 and a delayed version of the same signal via a glass delay line to pin 12. Active matrixing takes place in the IC and the separated (R-Y) and (B-Y) signals are available at pins 13 and 14 respectively.

The SECAM switch circuit is selected by system identification of SECAM reception. The inputs to the SECAM switch are the sequentially modulated quasi-PAL signals, direct and delayed, to pins 11 and 12 respectively. The SECAM switch separates the (R-Y) and (B-Y) signals which are then available at pins 13 and 14 respectively.

Pins 15 and 16. Luminance signals

The maximum peak-to-peak amplitude of the input to pin 16 should be 1,7 V. The relatively high input impedance of the luminance amplifier allows a 22 nF coupling capacitor to be used. The luminance amplifier has internal input clamping and a gain of 8 dB. The output is available at pin 15.

During SECAM reception the luminance signal is delayed approximately 470 ns by an external delay line to equalize the SECAM processing delay. The luminance and chrominance outputs are then correctly timed.

During PAL reception the PAL composite video signal passes through the external delay line and, after amplification, is available at pins 15 and 8.

APPLICATION INFORMATION (continued)

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply voltage range of 10,8 to 13,2 V. The typical power dissipation of the IC at 12 V is 1,2 W.

Pins 17 and 18 are separated by an external RC filter. Pin 18 supplies all the output stages and the biasing for several current sinks in the IC. Separation of the supply voltages minimizes crosstalk between the various parts of the IC. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) to avoid the possibility of internal damage to the IC by discharge current should pin 17 be short-circuited to ground.

Pin 19. Sandcastle pulse

The required three-level sandcastle pulse may be coupled directly to the sandcastle pulse detector input at pin 19. The horizontal blanking, vertical blanking and burst gate pulses are separated by the IC.

Pin 20. De-emphasis

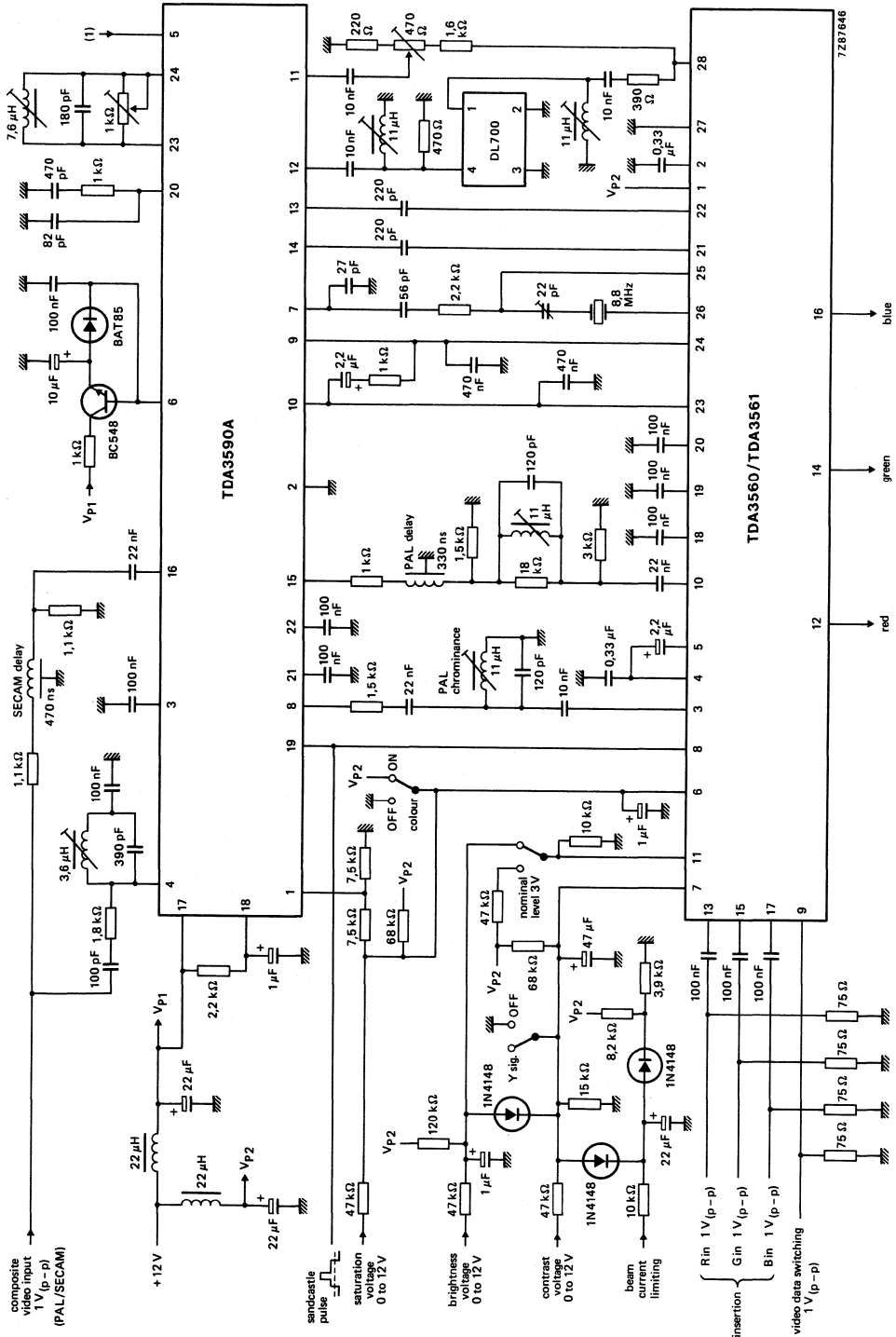
De-emphasis is performed at this pin with a 1 kΩ resistor and a 470 pF capacitor. Additional filtering of the 8,8 MHz signal using an 82 pF coupling capacitor prevents moiré patterns appearing on the screen.

Pins 21 and 22. Clamping of (R-Y) and (B-Y) signals

Clamping of the colour difference signals is performed after they have been separated. The normal value for the clamping storage capacitors is 100 nF but this may be increased to 470 nF if required.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via a bell filter and a limiter amplifier. Only one chrominance demodulator is used because of the sequential nature of the signal. The reference signal from the tuned circuit is applied to pins 23 and 24. Tuning and damping adjustments of the reference tuned circuit should be performed at $V_{5\text{-}2} > 2$ V (SECAM video (R-Y) (B-Y) information switched off). Adjustments should be such that minimum modulator voltage appears at pin 8, then any deviations between the black levels (when clamping on the back porch and when an artificial black level is filled in) can be made minimum.



(1) See Application Information for pin 5 — horizontal/vertical identification.

Fig. 3 PAL/SECAM decoder application.

APPLICATION INFORMATION (continued)

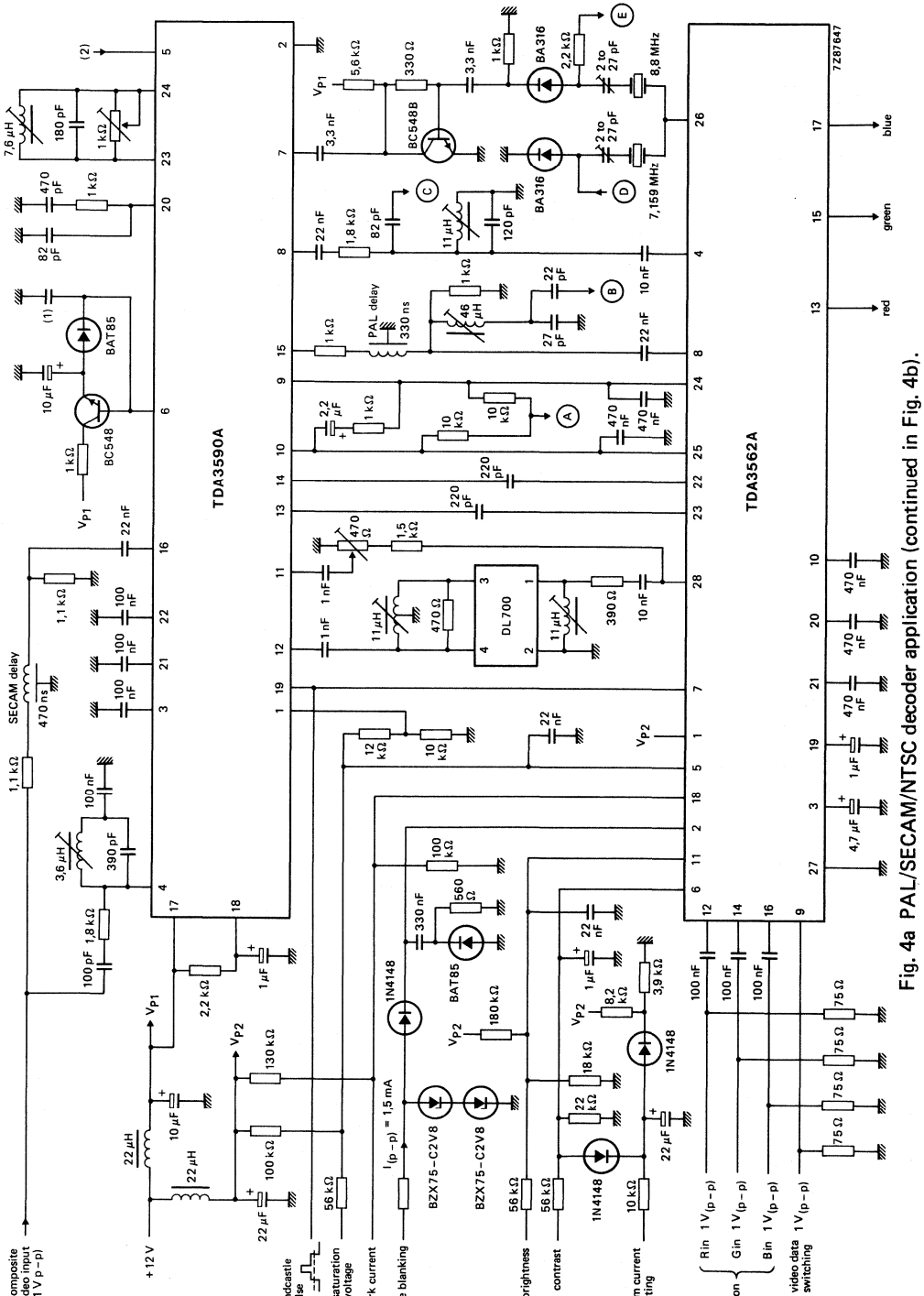
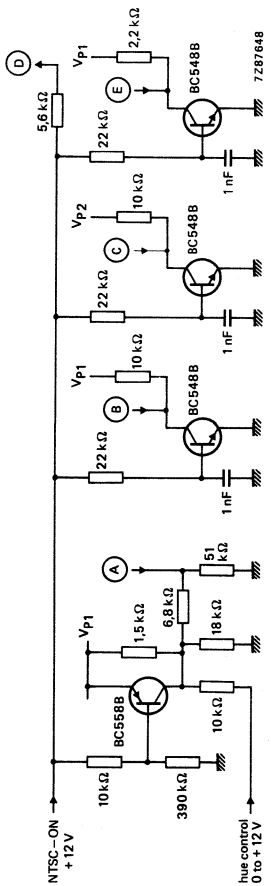


Fig. 4a PAL/SECAM/NTSC decoder application (continued in Fig. 4b).



(1) Capacitor value = 100 nF for horizontal identification or 1 μF for vertical identification.
(2) See Application Information for pin 5 – horizontal/vertical identification.

Fig. 4b PAL/SECAM/NTSC decoder application (continued from Fig. 4a).

SECAM-PAL TRANSCODER

GENERAL DESCRIPTION

The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V: SECAM processing shuts down but $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9-1(p-p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		V_{4-1}	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		V_{4-1}	0	–	2,9	V
Identification at pin 6		V_{6-1}	–	10,6	–	V
Slicing level reference voltage (pin 5)		V_{5-1}	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		V_{19-1}	–	1,5	–	V
Horizontal blanking level		V_{19-1}	–	3,5	–	V
Burst gating level		V_{19-1}	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16-1(p-p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		G_{16-15}	–	7,0	–	dB

PACKAGE OUTLINE

24-lead DIL; plastic with heat spreader (SOT-101B).

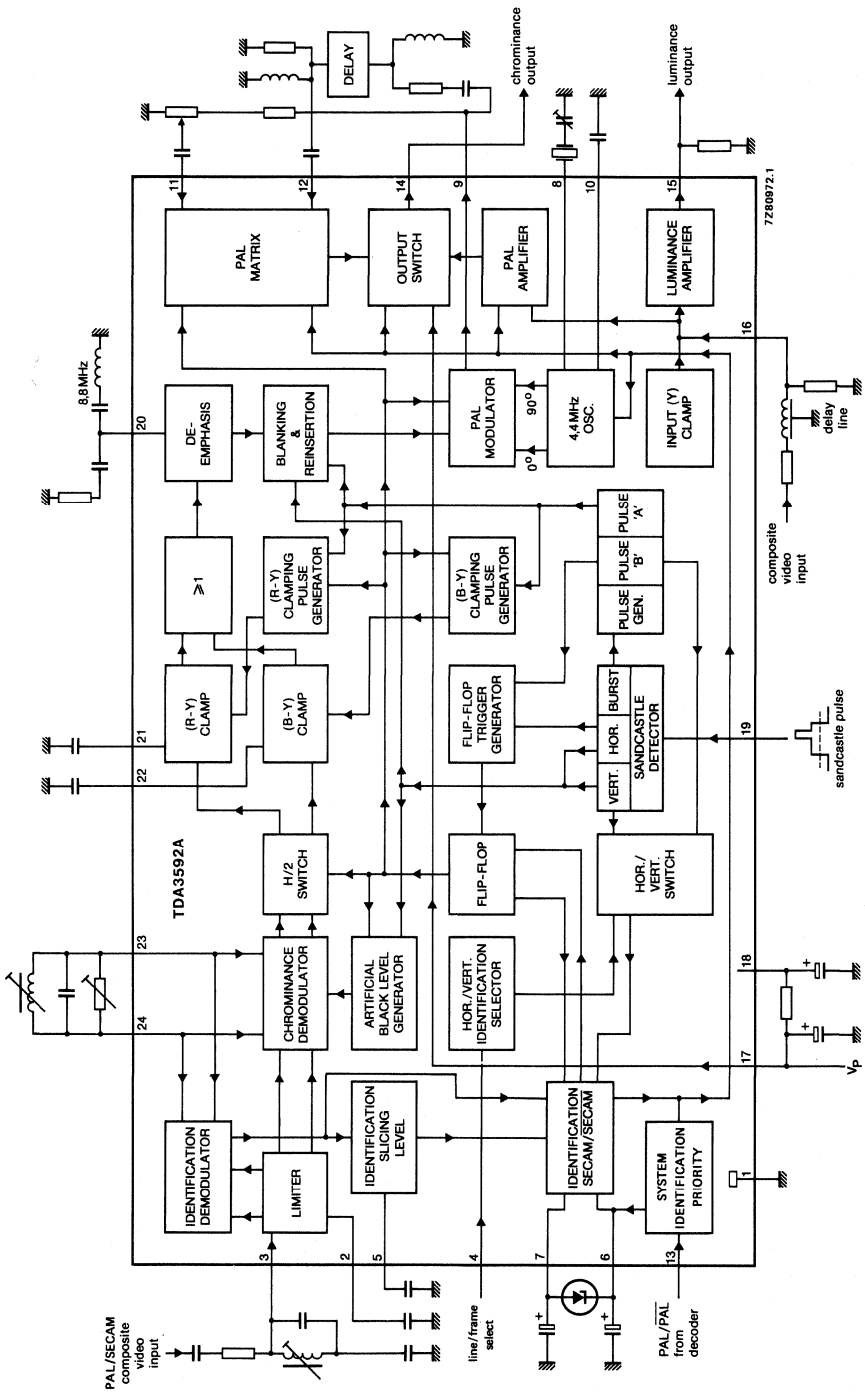


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1. Ground.
2. Limiter feedback.
3. Limiter input: chrominance input SECAM; identification input SECAM/$\overline{\text{SECAM}}$.
4. Identification selection input using a DC level to preset the identification mode.
   At $V_4 < 2{,}9$ V the TDA3592A is preset for frame identification.
   At $V_4 > 4{,}1$ V the TDA3592A is preset for line identification.
5. Storage capacitor input for floating level identification.
6. Storage capacitor input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
7. Double time-constant input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
8. 4,43 MHz oscillator.
9. Sequentially modulated output.
10. Decoupling capacitor for miller integrator feedback circuit.
11. Direct input chrominance signal.
12. Delayed input chrominance signal.
13. PAL/$\overline{\text{PAL}}$ input signal from PAL decoder.
14. Chrominance output signal.
15. Luminance output signal.
16. Luminance/$\overline{\text{SECAM}}$ input signal.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection: R = 560 Ω; C = 1 nF.
21. Storage capacitor connection for (R-Y) clamp.
22. Storage capacitor connection for (B-Y) clamp.
23. Demodulator reference tuned circuit: nominal frequency = 4,33 MHz; nominal $Q_L = 2{,}45$.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizontal blanking periods. This is done because of the possibility of horizontal burst signals not being available. The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and −(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90^{o} out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180^{o} out of phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse 'B' (see Fig. 2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4\text{-}1} < 2{,}9$ V;
- Vertical identification preset when $V_{4\text{-}1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse 'B' times the SECAM horizontal identification.

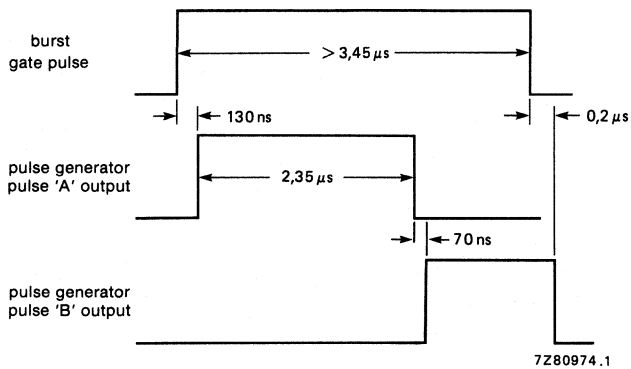


Fig. 2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90^{o} phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the −(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 µs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

FUNCTIONAL DESCRIPTION (continued)

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.

SECAM — The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of $< 1{,}1$ V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).

Black-and-white — The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL decoder mode	System operating mode
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 16 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{17-1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	μA
Decoupled supply voltage (pin 18)	$R_{ext17-18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	μF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j-a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p-p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p-p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		R_{23-24}	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		C_{23-24}	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier and demodulator (continued)						
Linearity of (B-Y) demodulation (pin 20)	note 3	–	–	94	–	%
Linearity of (R-Y) demodulation (pin 20)	note 4	–	–	100	–	%
(R-Y)/(B-Y) ratio (pin 20)		–	–	1,78	–	%
Relative deviation of reinserted black level/demodulated black level (pin 20) as a function of temperature						
(R-Y) signals	note 5	–	–	0,22	–	kHz/°C
(B-Y) signals	note 5	–	–	0,22	–	kHz/°C
Identification SECAM/$\overline{\text{SECAM}}$	note 6					
Input voltage for line identification (pin 4)		V_4	4,1	–	V_P	V
Input voltage for frame identification (pin 4)		V_4	0	–	2,9	V
Switching level for line/frame identification (pin 4)		V_4	3,0	3,5	4,0	V
Input current (pin 4)		$-I_4$	–	5	25	μA
Voltage at pin 6 during $\overline{\text{SECAM}}$/$\overline{\text{PAL}}$		V_6	–	10,2	–	V
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	11,5	–	V
Voltage at pin 6 during SECAM		V_6	–	7,0	–	V
Identification at pin 6		V_6	–	10,6	–	V
Colour OFF for SECAM		V_6	9,8	10,1	10,4	V
Colour ON for SECAM		V_6	8,8	9,1	9,4	V
Slicing level reference voltage (pin 5)		V_5	–	8,4	–	V
Sandcastle pulse detector and clamping pulse generator						
Voltage level at which the vertical blanking pulse is separated		V_{19}	1,0	1,5	2,0	V
Voltage level at which the horizontal blanking pulse is separated		V_{19}	3,0	3,5	4,0	V
Voltage level at which the burst gating pulse is separated		V_{19}	6,5	7,0	7,5	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector and clamping pulse generator (continued)						
Input current	V_{19} = 0 V	$-I_{19}$	–	30	100	μA
Width of pulse 'A' (Fig. 2)	note 7		1,85	2,35	2,85	μA
Required width of pulse 'B' (Fig. 2)	note 7		0,6	–	–	μs
Luminance amplifier						
Input signal (peak-to-peak value) (pin 16)		$V_{16(p-p)}$	–	1,2	1,7	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,5	7,5	8,5	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		Z_{15}	–	20	–	Ω
Frequency response at −3 dB (pin 15 and 16)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	6,0	7,0	8,0	dB
Frequency response at −3 dB (pin 14 and 16)		f	6,0	–	–	MHz
External load resistance (pin 15)		R_L	2,0	–	–	kΩ
Limiter, chrominance demodulator and PAL modulator	note 8					
Output resistance (pin 9)		R_9	–	25	–	Ω
DC output voltage during horizontal blanking (pin 9)		V_9	–	9,6	–	V
Internal biasing resistor for emitter follower (pin 9)			–	9,0	–	kΩ
External load resistance (pin 9)		$R_{L(9)}$	2	–	–	kΩ
Output signal (pin 9) when input to pin 3 has a Δf of 280 kHz; without external load (peak-to-peak value)		$V_{9(p-p)}$	–	0,82	–	mV
(R-Y)/(B-Y) ratio (pin 9)			1,50	1,78	2,11	
Chrominance/burst ratio for SECAM (pin 9)			2,5	3,0	3,5	
Linearity of (B-Y) signal (pin 9)	note 3		85	92	99	%
Linearity of (R-Y) signal (pin 9)	note 4		93	100	107	%
Black level shift as a function of temperature (pin 9)						
(R-Y) signals	note 9		–	0,22	–	kHz/°C
(B-Y) signals	note 9		–	0,22	–	kHz/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Limiter, chrominance demodulator and PAL modulator (continued)						
Phase relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			87	90	93	deg
Amplitude relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			−1,5	0	+1,5	dB
Black level shift as a function of supply voltage (pin 9)						
(R-Y) signal			–	−1,5	–	kHz/V
(B-Y) signal			–	1,0	–	kHz/V
Oscillator						
Oscillator frequency (pin 9) (set with series capacitor)		f_{OSC}	–	4,433619	–	MHz
Frequency deviation without spread of external components (pin 9)		Δf_{OSC}	–	–	±150	Hz
Temperature coefficient of oscillator frequency (pin 9)			–	−2	−3	Hz/°C
Frequency deviation for change of V_P from 9,0 to 13,2 V		Δf_{OSC}	–	–	150	Hz
DC voltage (pin 8)		V_8	–	4,7	–	V
Input resistance (pin 8)		R_8	–	1	–	kΩ
DC voltage (pin 10)		V_{10}	–	4,4	–	V
Input resistance (pin 10)		R_{10}	–	2	–	kΩ
PAL matrix						
Input resistance (pin 11)		R_{11}	700	900	1100	Ω
Input resistance (pin 12)		R_{12}	700	900	1100	Ω
Output resistance (pin 14) (SECAM/$\overline{\text{SECAM}}$)		R_{14}	–	40	–	Ω
Internal emitter follower load resistance (pin 14)		$R_{INT(14)}$	–	7	–	kΩ
External load resistor (pin 14)		$R_{L(14)}$	2,4	–	–	kΩ
DC voltage (pin 11)		V_{11}	–	5,0	–	V
DC voltage (pin 12)		V_{12}	–	5,0	–	V
DC voltage (pin 14)	SECAM mode	V_{14}	–	6,2	–	V
DC voltage (pin 14)	$\overline{\text{SECAM}}$ mode and line blanking	V_{14}	–	4,9	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
PAL matrix (continued)						
H/2 ripple on chrominance output (pin 14) (peak-to-peak value)	SECAM mode	$V_{14(p-p)}$	–	–	100	mV
Gain A; pin 11 to 14		G_A	9	10	11	dB
Gain B; pin 12 to 14 ((R-Y) at pin 9)		G_B	9	10	11	dB
Gain C; pin 12 to 14 ((B-Y) at pin 9)		G_C	9	10	11	dB
Gain A – gain B		G_A-G_B	–0,7	–	+0,7	dB
Gain A – gain C		G_A-G_C	–0,7	–	+0,7	dB
Gain B – gain C		G_B-G_C	–0,7	–	+0,7	dB
Phase A; pins 11, 14 to pins 12, 14 ((R-Y) at pin 9)			–	181,5	–	deg
Phase B; pins 11, 14 to pins 12, 14 ((B-Y) at pin 9)			–	1,5	–	deg
Phase A – phase B			178	180	182	deg
Identification PAL/$\overline{\text{PAL}}$						
Input condition for PAL (pin 13)		V_{13}	1,7	–	V_P	V
Input condition for $\overline{\text{PAL}}$ (pin 13)		V_{13}	–	–	1,1	V
Input current	V_{13} = 6 V	I_{13}	–	–	10	μA
Input resistance	V_{13} = 8,2 V	R_{13}	7,5	11,5	15,5	kΩ
Pin 6 internal current in PAL/$\overline{\text{SECAM}}$ mode		$-I_6$	0,24	0,4	0,58	mA
Switching level PAL/$\overline{\text{PAL}}$ (pin 13)		V_{13}	1,2	1,4	1,6	V

DEVELOPMENT DATA

CHARACTERISTICS AT LOW SUPPLY VOLTAGE

$V_P = V_{17-1} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply current		$I_{17}+I_{18}$	16	20	24	mA
Supply voltage switching level for preset SECAM signal path	SECAM processing OFF	V_{17-1}	6,5	7,5	8,2	V
Luminance amplifier						
Input signal (peak-to-peak value)		$V_{16(p-p)}$	–	0,45	0,56	V
Gain (pin 16 to 15)	$f_{16} = 4,4$ MHz	G_{16-15}	6,0	7,0	8,0	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		$\lvert Z_{15-1}\rvert$	–	20	–	Ω
Minimum load resistance (pin 15)		R_L	2	–	–	kΩ
Frequency response at −3 dB (pin 16 to 15)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	$f_{16} = 4,4$ MHz	G_{16-14}	5,7	6,8	7,9	dB
Frequency response at −3 dB (pin 16 to 14)		f	6	–	–	MHz

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 3 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 14 to the PAL decoder is minimum during scan (PAL black colour information).
2. When the input signal to the limiter (pin 3) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz; f = 4,33 MHz (typ.).
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz.
5. The parameter value is equated by: $\frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y - X} \times \frac{\Delta f\ (kHz)}{^{o}C}$

   $E = \frac{E1 - E2}{2}$ $\quad F = \frac{F1 - F2}{2}$

   Where A = demodulated black level at temperature X
   B = demodulated black level at temperature Y
   C = artificial black level at temperature X
   D = artificial black level at temperature Y
   E1 = demodulated output signal at temperature X ($f_o - \Delta f$)
   E2 = demodulated output signal at temperature X ($f_o + \Delta f$)
   F1 = demodulated output signal at temperature Y ($f_o - \Delta f$)
   F2 = demodulated output signal at temperature Y ($f_o + \Delta f$)

   for B-Y: $f_o = f_{ob}$ = 4,25 MHz (Δf = 230 kHz)
   for R-Y: $f_o = f_{or}$ = 4,40625 MHz (Δf = 280 kHz)
6. During stable signal conditions V_7 is always at V_F(BAT85) below V_6.
7. The burst gate pulse width $>$ 3,45 μs.
8. The specification figures are only valid when the reference tuned circuit is aligned as indicated in note 1.
9. Ensure that the 4,433 MHz carrier is in the correct phase; black level shift at temperature X = A and at Y = B.
   Output signal (Δf = 230 kHz for B-Y; Δf = 280 kHz for R-Y) at temperature X = E and at Y = F.

   The parameter is equated by: $\frac{(B/(F\text{-}B) - A/(E\text{-}A)}{Y - X} \times 230;\ 280\ kHz$
10. Chrominance definition — burst ratio at SECAM condition (pin 9).

    The parameter is equated by: $\frac{V_{out(p\text{-}p)}\ Red\ (R\text{-}Y)}{V_{burst(p\text{-}p)}\ (R\text{-}Y)}$.

DEVELOPMENT DATA

APPLICATION INFORMATION

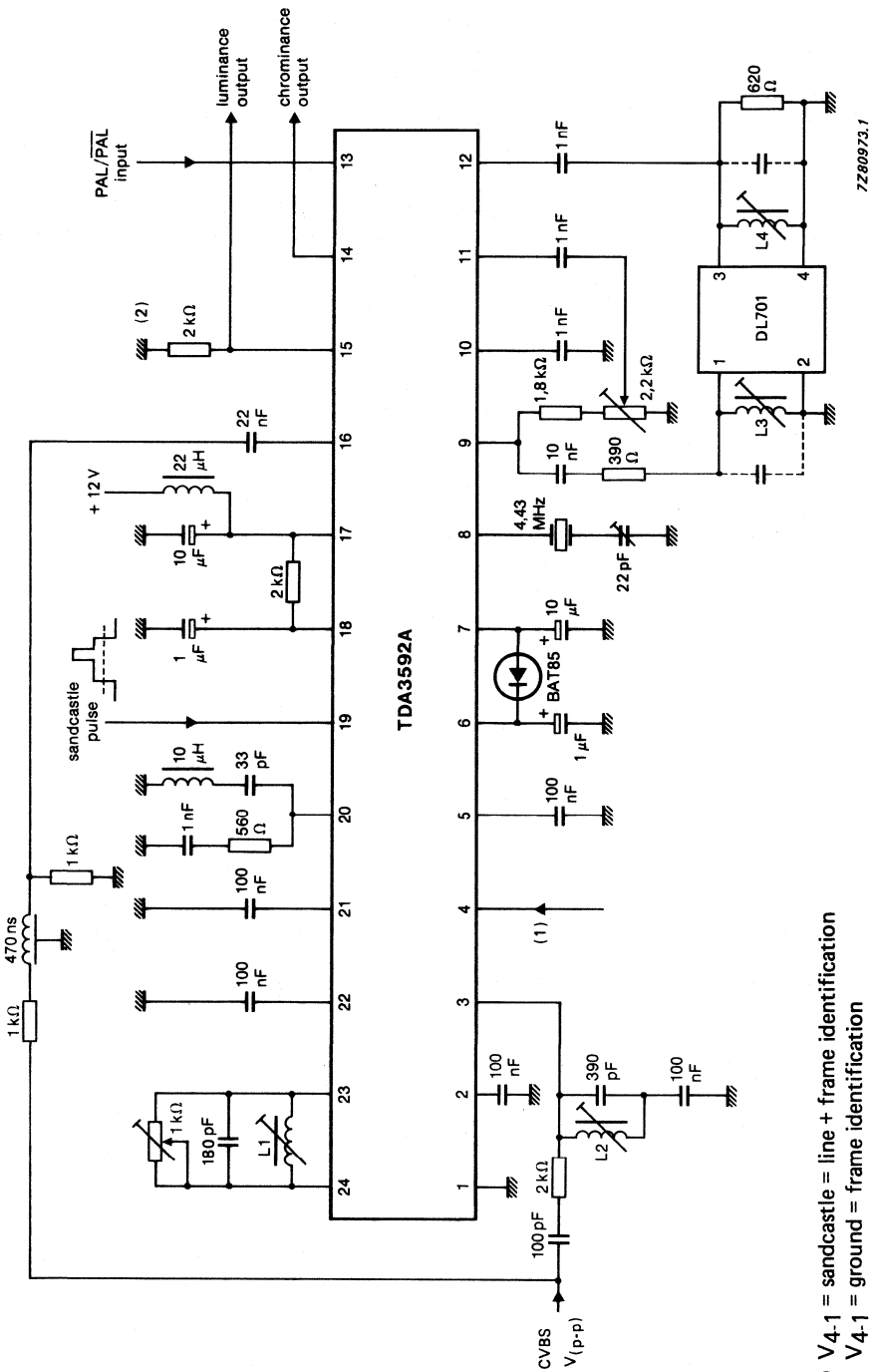


Fig. 3 Application circuit.

(1) V_{4-1} = sandcastle = line + frame identification
V_{4-1} = ground = frame identification
$V_{4-1} = V_P$ = line identification

(2) minimum load resistance at pin 15 = 2 kΩ

VERTICAL DEFLECTION AND GUARD CIRCUIT (90°)

GENERAL DESCRIPTION

The TDA3653B/C is a vertical deflection output circuit for drive of various deflection systems with currents up to 1.5 A peak-to-peak.

Features

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer
- Guard circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply (note 1)					
Supply voltage range					
pin 9	$V_P = V_{9-4}$	10	–	40	V
pin 6	V_{6-4}	–	–	60	V
Output (pin 5)					
Peak output voltage during flyback	V_{5-4M}	–	–	60	V
Output current	$I_{5(p-p)}$	–	1.2	1.5	A
Operating junction temperature range	T_j	−25	–	+150	°C
Thermal resistance junction to mounting base					
(SOT110B)	$R_{th\ j-mb}$	–	10	–	K/W
(SOT131)	$R_{th\ j-mb}$	–	3.5	–	K/W

Note to the quick reference data

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.

PACKAGE OUTLINES

TDA3653B: 9-lead SIL; plastic (SOT110B).
TDA3653C: 9-lead SIL; plastic power (SOT131).

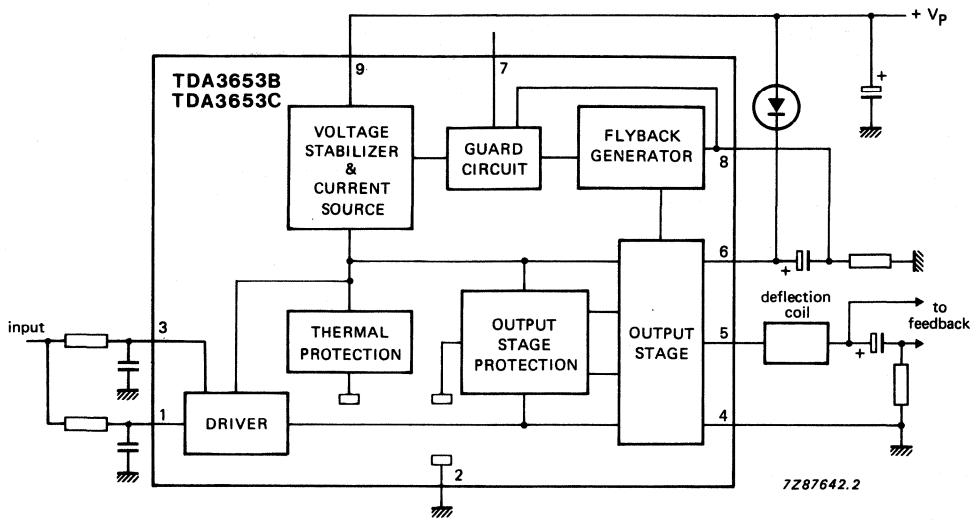


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 0.75 A maximum. The maximum voltage for pin 5 and 6 is 60 V.

The output power transistors are protected such that their operation remains within the SOAR area. This is achieved by the co-operation of the thermal protection circuit, the current-voltage detector, the short-circuit protection and the special measures in the internal circuit layout.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied via external resistors to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.

External connection of pin 1 to pin 3 allows for applications in which the pins are driven separately.

Flyback generator

During scan the capacitor connected between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig.1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is > 2.5 V, during normal operation.

Guard circuit

When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 1.8 V. The guard circuit will then produce a DC voltage at pin 7, which can be used to blank the picture tube and thus prevent screen damage.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, which prevents the drive current of the output stage being affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); pins 4 and 2 externally connected to ground.

paramater	symbol	min.	max.	unit
Supply voltage (pin 9)	$V_P = V_{9-4}$	–	40	V
Supply voltage output stage (pin 6)	V_{6-4}	–	60	V
Output voltage (pin 5)	V_{5-4}	–	60	V
Input voltage (pins 1 and 3)	$V_{1;3-2}$	–	V_P	V
External voltage at pin 7	V_{7-2}	–	5.8	V
Peak output current (pin 5)				
repetitive	$\pm I_{5RM}$	–	0.75	A
non-repetitive	$\pm I_{5SM}$	–	1.5	A*
Peak output current (pin 8)				
repetitive	I_{8RM}	0.85	0.75	A
non-repetitive	$\pm I_{8SM}$	–	1.5	A*
Total power dissipation	P_{tot}	see Fig. 2		
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature range	T_{amb}	see Fig. 2		
Operating junction temperature range	T_j	–25	+150	°C

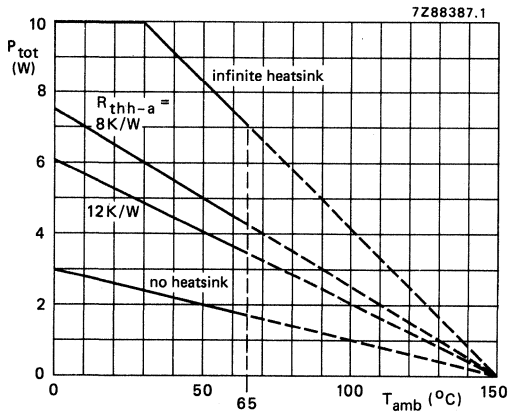


Fig. 2 Power derating curves (for SOT110B).

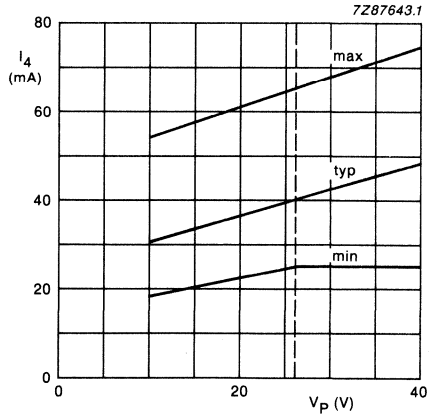


Fig. 3 Quiescent current I_4 as a function of supply voltage V_P.

* Non-repetitive dutv factor maximum 3.3%.

CHARACTERISTICS

$V_P = V_{9-4}$ = 26 V; T_{amb} = 25 °C; pins 2 and 4 externally connected to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 9)	note 1	$V_P = V_{9-4}$	10	–	40	V
Supply voltage (pin 6)	note 1	V_{6-4}	–	–	60	V
Total supply current (pin 6 and pin 9)	note 2	$I_P = I_6 + I_9$	34	50	85	mA
Quiescent current (pin 4)	see Fig. 3	I_4	25	40	65	mA
Variation of quiescent current with temperature		ΔI_4	–	–0.04	–	mA/K
Output current						
Output current (pin 5) (peak-to-peak value)		$I_{5(p-p)}$	–	1.2	1.5	A
Output current flyback generator (pin 8)		$-I_8$	–	0.7	0.85	A
Output current flyback generator (pin 8)		I_8	–	0.6	0.75	A
Output voltage						
Peak voltage during flyback		V_{5-4M}	–	–	60	V
Saturation voltage to supply						
at $-I_5$ = 0.75 A		V_{6-5sat}	–	2.5	3.0	V
at I_5 = 0.75 A	note 3	V_{5-6sat}	–	2.5	3.0	V
at $-I_5$ = 0.60 A		V_{6-5sat}	–	2.2	2.7	V
at I_5 = 0.60 A	note 3	V_{5-6sat}	–	2.3	2.8	V
Saturation voltage to ground						
at I_5 = 0.75 A		V_{5-4sat}	–	2.3	2.7	V
at I_5 = 0.60 A		V_{5-4sat}	–	2.1	2.4	V
Flyback generator						
Saturation voltage						
at $-I_8$ = 0.85 A		V_{9-8sat}	–	1.6	2.1	V
at I_8 = 0.75 A	note 3	V_{8-9sat}	–	2.3	2.8	V
at $-I_8$ = 0.70 A		V_{9-8sat}	–	1.4	1.9	V
at I_8 = 0.60 A	note 3	V_{8-9sat}	–	2.2	2.7	V
Flyback generator active if:		V_{5-9}	4.0	–	–	V
Leakage current at pin 8		$-I_8$	–	5.0	100	μA
Input						
Input current (pin 1)	I_5 = 0.75 A	I_1	–	0.33	0.55	mA
Input voltage during scan (pin 1)	I_5 = 0.75 A	V_{1-2}	–	1.5	2.4	V
Input voltage during scan (pin 3) pins 1 and 3 not connected		V_{3-2}	0.8	–	V_P	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input (continued)						
Input current during scan (pin 3)						
pins 1 and 3 not connected		I_3	0.03	–	–	mA
pins 1 and 3 connected		I_3	–	–	0.21	mA
Input resistance (pin 3)		R_3	3.9	5.3	6.7	kΩ
Input voltage during flyback (pin 1)		V_{1-2}	–	–	250	mV
Input voltage during flyback (pin 3)		V_{3-2}	–	–	250	mV
Guard circuit						
Output voltage (pin 7)	note 4					
loaded with 100 kΩ		V_{7-2}	4.4	5.1	5.8	V
loaded with 0.5 mA		V_{7-2}	3.6	4.4	5.3	V
Internal series resistance of pin 7		R_{i7}	0.95	1.35	1.7	kΩ
Guard circuit active if V_{8-2} is lower than	note 5	V_{8-2}	–	–	1.8	V
General data						
Thermal protection becomes active if junction temperature exceeds		T_j	158	175	192	°C
Thermal resistance junction to mounting base		$R_{th\ j\text{-}mb}$	–	10	12	K/W
Open loop gain at 1 kHz	note 6	G_{ol}	–	42	–	dB
Frequency response (–3 dB)	note 7	f	–	40	–	kHz

Notes to the characteristics

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.
2. When V_{5-4} = 13 V and no load at pin 5.
3. Duty factor maximum 3.3%.
4. Guard circuit is active.
5. During normal operation the voltage V_{8-2} may not be lower than 2.5 V.
6. R_{load} = 8 Ω; $I_{load(rms)}$ = 125 mA.
7. With 220 pF between pins 1 and 5.

APPLICATION INFORMATION

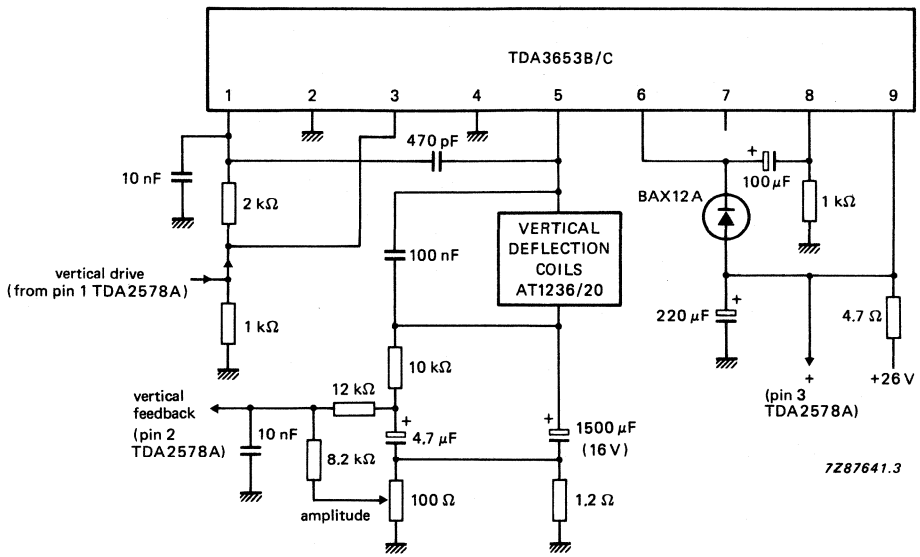


Fig. 4 Typical application circuit diagram of the TDA3653B/C (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13.6 Ω; deflection current without overscan is 0.82 A peak-to-peak and EHT voltage is 25 kV.

APPLICATION INFORMATION (continued)

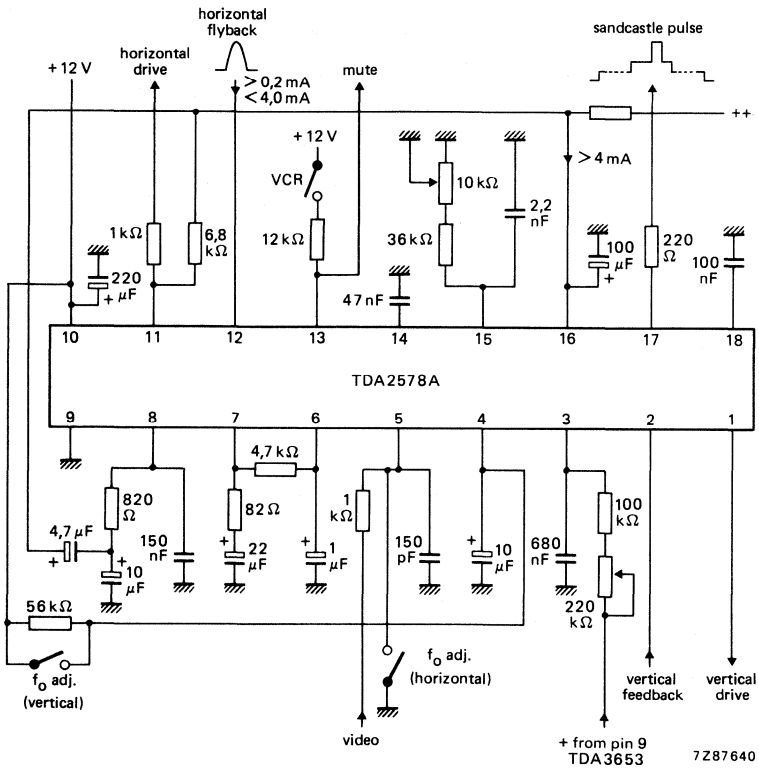


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3653B/C (see Fig. 4).

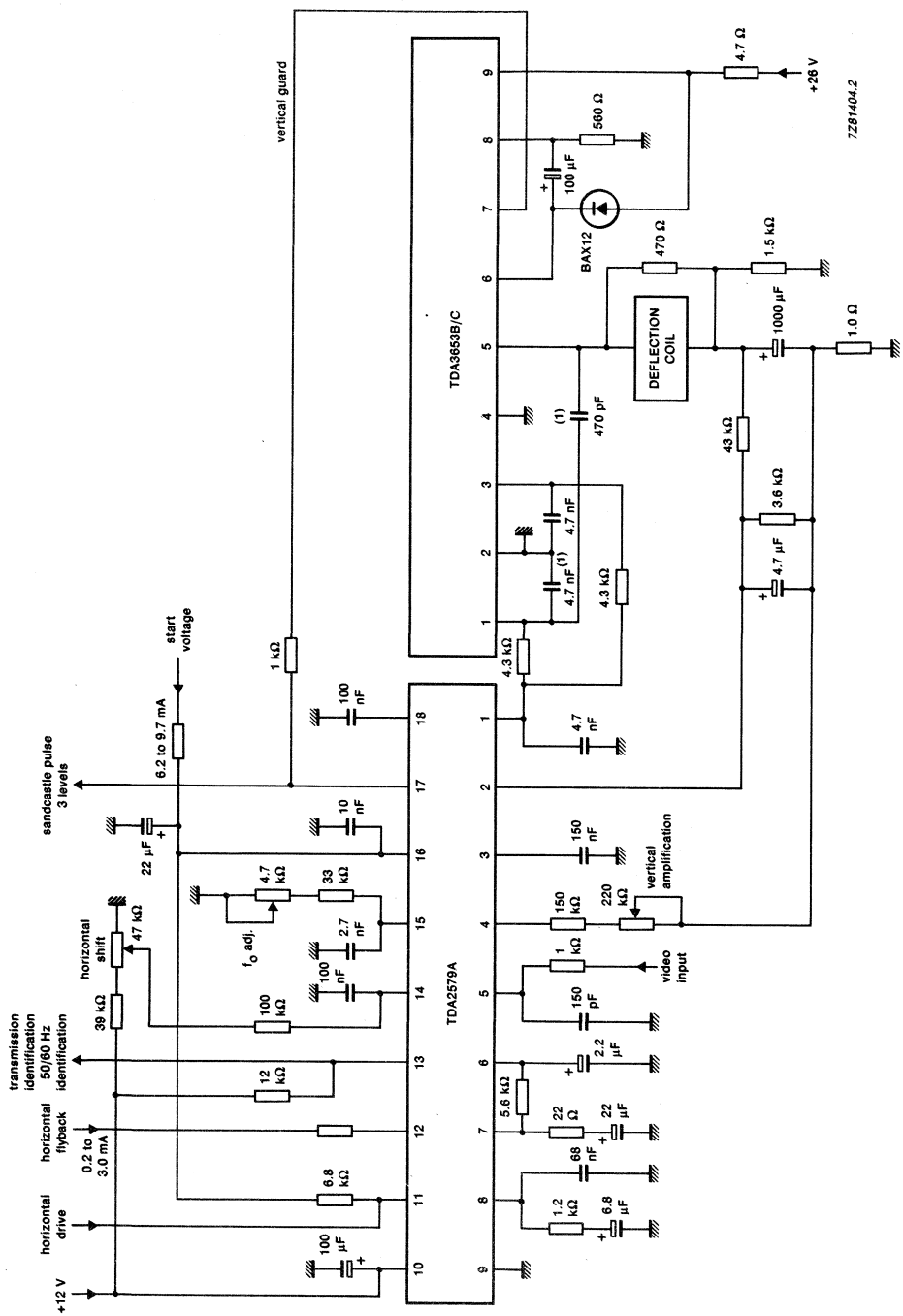


Fig.6 Application circuit diagram for combination with TDA2579A for 90° picture tube.

(1) Dependent on PCB layout.

VERTICAL DEFLECTION AND GUARD CIRCUIT (110°)

GENERAL DESCRIPTION

The TDA3654 is a full performance vertical deflection output circuit for direct drive of the deflection coils and can be used for a wide range of 90° and 110° deflection systems.
A guard circuit is provided which blanks the picture tube screen in the absence of deflection current.

Features

- Direct drive to the deflection coils
- 90° and 110° deflection system
- Internal blanking guard circuit
- Internal voltage stabilizer

QUICK REFERENCE DATA

Output voltage	V_{5-2}	max.	60	V
Output current (peak-to-peak)	$I_{5(p-p)}$	max.	3	A
Supply voltage	V_{9-2}	max.	40	V
Guard circuit output voltage	V_{7-2}	max.	5,6	V
Operating ambient temperature range	T_{amb}		−25 to +60	°C
Storage temperature	T_{stg}		−55 to +150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	3,5 to 4	K/W

PACKAGE OUTLINES

TDA3654 : 9-lead SIL; plastic power (SOT131).
TDA3654Q : 9-lead SIL bent to DIL; plastic power (SOT157).

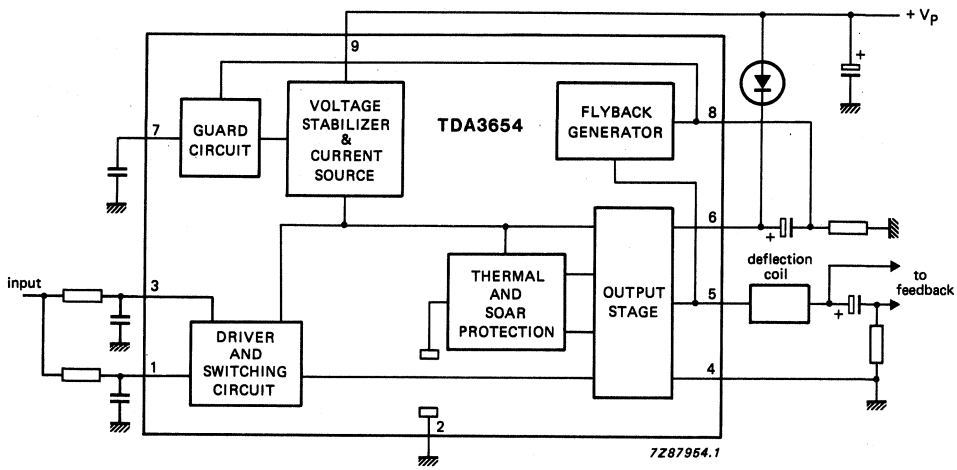


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuits

The output stage consists of two Darlington configurations in class B arrangement.
Each output transistor can deliver 1,5 A maximum and the V_{CEO} is 60 V.
Protection of the output stage is such that the operation of the transistors remains well within the SOAR area in all circumstances at the output pin, (pin 5). This is obtained by the cooperation of the thermal protection circuit, the current-voltage detector and the short circuit protection.
Special measures in the internal circuit layout give the output transistors extra solidity, this is illustrated in Fig. 5 where typical SOAR curves of the lower output transistor are given. The same curves also apply for the upper output device. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit (pin 1 and 3 are connected via external resistors).
This switching circuit rapidly turns off the lower output stage when the flyback starts and it, therefore, allows a quick start of the flyback generator. The maximum required input signal for the maximum output current peak-to-peak value of 3 A is only 3 V, the sum of the currents in pins 1 and 3 is then maximum 1 mA.

Flyback generator

During scan, the capacitor between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig. 1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is $> 1{,}5$ V, during normal operation.

Guard circuit

When there is no deflection current, for any reason, the voltage at pin 8 becomes less than 1 V, the guard circuit will produce a d.c. voltage at pin 7. This voltage can be used to blank the picture tube, so that the screen will not burn in.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, so the drive current is not affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Pins 2 and 4 are externally connected to ground.

Voltages

Output voltage	V_{5-4}	0 to 60	V
Supply voltage	V_{9-4}	0 to 40	V
Supply voltage output stage	V_{6-4}	0 to 60	V
Input voltage	V_{1-2}	0 to V_{9-4}	V
Input voltage switching circuit	V_{3-2}	0 to V_{9-4}	V
External voltage at pin 7	V_{7-2}	0 to 5,6	V

Currents

Repetitive peak output current	$\pm I_{5RM}$	max.	1,5	A
Non-repetitive peak output current (note 1)	$\pm I_{5SM}$	max.	3	A
Repetitive peak output current of flyback generator	I_{8RM}	max.	+ 1,5 −1,6	A A
Non-repetitive peak output current of flyback generator (note 1)	$\pm I_{8SM}$	max.	3	A

Temperatures

Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to + 60	°C
Operating junction temperature range (the output current at pin 5 should not exceed 2.5A)	T_j	−25 to + 150	°C

CHARACTERISTICS

T_{amb} = 25 °C, supply voltage (V_{9-4}) = 26 V; unless otherwise stated; pin 1 externally connected to pin 3. Pins 2 and 4 externally connected to ground.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage, pin 9 (note 2)	V_{9-4}	10	–	40	V
Supply voltage output stage	V_{6-4}	–	–	60	V
Supply current, pins 6 and 9 (note 3)	I_6+I_9	35	55	85	mA
Quiescent current (note 4)	I_4	25	40	65	mA
Variation of quiescent current with temperature	TC	–	–0,04	–	mA/K
Output current					
Output current, pin 5 (peak-to-peak)	$I_{5(p-p)}$	–	2,5	3	A
Output current flyback generator, pin 8	$+ I_{8(p-p)}$	–	1,25	1,5	A
	$-I_{8(p-p)}$	–	1,35	1,6	A
Output voltage					
Peak voltage during flyback	V_{5-4}	–	–	60	V
Saturation voltage to supply					
at I_5 = –1,5 A	$V_{6-5(sat)}$		2,5	3,2	V
at I_5 = 1,5 A (note 5)	$V_{5-6(sat)}$		2,5	3,2	V
at I_5 = –1,2 A	$V_{6-5(sat)}$		2,2	2,7	V
at I_5 = 1,2 A (note 5)	$V_{5-6(sat)}$		2,3	2,8	V
Saturation voltage to ground					
at I_5 = 1,2 A	$V_{5-4(sat)}$	–	2,2	2,7	V
at I_5 = 1,5 A	$V_{5-4(sat)}$	–	2,5	3,2	V
Flyback generator					
Saturation voltage					
at I_8 = –1,6 A	$V_{9-8(sat)}$	–	1,6	2,1	V
at I_8 = 1,5 A (note 5)	$V_{8-9(sat)}$	–	2,3	3	V
at I_8 = –1,3 A	$V_{9-8(sat)}$	–	1,4	1,9	V
at I_8 = 1,2 A (note 5)	$V_{8-9(sat)}$	–	2,2	2,7	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Flyback generator active if:	V_{5-9}	4	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Input					
Input current, pin 1, for I_5 = 1,5 A	I_1	–	0,33	0,55	mA
Input voltage during scan, pin 1	V_{1-2}	–	2,35	3	V
Input current, pin 3, during scan (note 6)	I_3	0,03	–	–	mA
Input voltage, pin 3, during scan (note 6)	V_{3-2}	0,8	–	V_{9-4}	V
Input voltage, pin 1, during flyback	V_{1-2}	–	–	250	mV
Input voltage, pin 3, during flyback	V_{3-2}	–	–	250	mV
Guard circuit					
Output voltage, pin 7 R_L = 100 kΩ (note 9)	V_{7-2}	4,1	4,5	5,8	V
Output voltage, pin 7 at I_L = 0,5 mA (note 9)	V_{7-2}	3,4	3,9	5,3	V
Internal series resistance of pin 7	Ri_7	0,95	1,35	1,7	kΩ
Guard circuit activates (note 7)	V_{8-2}	–	–	1,0	V
General data					
Thermal protection activation range	T_j	158	175	192	°C
Thermal resistance					
From junction to mounting base	$R_{th\ j\text{-}mb}$	–	3,5	4	K/W
Power dissipation	P_{tot}	–	see Fig. 3		
Open loop gain at 1 kHz; (note 8)	G_o	–	33	–	
Frequency response, –3 dB; (note 10)	f	–	60	–	kHz

Notes to the characteristics

1. Non-repetitive duty factor 3,3%.
2. The maximum supply voltage should be chosen so that during flyback the voltage at pin 5 does not exceed 60 V.
3. When V_{5-4} is 13 V and no load at pin 5.
4. See Fig. 4.
5. Duty cycle, d = 5% or d = 0,05.
6. When pin 3 is driven separately from pin 1.
7. During normal operation the voltage V_{8-2} may not be lower than 1,5 V.
8. $R_L = 8\ \Omega$; $I_L = 125$ mA (r.m.s.).
9. If guard circuit is active.
10. With a 22 pF capacitor between pins 1 and 5.

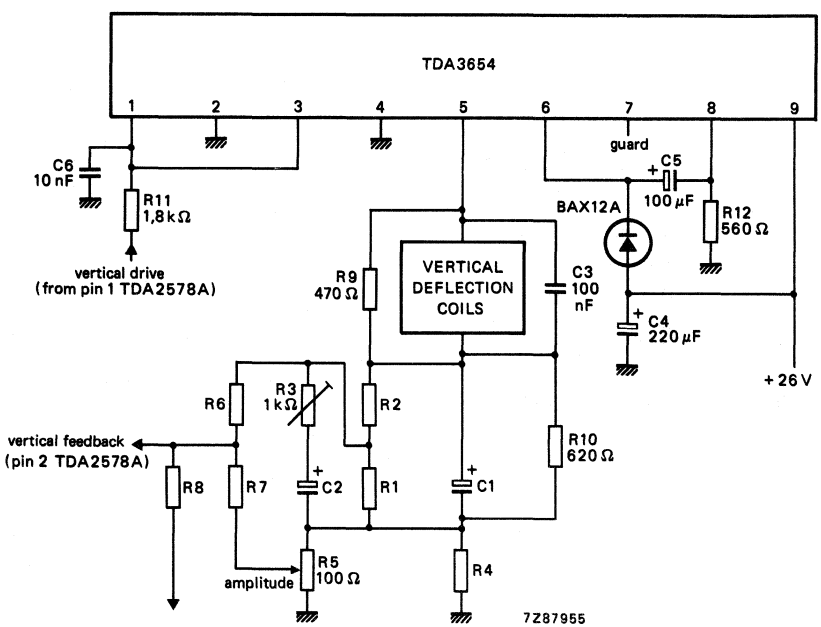


Fig. 2 Application diagram.

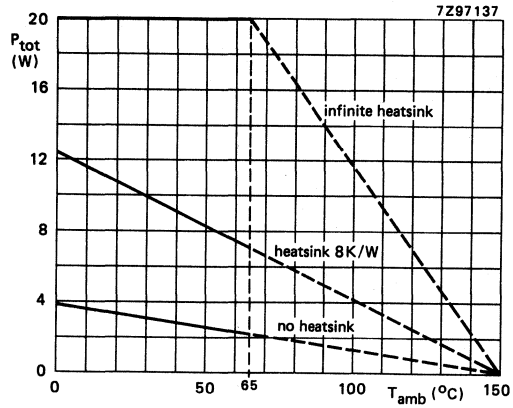


Fig. 3 Power derating curve.

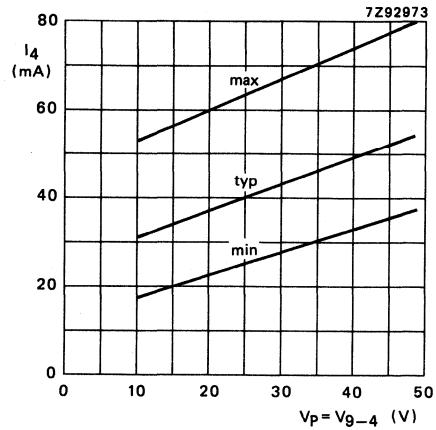
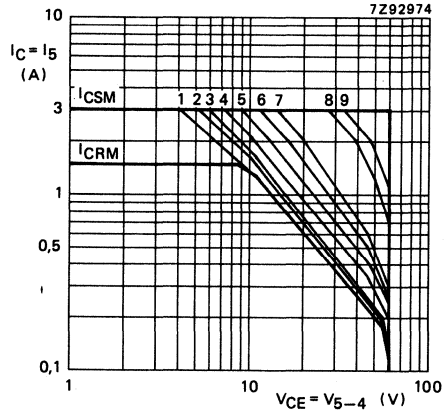


Fig. 4 Quiescent current as a function of the supply voltage.

curve	t_p	δ	peak junction temperature
1	d.c.	—	150 °C
2	10 ms	0,5	150 °C
3	10 ms	0,25	150 °C
4	1 ms	0,5	150 °C
5	1 ms	0,25	150 °C
6	1 ms	0,05	150 °C
7	1 ms	0,05	180 °C
8	0,2 ms	0,1	150 °C
9	0,2 ms	0,1	180 °C



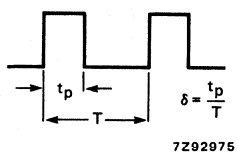


Fig. 5 Typical SOAR of lower output transistor.

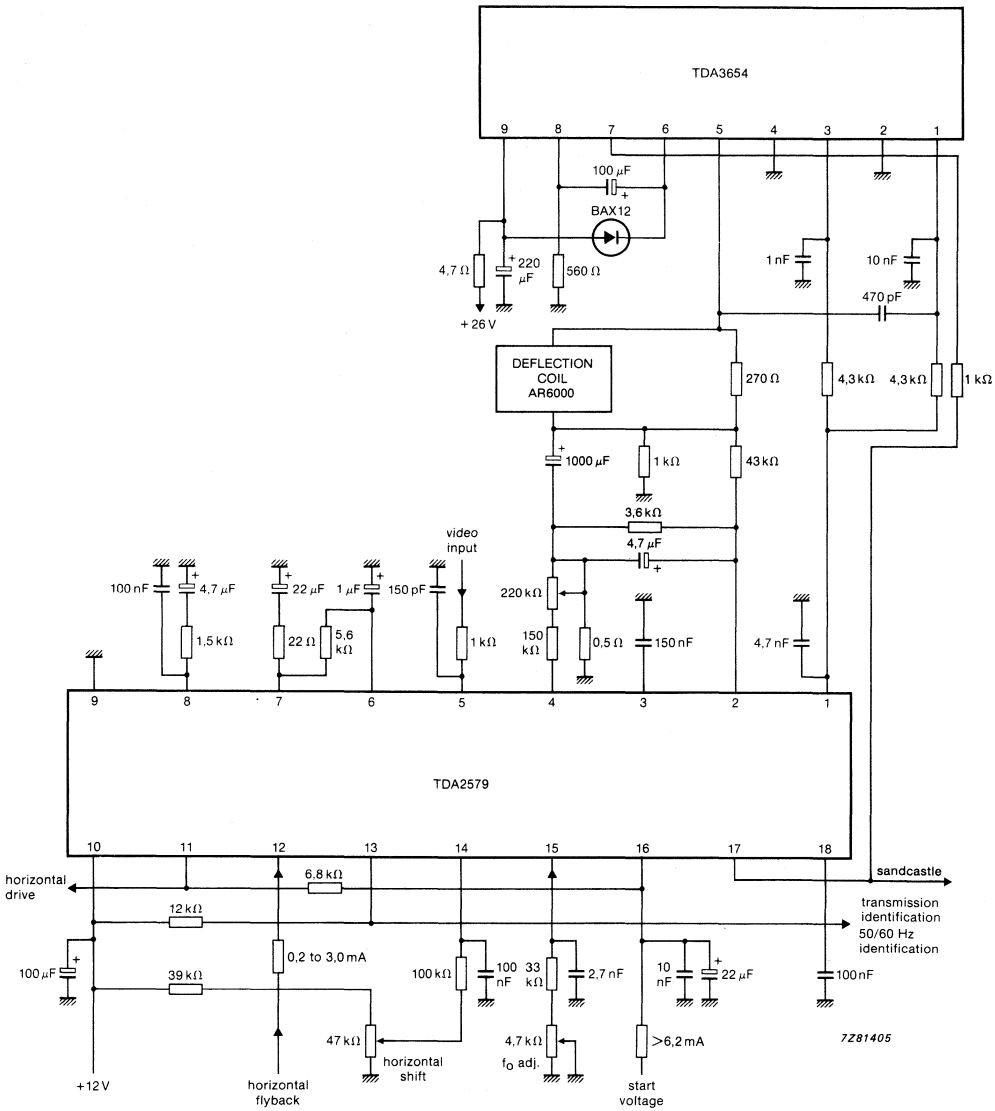


Fig. 6 Application diagram in combination with TDA2579.

SECAM IDENTIFICATION CIRCUIT

GENERAL DESCRIPTION

The TDA3724 is a monolithic integrated circuit for SECAM identification in PAL/SECAM (B,G) video tape recorders.

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10-8}$	typ.	10 V
Supply current (pin 10)	$I_P = I_{10}$	typ.	16 mA
Identification inputs	V_{3-8} (p-p)	min.	0,22 V
Identification inputs	V_{4-8} (p-p)	min.	0,22 V
Identification output current	I_1	min.	3 mA

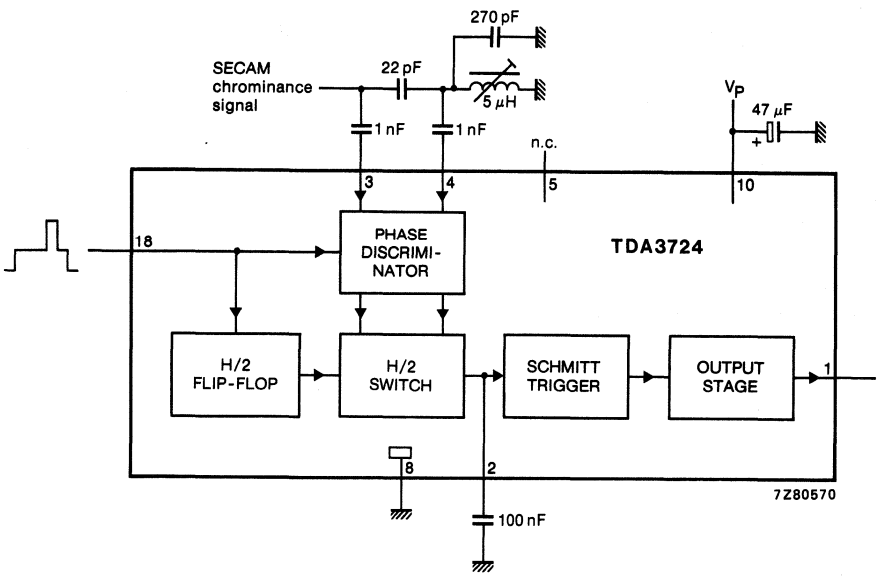


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{10-8}$	max.	13,2	V
Voltage range at pins 3,4,18	V_{n-8}		0 to V_P	V
Voltage range at pin 2	V_{2-8}		½V_P to V_P	V
Current at pin 1	$-I_1$		5	mA
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply at pin 10					
Supply voltage	$V_P = V_{10-8}$	9,6	10	13,2	V
Supply current at V_P = 10 V	I_{10}	–	16	21	mA
Supply current at V_P = 13,2 V	I_{10}	–	–	28	mA
Output voltage at pin 1 (open collector of pnp transistor) at SECAM mode	V_{1-8}	9,3	–	–	V
Output current pin 1 at SECAM mode	$-I_1$	3	–	–	mA
Output current pin 1 at NOT SECAM mode	$-I_1$	–	–	10	μA
Charge capacitor for ident. integration	C_{2-8}	100	–	2000	nF
Identification inputs pin 3,4					
input voltage	$V_{3,\,4-8\,(p-p)}$	0,22	–	1,0	V
input resistance	$R_{3,\,4-8}$	14	–	22	kΩ
Sandcastle input pin 18					
input voltage for active discriminating stage	V_{18-8}	6,0	–	V_P	V

SECAM (L) CHROMINANCE PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3725 is a monolithic integrated circuit for chrominance processing in SECAM (L) video recorders.

Features

- SECAM identification with output stage of SECAM/NOT SECAM identification
- Input to force recording or playback mode
- A.G.C. amplifier and soft limiting amplifier for SECAM chrominance inputs
- Divide by 4 of the chrominance frequencies for recording mode
- Rectifier and multiplier to generate 4 times SECAM chrominance frequencies at playback mode with external filtering
- Output for monitoring

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)	$V_P = V_{10-8}$	–	10	–	V
Supply current (pin 10)	$I_p = I_{13}$	–	38	–	mA
Chroma input signal (record)	$V_{11-8(p-p)}$	25	–	–	mV
Chroma input signal (playback)	$V_{9-8(p-p)}$	25	–	–	mV
Identification inputs	$V_{3-8(p-p)}$	0,22	–	1	V
Identification inputs	$V_{4-8(p-p)}$	0,22	–	1	V
Identification output current	I_1	3	–	–	mA
Monitor output	$V_{14-8(p-p)}$	–	0,6	–	V
Suppression of 2,2 MHz	α_{14}	–	35	–	dB
Suppression of 8,8 MHz	α_{14}	–	10	–	dB
Recording output (a.c.)	$V_{16-8(p-p)}$	–	3	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

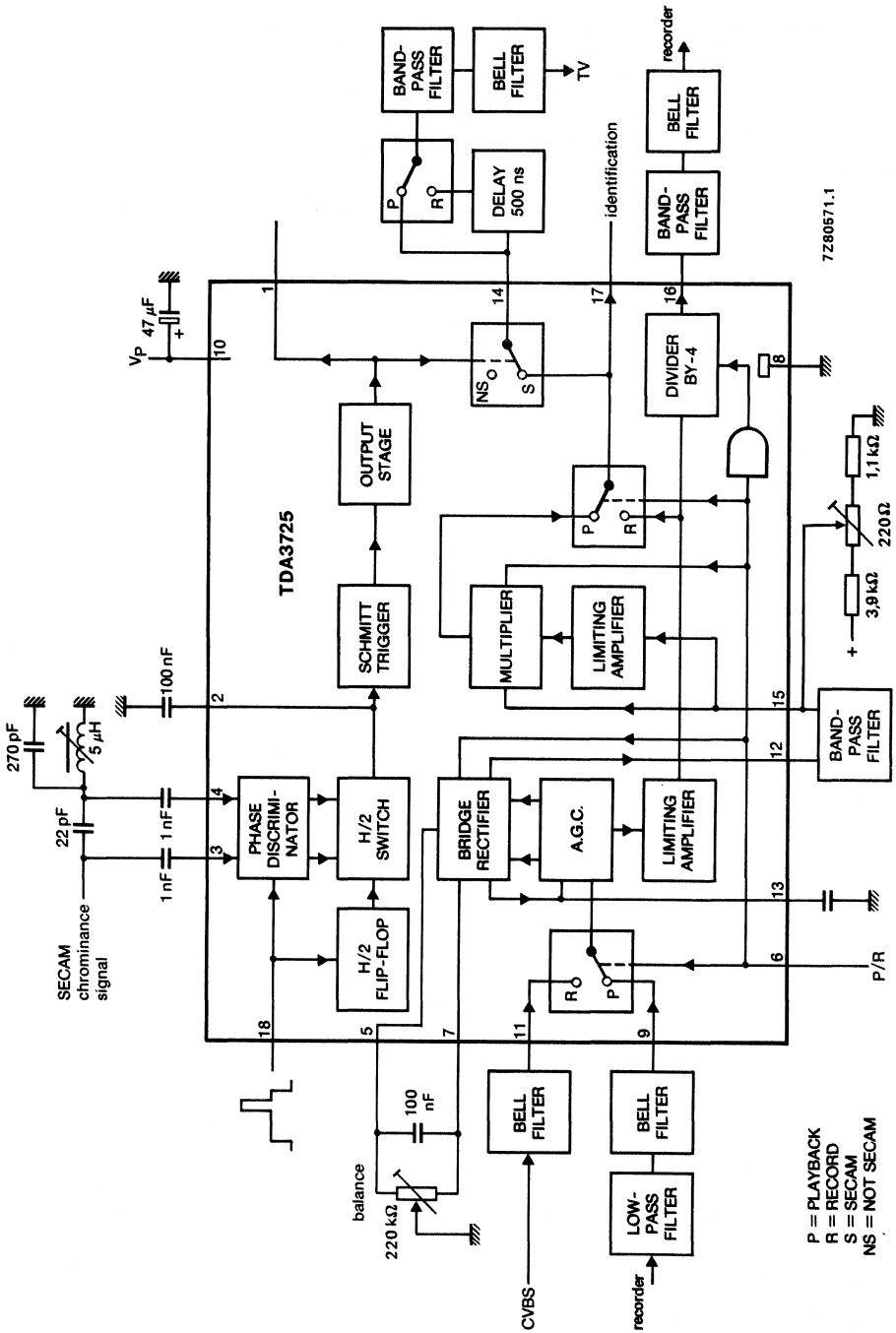


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage pin 10	$V_P = V_{10-8}$	–	–	13,2	V
Voltage range at pins 3,4,5,6, 7,9,11,15,18 to pin 8 (ground)	V_{n-8}	0	–	V_P	V
Voltage range at pin 2 to pin 8	V_{2-8}	½V_P	–	V_P	V
Currents at pins 1,12,13,14,16,17	$-I_n$	–	–	5	mA
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °; measured in Fig. 1, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-8}$	9,6	10	13,2	V
Supply current at V_P = 10 V	I_{10}	–	38	50	mA
Supply current at V_P = 13,2 V	I_{10}	–	–	66	mA
Input switch and a.g.c.					
Input signal at record mode	$V_{11-8(p-p)}$	25	–	500	mV
Input signal at playback mode	$V_{9-8(p-p)}$	25	–	150	mV
Output signal (rectified) pin 12 (2,2 MHz)	$V_{12-8(p-p)}$	–	300	–	mV
d.c. level	V_{12-8}	5,0	5,5	–	V
Suppression of 1,1 MHz	α_{12}	30	32	–	dB
Suppression of 3,3 MHz	α_{12}	40	42	–	dB
Suppression of 4,4 MHz	α_{12}	10	14	–	dB
Output resistance	R_{12-8}	–	V_T/I_C	–	Ω
Mixer and limiter					
Input resistance pin 15	R_{15-8}	0,5	–	–	MΩ
Output signal pin 14 (4,4 MHz)	$V_{14-8(p-p)}$	0,3	0,4	–	V
d.c. level	V_{14-8}	5,0	5,5	–	V
Suppression of 2,2 MHz and 6,6 MHz	α_{14}	30	35	–	dB
Suppression of 8,8 MHz	α_{14}	12	14	–	dB
Output resistance	R_{14-8}	–	V_T/I_C	–	Ω
Output signal pin 17 (4,4 MHz)	$V_{17-8(p-p)}$	0,3	0,4	–	V
d.c. level	$V_{17-8(p-p)}$	6,0	6,5	–	V
Output resistance	R_{17-8}	–	V_T/I_C	–	Ω
Divider and limiter					
Output signal pin 16	$V_{16-8(p-p)}$	2,5	3	–	V
d.c. level	V_{16-8}	3,5	4	–	V
Output resistance	R_{16-8}	–	V_T/I_C	–	Ω
Input for playback/record switching					
Input voltage record	V_{6-8}	0	–	5	V
Input voltage playback	V_{6-8}	7	–	V_P	V
Identification					
Output voltage pin 1 (open collector of pnp transistor) in SECAM mode	V_{1-8}	9,3	–	–	V
Output current pin 1 in SECAM mode	$-I_1$	3	–	–	mA
Output current pin 1 in NOT SECAM mode	$-I_1$	–	–	1	μA
Charge capacitor for ident integration	C_{2-8}	100	–	1000	nF
Threshold colour forced on	V_{2-8}	8	–	V_P	V
Threshold killer forced on	V_{2-8}	5,8	–	6,2	V
Identification input voltage pin 3	$V_{3-8(p-p)}$	0,22	–	1	V
Identification input voltage pin 4	$V_{4-8(p-p)}$	0,22	–	1	V
Input resistance pins 3,4	$R_{3,4-8}$	14	18	22	kΩ
Sandcastle input pin 18					
Input voltage for inactive discriminating stage	V_{18-8}	0	–	4,8	V
Input voltage for active discriminating stage	V_{18-8}	6	–	V_P	V

FREQUENCY DEMODULATOR AND DROP OUT COMPENSATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3730 is a monolithic integrated circuit for luminance processing in the playback path of video recorders. The device incorporates two signal channels, one for the main signal and one for the drop out signal.

Features

- FM preamplifier
- Limiter in main and drop out channel
- Demodulator in main and drop out channel
- Drop out detector with Schmitt-trigger
- Electronic switches for FM and video signal controlled by drop out detector
- Linear and dynamic video de-emphasis
- D.C. reference stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 7 and pin 23)	$V_P = V_{7,\ 23\text{-}5,\ 25}$	typ.	10 V
Supply current (pin 7 + pin 23)	$I_P = I_7 + I_{23}$	typ.	40 mA
FM input signal (pin 17) (peak-to-peak value)	$V_{17\text{-}25(p\text{-}p)}$	typ.	100 mV
Video output signal (pin 26) (peak-to-peak value)	$V_{26\text{-}5(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

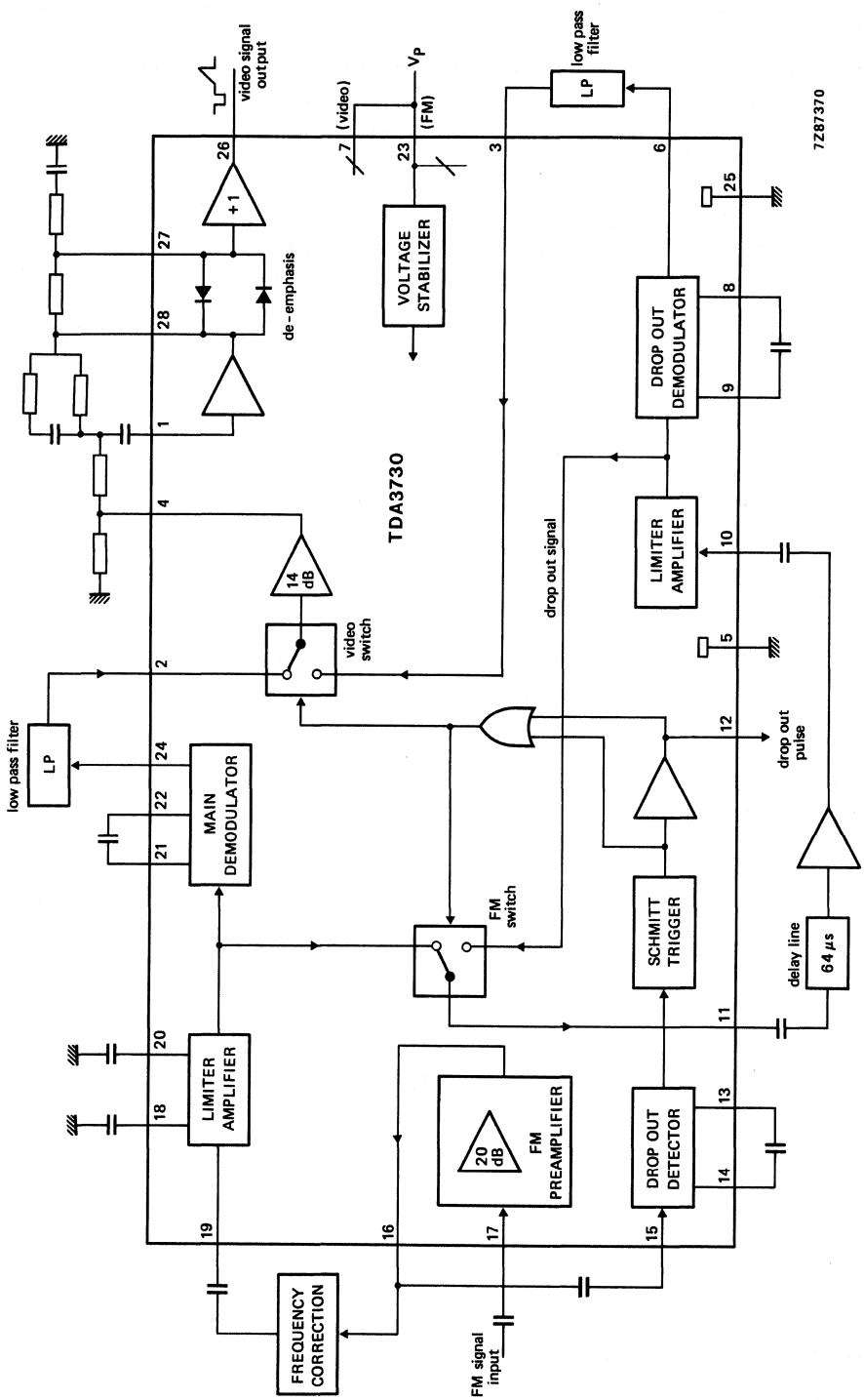


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 7 and 23)	$V_P = V_{7,23-5,25}$	max.	13,2 V
Voltage range at pins 1, 2, 3, 4, 5, 6, 10, 11, 12, 15, 16, 17, 18, 19, 20, 24, 26 to pin 5 and 25 (ground)	$V_{n-5,25}$		0 to V_P V
Voltage at pins 8, 9, 13, 14, 21, 22 to pin 5 and 25 (ground)	$V_{n-5,25}$	max.	V_P V
Voltage at pins 27, 28 to pin 5 and 25 (ground)	$V_{n-5,25}$	min.	0 V
Currents			
at pins 8, 9, 13, 14, 21, 22	$-I_n$	max.	3 mA
at pins 27 and 28	I_n	max.	3 mA
Total power dissipation	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

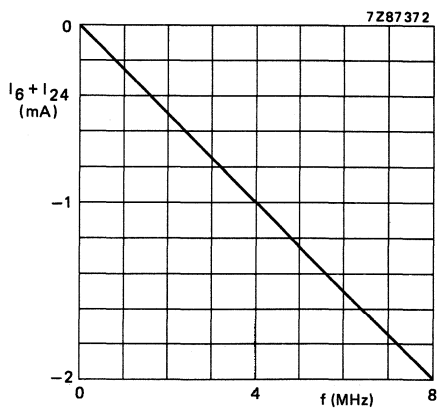


Fig. 2 Steepness of the main and drop out demodulator.

CHARACTERISTICS

$V_P = V_{7, 23\text{-}5, 25} = 10$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7 and pin 23)					
Supply voltage	$V_P = V_{7, 23\text{-}5, 25}$	9,6	10	13,2	V
Supply current	$I_{P1} = I_7$	–	23	–	mA
	$I_{P2} = I_{23}$	–	17	–	mA
FM amplifier					
Input voltage (pin 17) (peak-to-peak value)	$V_{17\text{-}25(p\text{-}p)}$	–	100	–	mV
Input resistance	$R_{17\text{-}25}$	10	–	–	kΩ
Gain	G_v	–	20	–	dB
Bandwidth ($R_G \leqslant 50\ \Omega$)	B	–	12	–	MHz
Output signal amplitude (pin 16) (peak-to-peak value)	$V_{16\text{-}25(p\text{-}p)}$	–	–	1,3	V
Main limiter amplifier (pin 19)					
FM input signal (peak-to-peak value)	$V_{19\text{-}25(p\text{-}p)}$	–	0,5	1	V
Input resistance	$R_{19\text{-}25}$	–	600	–	Ω
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{19\text{-}25(p\text{-}p)}$	–	–	2,5	mV
Drop out limiter amplifier (pin 10)					
FM input signal (peak-to-peak value)	$V_{10\text{-}5(p\text{-}p)}$	–	–	0,8	V
Input resistance	$R_{10\text{-}5}$	–	1	–	kΩ
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{10\text{-}5(p\text{-}p)}$	–	–	80	mV
Main and drop out demodulators					
Range of output voltages (pin 6 and pin 24) (peak-to-peak value)	$V_{6, 24\text{-}5, 25(p\text{-}p)}$	–	–	3,5	V
Linearity (bandwidth = 1 to 6 MHz)		–5	–	+5	%
Steepness (see Fig. 2)	S	–	0,25	–	mA/MHz
FM switch (pin 11)					
Output amplitude (peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	–	0,5	–	V
D.C. output voltage	$V_{11\text{-}5}$	–	8,4	–	V

parameter	symbol	min.	typ.	max.	unit
Video switch (pin 4)					
Input voltage (pin 2 and pin 3) (peak-to-peak value)	$V_{2,\,3\text{-}5(p\text{-}p)}$	–	–	0,5	V
Input resistance (open base)	$R_{2,\,3\text{-}5}$	20	–	–	kΩ
Voltage gain	G_v	–	14	–	dB
D.C. output voltage at $V_{2,\,3\text{-}5}$ = 9,5 V	$V_{4\text{-}5}$	–	5,4	–	V
De-emphasis amplifier (linear)					
Video output signal (pin 28) (peak-to-peak value)	$V_{28\text{-}5(p\text{-}p)}$	–	–	3	V
Gain-bandwidth product	G.B.	30	–	–	MHz
D.C. output voltage	$V_{28\text{-}5}$	–	4,8	–	V
Dynamic de-emphasis					
Output signal (pin 26) (peak-to-peak value) at $V_{28\text{-}5(p\text{-}p)}$ = 1 V; f = 1 MHz sine	$V_{26\text{-}5(p\text{-}p)}$	–	632	–	mV
D.C. output voltage	$V_{26\text{-}5}$	–	3,4	–	V
Output current (emitter follower)	$-I_{26}$	–	–	5	mA
Drop out detector and Schmitt-trigger					
Input voltage for lower drop out threshold (pin 15) (peak-to-peak value)	$V_{15\text{-}5(p\text{-}p)}$	–	110	–	mV
Hysteresis of the Schmitt-trigger	V/V	–	1,5	–	dB
Input resistance	$R_{15\text{-}5}$	1,4	–	–	kΩ
D.C. output voltage without drop out	$V_{12\text{-}5}$	–	–	2	V
D.C. output voltage with drop out	$V_{12\text{-}5}$	5	–	–	V
OR-gate (internal)					
Switching voltage threshold (pin 12) for signal flow from pin 2 to pin 4	$V_{12\text{-}5}$	–	–	1,5	V
for signal flow from pin 3 to pin 4	$V_{12\text{-}5}$	3	–	–	V

APPLICATION INFORMATION

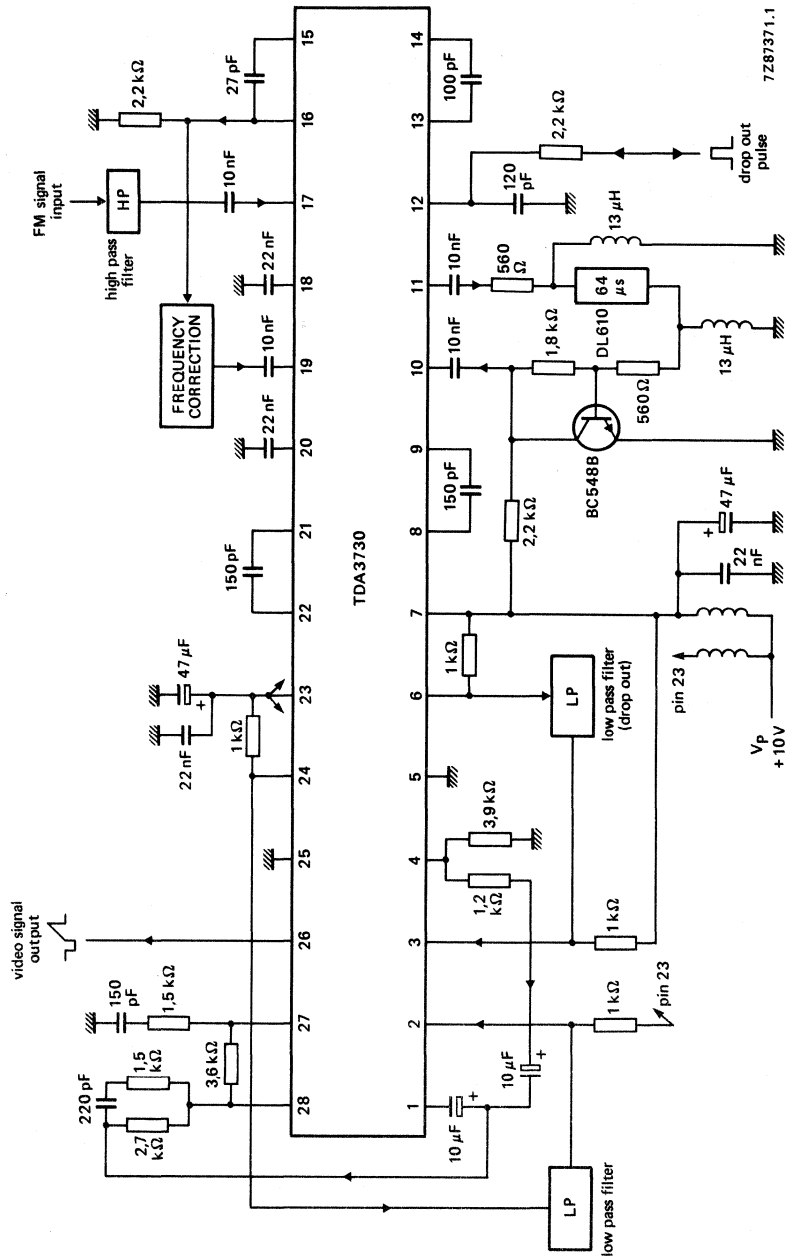


Fig. 3 Application diagram; also used as test circuit.

VIDEO PROCESSOR AND FREQUENCY MODULATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3740 is a monolithic integrated circuit for video signal processing and frequency modulation in video recorders.

Features

- Video controlled amplifier with clamping stage
- Fast and slow white amplitude detector
- Sync amplitude detector
- Black and white clip
- Insertion of sync and composite video signals
- Adder stage for composite video and chrominance signals
- Two-stage amplification for the composite video signal with dynamic (adjustable) and linear pre-emphasis
- White clip with external determination of clipping level
- Voltage controlled oscillator (frequency modulator)
- Blanking stage for the voltage controlled oscillator and limiter amplifier
- Reference voltage source

QUICK REFERENCE DATA

Supply voltage (pin 18, 28)	$V_P = V_{18,28-27}$	typ.	10 V
Supply current (pin 18, 28) (record mode)	$I_P = I_{18,28}$	typ.	58 mA
Supply current (pin 18) (playback mode)	$I_P = I_{18}$	typ.	28 mA
Composite video input signal (peak-to-peak value)	$V_{3-27(p-p)}$	typ.	350 mV
Composite colour video output signal (peak-to-peak value)	$V_{7-27(p-p)}$	typ.	2 V
Chrominance input signal (peak-to-peak value)	$V_{9-27(p-p)}$	typ.	240 mV
Output current (pin 22, 23)	$I_{22,23}$	typ.	8,5 mA

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

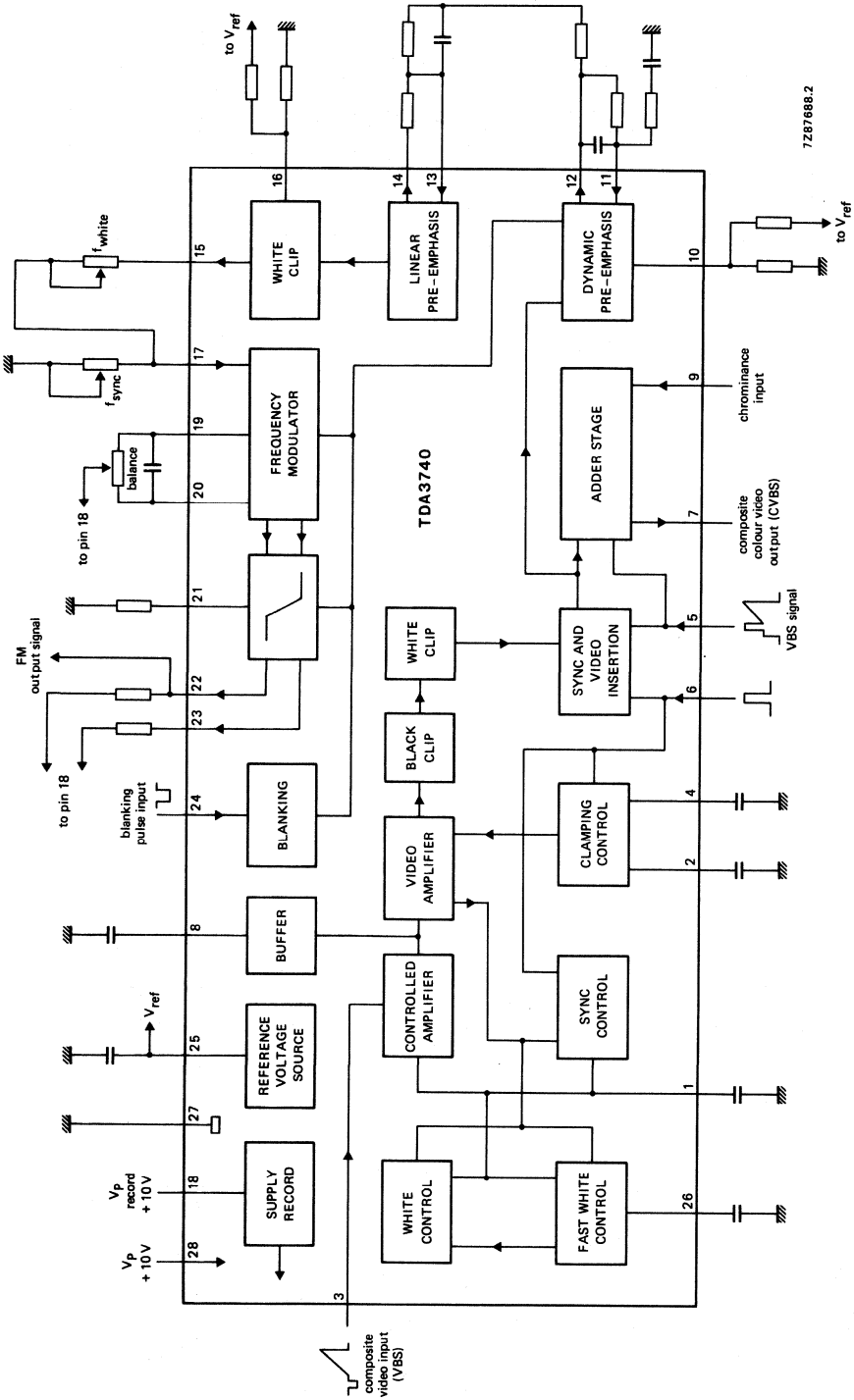


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18, 28) $V_P = V_{18,28-27}$ max. 13,2 V

With pin 27 connected to ground and pin 18 and 28 to supply voltage (V_P) all voltages between 0 and V_P are allowed.

Total power dissipation	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}		−25 to +150 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

CHARACTERISTICS

$V_P = V_{18-28} = 10$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 18, 28)					
Supply voltage	$V_P = V_{18,28-27}$	9	10	13,2	V
Supply current					
at record (FM kill inactive)	$I_P = I_{18,28}$	–	58	–	mA
at playback	$I_P = I_{28}$	–	28	–	mA
Controlled amplifier					
Composite video input signal (peak-to-peak value)	$V_{3-27(p-p)}$	0,20	0,35	0,62	V
Video signal control range (referred to 0,35 V input signal at pin 3)	α_{3-27}	±5	±6	–	dB
Input resistance	R_{3-27}	7	10	13	kΩ
Input capacitance	C_{3-27}	–	–	10	pF
Composite colour video output signal (peak-to-peak value)	$V_{7-27(p-p)}$	1,9	2	2,1	V
Frequency response (0 to 3 MHz)	α_{7-3}	−0,5	–	0,5	dB
Sync recovering and insertion of composite video signal					
Threshold voltage for sync recovering	V_{6-27}	3,0	3,5	4,0	V
Input resistance	R_{6-27}	100	–	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Insertion of composite video signal					
insertion inactive	V_{5-27}	0	–	0,9	V
video + chroma mute	V_{5-27}	2,5	–	3,0	V
insertion black level	V_{5-27}	3,1	3,25	3,4	V
insertion white level (90% CVBS)	V_{5-27}	3,7	4,0	4,3	V
Input resistance	V_{5-27}	100	–	–	kΩ
Gain	G_{7-5}	2,9	4,5	6,5	dB
Frequency response (0 to 5 MHz)	α_{7-5}	–	–	3	dB
Signal suppression pin 7 at mute		−40	–	–	dB
Clamping control					
Duration of clamping pulse (note 1) with C_{2-27} = 100 nF; C_{4-27} = 2,2 nF	t_d	1	3	4,5	μs
Max. leakage current of external capacitor	I_{L2}	–	–	1	μA
Black and white clip					
Black clip relative to black level	ΔV_{7-27}	−40	−25	0	mV
White clip at pin 7 (referred to nominal VBS)		103	105	107	%
Chrominance signal adder and output stage					
Burst input signal (peak-to-peak value)	$V_{9-27(p-p)}$	–	240	400	mV
Input resistance	R_{9-27}	4	5,6	–	kΩ
D.C. level of top sync	V_{7-27}	2,4	2,7	3,0	V
Sync amplitude at CVBS output pin 7	$V_{7-27(p-p)}$	570	600	630	mV
Gain (f = 4,43 MHz)	G_{7-9}	7	8	9	dB
Output resistance	R_{7-27}	–	–	30	Ω
Frequency response (0 to 5 MHz)	α_{7-9}	−0,5	–	+0,5	dB
Dynamic and linear pre-emphasis; white limiter					
Input resistance pin 11	R_{11-27}	15	–	–	kΩ
Output resistance (emitter follower with internal current source)	R_{12-27}	–	–	30	Ω
Gain-bandwidth product					
dynamic ($V_{24-27} = V_P$)		24	36	–	MHz
linear		30	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Range of dynamic pre-emphasis (fixed by external resistors at pin 10)	$V_{10\text{-}27}$	0	–	2,5	V
Gain adjustment range at 1 MHz and $V_{7\text{-}27}$ = 632 mV	$G_{12\text{-}7}$	1,5	–	8	dB
Output resistance (emitter follower with internal current source)	$R_{14\text{-}27}$	–	–	30	Ω
White clip level deviation relative to $V_{16\text{-}27}$ = 1,5 V	$V_{16\text{-}15}$	75	–	125	mV
Range of clipping determination (note 2)	$V_{16\text{-}27}$	1	–	3	V
Frequency modulator					
D.C. level at pin 21 (note 3)	$V_{21\text{-}27}$	1,8	1,9	2,0	V
FM output voltage (note 3) $R_{21\text{-}27}$ = 1,5 kΩ, $R_{22,\ 23\text{-}18}$ = 470 Ω	$V_{22,\ 23\text{-}27}$	–	660	–	mV
Slope between 3 MHz and 6 MHz	$\frac{\Delta f_{22,23}}{\Delta I_{17}}$	–	10,5	–	$\frac{KHz}{\mu A}$
Linearity between 3 MHz and 6 MHz	m	95	–	–	%
Suppression of the 2nd harmonic referred to the 1st harmonic 3,8 MHz (balanced)	α_{harm}	40	46	–	dB
Frequency drift dependent on: drift of supply voltage (V_P = 9 – 13,2 V)	$\frac{\Delta f_{22,23}}{\Delta V_P}$	–	5	10	$\frac{KHz}{V}$
drift of ambient temperature (T_{amb} = 0 – 70 °C) at 3,8 MHz	$\Delta f_{22,23}$	–85	–	+85	kHz
at 4,8 MHz	$\Delta f_{22,23}$	–85	–	+85	kHz
Drift of frequency span dependent on temperature drift (T_{amb} = 0 – 70 °C)	Δf	–70	–	+70	kHz
Input voltage to switch FM off	$V_{24\text{-}27}$	–	–	2	V
Input voltage to switch FM on	$V_{24\text{-}27}$	3	–	–	V
Input resistance	$R_{24\text{-}27}$	10	–	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Reference voltage source (pin 25)					
Output voltage	$V_{25\text{-}27}$	–	5,5	–	V
Output current (additional to application)	I_{25}	–3	–	+5	mA
Output voltage drift dependent on drift of supply voltage (V_P = 9 – 13,2 V)	$\frac{\Delta V_{25\text{-}27}}{\Delta V_P}$	–10	–	+10	$\frac{mV}{V}$
drift of ambient temperature (T_{amb} = 0 – 70 °C)	$\Delta V_{25\text{-}27}$	–90	–	+90	mV

Notes

1. Duration of clamping pulse is determined by $C_{4\text{-}27}$ as follows: t_d (μs) = 1,364 . $C_{4\text{-}27}$ (nF).
2. White clipping level is fixed by the external resistors at pin 16, e.g. $R_{16\text{-}25}$ = 3,3 kΩ and $R_{16\text{-}27}$ = 2 kΩ results in 160% clipping level.
3. FM output amplitude at pins 22 and 23 is determined by the external fixed resistors $R_{21\text{-}27}$, $R_{22\text{-}18}$ and $R_{23\text{-}18}$.

DEVELOPMENT DATA

APPLICATION INFORMATION

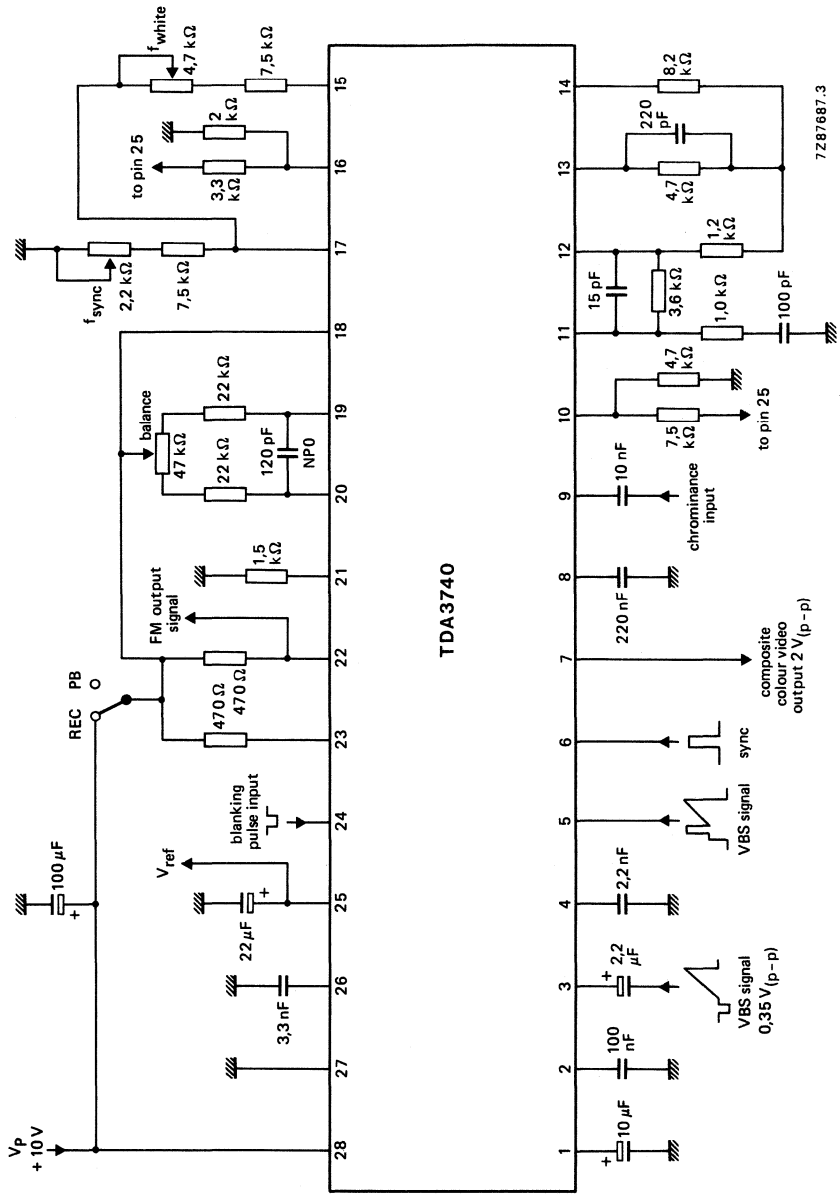


Fig. 2 Application diagram; also used as test circuit.

REC = record.
PB = playback.

PAL/NTSC/SECAM SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3755 is a monolithic integrated circuit for PAL/NTSC SECAM synchronization processing in VHS video recorders.

Features

- Adaptive sync separator
- Internal vertical sync pulse integrator
- Composite sync and vertical pulse output
- Current controlled oscillator (CCO) with 320/321 times horizontal frequency
- Horizontal phase detector with current output
- Video identification and mute circuit
- Burst gating pulse output (externally adjustable phase relationship)
- Test-picture output
- Subcarrier frequency output switched in phase in accordance with VHS standard
- Fast phase correction of subcarrier frequency
- Selection input to force PAL or NTSC function
- Still picture input

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13\text{-}15}$	typ.	10 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	24 mA
Sync separator			
Sync pulse input voltage (peak-to-peak value)	$V_{3\text{-}15(p\text{-}p)}$	typ.	300 mV
Sync pulse output voltage (peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	min.	7,3 V
Vertical sync pulse			
Output voltage (peak-to-peak value)	$V_{18\text{-}15(p\text{-}p)}$	min.	2,7 V
Phase detector			
Catching range	Δf	min.	± 3,0 %
Oscillator			
Oscillator frequency			
PAL	f_{osc}	typ.	5,02 MHz
NTSC	f_{osc}	typ.	5,04 MHz
Output frequency			
PAL	f_o	typ.	627 kHz
NTSC	f_o	typ.	629 kHz
Output sinewave (peak-to-peak value)	$V_{8\text{-}15(p\text{-}p)}$	typ.	3 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

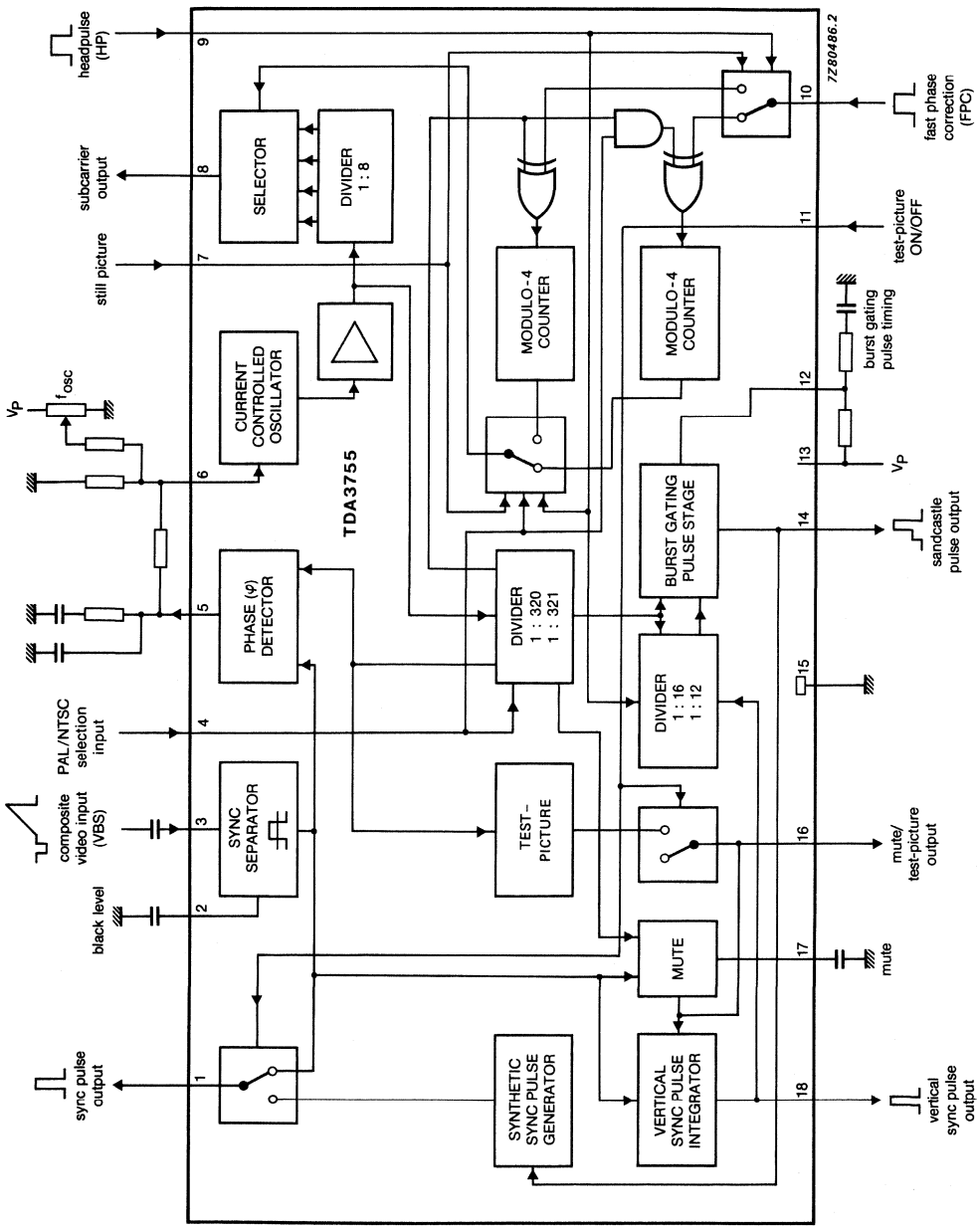


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-15}$	max.	13,2	V
Voltage range at pins 2, 3, 4, 7, 9, 10, 11, 17 to pin 15 (ground)	V_{n-15}		0 to V_P	V
Voltage range at pin 12	V_{12-15}	min.	0	V
Voltage range at pin 6	V_{6-15}	max.	8	V
Currents				
at pins 1, 5, 8, 14, 16, 18	$\pm I_n$	max.	5	mA
at pin 6	$-I_6$	max.	1	mA
at pin 12	I_{12}	max.	2	mA
Total power dissipation	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-15}$	9,6	–	13,2	V
Supply current	$I_P = I_{13}$	–	24	–	mA
Sync separator (pin 3)					
Colour composite video input voltage (note 1) (peak-to-peak value)	$V_{3-15(p-p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{3-15(p-p)}$	75	–	600	mV
Slicing level, relative to sync pulse amplitude (note 2)		–	50	–	%
Internal resistance of video source	R_G	–	–	1	kΩ
Sync output voltage HIGH at $-I_1$ = 1 mA	V_{1-15}	7,8	–	–	V
Sync output voltage LOW at I_1 = 1 mA	V_{1-15}	–	–	0,5	V
Delay between signal at input pin 3 and sync pulse at output pin 1	t_d	–	0,2	–	μs
Vertical sync pulse (pin 18; note 3)					
Output voltage HIGH at $-I_{18}$ = 1 mA	V_{18-15}	2,7	–	5,0	V
Output voltage LOW at I_{18} = 1,6 mA	V_{18-15}	–	–	0,5	V
Duration of HIGH state of internally generated output pulse	t_p	–	190	–	μs
Delay between leading edge of input signal at pin 3 and leading edge of output pulse at pin 18	t_d	32	–	64	μs
Selection input (pin 4)					
Input voltage for NTSC state	V_{4-15}	–	–	0,3	V
Input current at V_{4-15} = 0 V	$-I_4$	–	–	20	μA
Input voltage for PAL state pin 4 open circuit or	V_{4-15}	2	–	–	V

parameter	symbol	min.	typ.	max.	unit
Test picture/mute/synthetic sync pulse					
Minimum voltage at pin 11 for test picture mode **active** (note 4)	V_{11-15}	4,8	–	–	V
Maximum voltage at pin 11 for test picture mode **inactive**	V_{11-15}	–	–	3,8	V
Output voltage at pin 16					
at test picture "black" or at mute	V_{16-15}	–	2,75	–	V
at test picture "white"	V_{16-15}	–	4,50	–	V
at "in sync condition"	V_{16-15}	–	–	0,5	V
Input current (pin 11)	$-I_{11}$	–	–	25	μA
Oscillator/phase detector					
Oscillator frequency (note 5)					
PAL	f_{osc}	–	5,02	–	MHz
NTSC	f_{osc}	–	5,04	–	MHz
Oscillator conversion gain	k_o	–	16,13	–	MHz/mA
D.C. control voltage	V_{6-15}	–	2,1	–	V
Input current for f = 5,016 MHz	$-I_{16}$	–	310	–	μA
Holding range (note 6)	Δf	± 3,2	–	–	%
Catching range (note 6)	Δf	± 3,0	–	–	%
Control loop gain	k_v	–	380 x 10^3	–	s^{-1}
Output of lower subcarrier (note 7) (peak-to-peak value)	$V_{8-15(p-p)}$	–	3	–	V
Output current	I_8	–	–	2	mA
D.C. output voltage	V_{8-15}	–	3,1	–	V
2nd harmonic suppression without switching	α_{2nd}	20	–	–	dB
Switching position prior to centre of sync pulse (pin 3)	t_s	–	2	–	μs
Output peak current of phase detector during sync pulse	$\pm I_5$	–	3,78	–	mA
Output voltage range (note 8)	V_{5-15}	1,4	–	2,8	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 14; note 9)					
Output voltage HIGH (note 10) at $-I_{14}$ = 1 mA	V_{14-15}	7,8	–	–	V
Output voltage INTERMEDIATE at $-I_{14}$ = 1 mA	V_{14-15}	2,3	3,0	3,7	V
Output voltage LOW at I_{14} = 1 mA	V_{14-15}	–	–	0,5	V
Lower part is starting prior to the centre of sync pulse at pin 3 and ending with the upper part	t_{14-3}	–	2,6	–	μs
Fast phase correction/head pulse					
Threshold voltage for fast phase correction (note 11)	V_{10-15}	–	7,2	–	V
Input current	$-I_{10}$	–	–	20	μA
Threshold voltage of head pulse input	V_{9-15}	–	1,4	–	V
Input current	$-I_9$	–	–	20	μA
D.C. input voltage	V_{7-15}	–	5,6	–	V
Input resistance	R_{7-15}	3	–	–	kΩ
Subcarrier phase switching (note 12)					
Phase switching of subcarrier phase in accordance with head pulse if	V_{7-15}	–	5,6*	–	V
LOW state of still picture input	V_{7-15}	–	–	0,5	V
Continuous phase switching regardless of head pulse if	V_{7-15}	–	V_P	–	V

* Or not connected.

Notes to characteristics

1. The sync separator input signal is shown in Fig. 2.

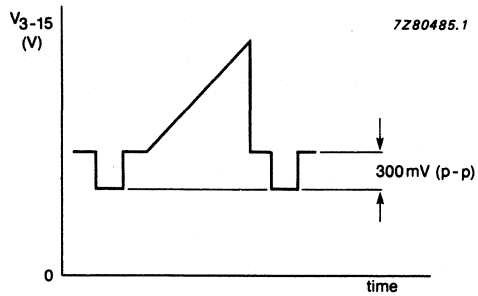
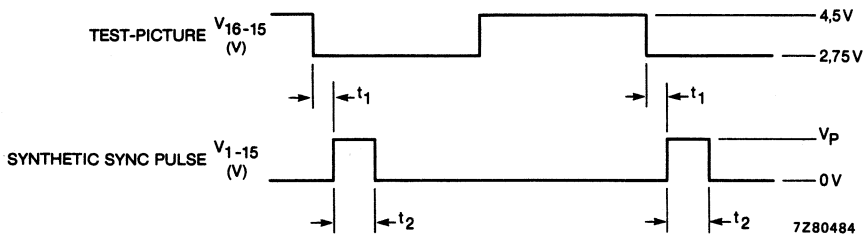


Fig. 2 Colour composite video input signal at pin 3.

2. The black level and the top sync level are detected internally and stored in capacitors at pin 2 and pin 3 respectively.
3. The vertical sync pulse output is disabled by mute.
4. In test picture mode the synthetic sync pulse is fed to output pin 1 and the vertical pulse consists of an uninterrupted block pulse of 192 μs triggering at every transition of head pulse (HP) at pin 9. The timing of test picture and synthetic sync pulse is shown in Fig. 3.



Where: The value of t_1 is dependent upon adjustment of the burst gating pulse delay.
Time t_2 is the burst gating pulse duration.

Fig. 3 Timing of test picture and synthetic sync pulse.

5. Oscillator adjustment during test picture mode made only, at $V_{11-15} > 4{,}8$ V, $V_{7-15} = 0$ V and $V_{4-15} > 2$ V or open circuit; measurement is $f_{osc}/8$ at output pin 8.
6. The holding range and catching range are both determined by the resistor connected between pin 5 and pin 6.
7. The phase of the lower subcarrier is switched in accordance with the VHS standard. PNP emitter follower, internal resistive load of 10 kΩ (typ.) to V_P.
8. The output voltage at pin 5 is disabled during test picture mode.

Notes to characteristics (continued)

9. The burst gating pulse is superimposed on an uninterrupted horizontal pulse. It is suppressed 16 times starting with every transition of the head pulse at pin 9. If a vertical pulse is detected during that time the burst gating pulses are additionally suppressed until line 12 and line 324 respectively. In any event the number of suppressed burst gating pulses is even.
10. The timing of the upper part of the sandcastle pulse is determined by the components connected to pin 12 (Fig. 4) and is independent of supply voltage variations.
11. The fast phase correction pulses have to be in the burst gating reference pulse. For any HIGH to LOW transitions of the correction pulse the phase is corrected by -90^{o} if the head pulse input is LOW and by $+90^{o}$ if the head pulse input is HIGH.
12. Subcarrier phase switching is detailed in Table 1.
    Subcarrier is 40,000 x f_H for NTSC state and 40,125 x f_H for PAL state.

Table 1 Subcarrier phase switching

still picture input	PAL		NTSC	
	HP = HIGH	HP = LOW	HP = HIGH	HP = LOW
HIGH	-90^{o}	-90^{o}	-90^{o}	-90^{o}
not connected	0^{o}	-90^{o}	$+90^{o}$	-90^{o}
LOW	0^{o}	0^{o}	$+90^{o}$	$+90^{o}$

APPLICATION INFORMATION

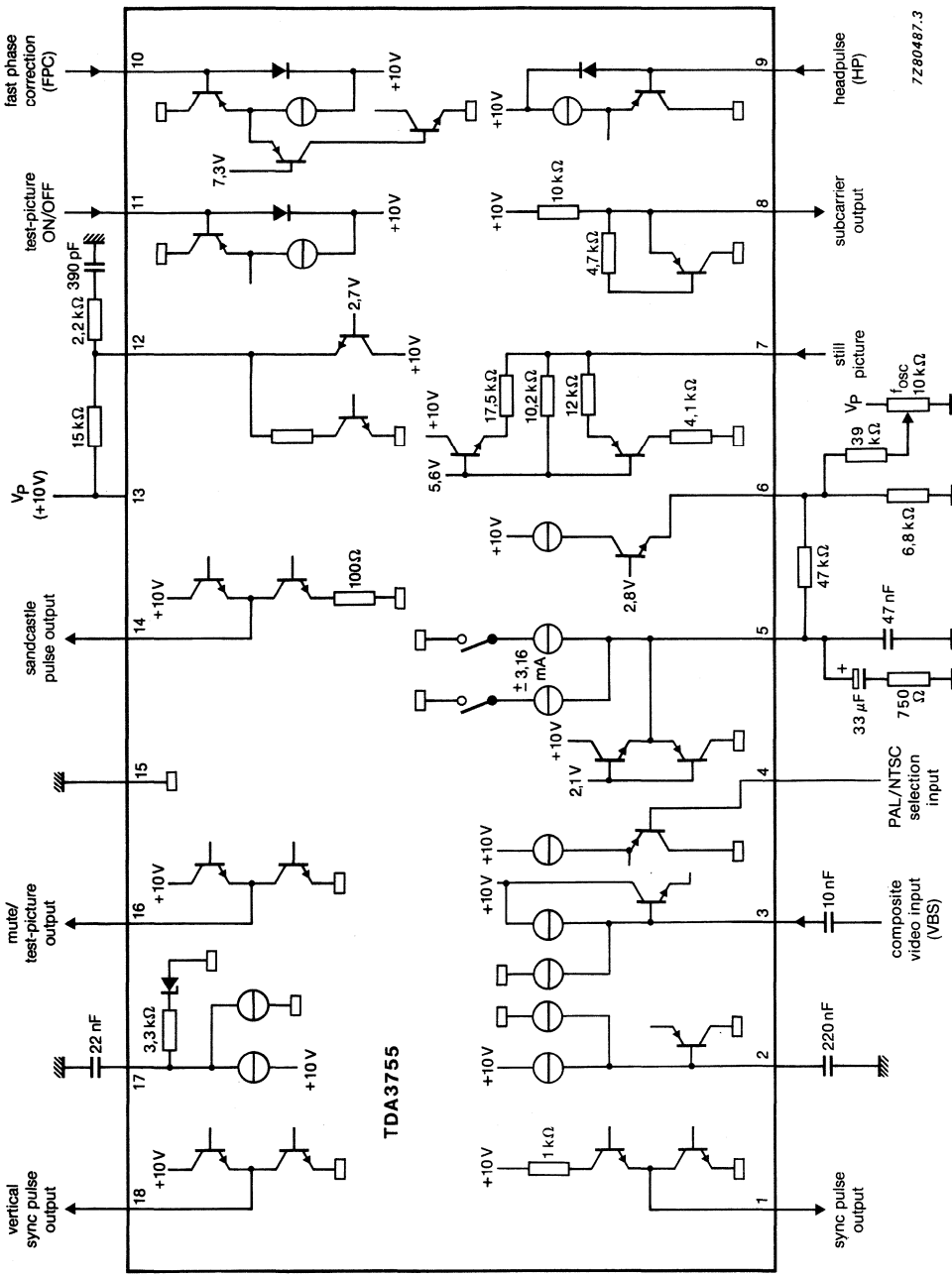


Fig. 4 Application circuit diagram.

PAL CHROMINANCE SIGNAL PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3760 is a monolithic integrated circuit for chrominance signal processing in video recorders.

Features

- Automatic gain controlled pre-amplifier with record/playback selection
- Signal mixer with balancing stage
- Output stage for the 627 kHz chrominance signal, with facility for being disabled by colour killer and record/playback mode switch
- Amplitude detector with automatic gain control for the preamplifier
- 4,43 MHz voltage controlled oscillator (VCO) for recording and playback
- 4,43 MHz fixed oscillator for playback
- Phase detector controlled synchronization of the VCO
- Subcarrier mixer
- H/2 demodulator for the production of PAL identification and colour killing signals
- Flip-flop for PAL identification
- Sandcastle pulse processing
- Colour killing stage with hysteresis
- Internal record/playback selection
- Second phase detector for fast phase correction of sub-carrier

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_P = V_{9\text{-}15}$	typ.	10 V
Supply current (pin 9)	$I_P = I_9$	typ.	45 mA
Inputs			
Chrominance signal			
4,43 MHz for record (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	typ.	200 mV
627 kHz for playback (peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	typ.	200 mV
Outputs			
Chrominance signal			
4,43 MHz (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	typ.	490 mV
627 kHz (peak-to-peak value)	$V_{26\text{-}15(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

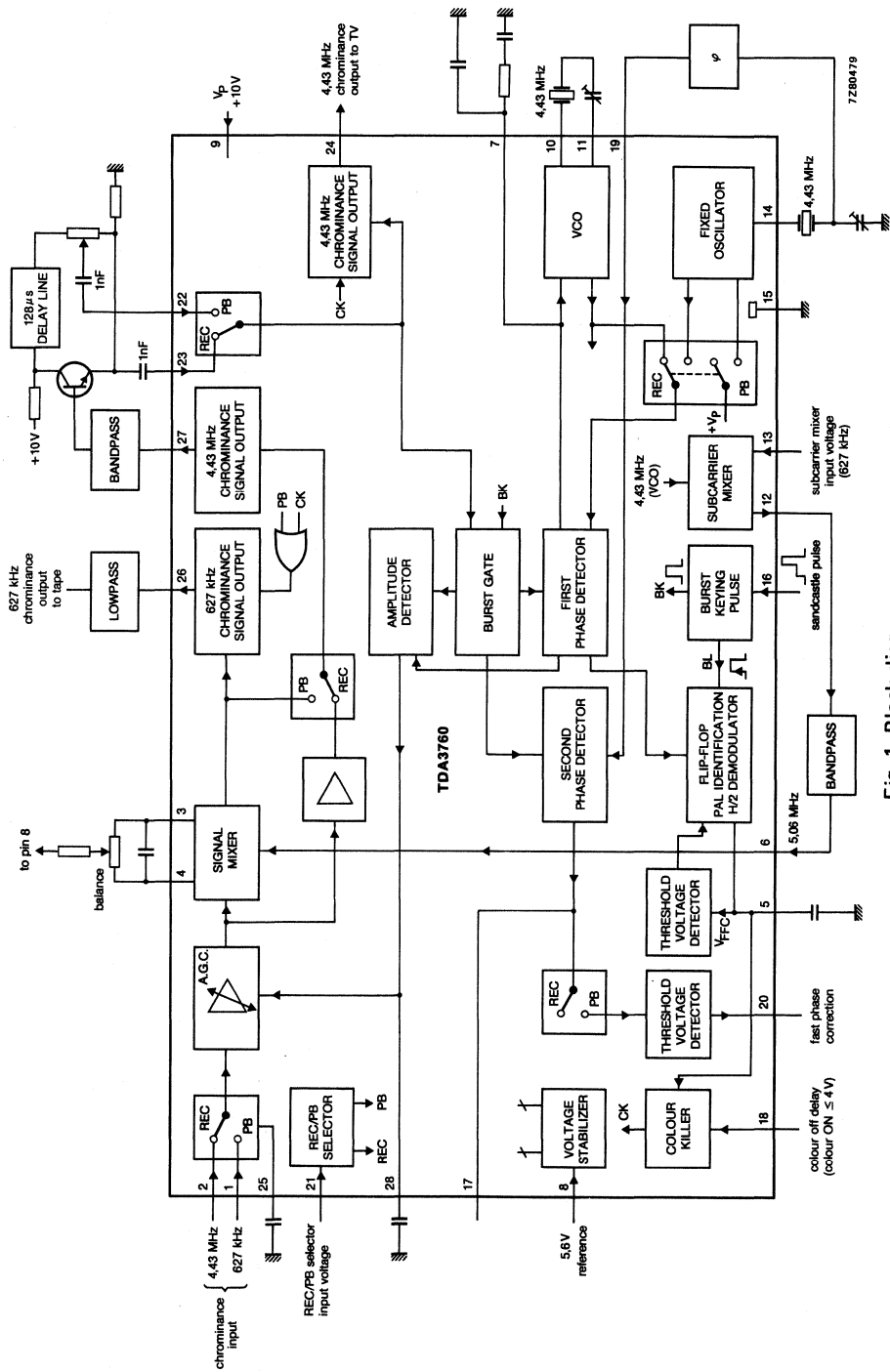


Fig. 1 Block diagram.

BK = burst key pulse
BL = blanking pulse
FFC = flip-flop correction
FPC = fast phase correction

REC = record
PB = playback
CK = colour killer

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_P = V_{9-15}$	max.	13,2	V
Voltage range at pins 1, 2, 5, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23 to pin 15 (ground)	V_{n-15}		0 to V_P	V
Voltage ranges				
at pins 3, 4, 28*	$V_{3, 4, 28-15}$		3 to 6	V
at pin 6, 25*	$V_{6, 25-15}$		0 to 5	V
at pin 10*	V_{10-15}		1,5 to 4	V
at pin 13*	V_{13-15}		0 to 3	V
at pin 14*	V_{14-15}		0 to 8	V
Voltages				
at pin 12	V_{12-15}	max.	V_P	V
at pin 24	V_{24-15}	max.	7	V
Currents				
at pins 11, 18	$-I_{11, 18}$	max.	2	mA
at pins 12, 26, 27	$-I_{12, 26, 27}$	max.	5	mA
at pin 24	$-I_{24}$	max.	3	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

* Measured with $V_{8-15} = 5,6$ V

CHARACTERISTICS

$V_P = V_{9-15} = 10$ V; $V_{8-15} = 5{,}6$ V; $T_{amb} = 25$ °C; burst key duration 4 μs; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 9)					
Supply voltage	$V_P = V_{9-15}$	9,6	–	13,2	V
Supply current for playback and burst keying					
at $-I_{12, 18, 24, 26, 27} = 0$	$I_P = I_9$	–	45	–	mA
at $-I_{12, 18, 24, 26, 27} = 0$; $V_P = 12$ V	$I_P = I_9$	–	46	–	mA
A.G.C. preamplifier (pins 1 and 2)					
Input voltage* (f = 4,43 MHz) during record (peak-to-peak value)	$V_{2-15(p-p)}$	20	–	400	mV
Input voltage* (f = 627 kHz) during playback (peak-to-peak value)	$V_{1-15(p-p)}$	30	–	400	mV
Input resistance	$R_{1, 2-15}$	7	–	–	kΩ
Input capacitance	$C_{1, 2-15}$	–	–	5	pF
627 kHz chrominance signal (pin 26)* (transposed on to 627 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-15(p-p)}$	–	2	–	V
Signal suppression at output					
for f = 1,25 MHz	α_{26}	–	35	–	dB
for f = 5,06 MHz (externally balanced via pins 3 and 4)	α_{26}	–	40	–	dB
during colour killing (pin 25)	α_{26}	40	–	–	dB
D.C. output voltage	V_{26-15}	–	6,7	–	V
4,43 MHz chrominance signal (pin 27)*					
Output voltage					
during record (peak-to-peak value)	$V_{27-15(p-p)}$	–	1,15	–	V
during playback after signal mixing (peak-to-peak value)	$V_{27-15(p-p)}$	–	–	3,1	V
Signal suppression at output					
for f = 5,06 MHz (externally balanced)	α_{27}	–	40	–	dB
for f = 8,86 MHz	α_{27}	–	30	–	dB
for f = 3,81 MHz	α_{27}	–	38	–	dB
for f = 3,18 MHz	α_{27}	–	30	–	dB
D.C. output voltage	V_{27-15}	–	7	–	V

* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	signal	min.	typ.	max.	unit
4,43 MHz chrominance signal amplifier*					
Burst input signal					
at pin 22 (peak-to-peak value)	$V_{22\text{-}15(p\text{-}p)}$	–	225	–	mV
at pin 23 (peak-to-peak value)	$V_{23\text{-}15(p\text{-}p)}$	–	225	–	mV
Input resistance					
at pin 22	$R_{22\text{-}15}$	6	–	–	kΩ
at pin 23	$R_{23\text{-}15}$	6	–	–	kΩ
Output voltage of the chrominance signal					
at pin 24 (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	–	490	–	mV
Signal suppression at output (pin 24)					
during colour killing	α_{24}	35	–	–	dB
D.C. output voltage					
during colour-on	$V_{24\text{-}15}$	–	2,4	–	V
during colour-off (killed)	$V_{24\text{-}15}$	–	0,7	–	V
Subcarrier mixer					
627 kHz input voltage; sine-wave					
(peak-to-peak value)	$V_{13\text{-}15(p\text{-}p)}$	220	–	–	mV
Input resistance	$R_{13\text{-}15}$	1	–	–	kΩ
D.C. output voltage	$V_{12\text{-}15}$	–	7,9	–	V
5,06 MHz output voltage selective**					
(peak-to-peak value)	$V_{12\text{-}15(p\text{-}p)}$	–	800	–	mV
Signal suppression at output**					
for f = 4,43 MHz	α_{12}	20	–	–	dB
for f = 5,68 MHz	α_{12}	30	–	–	dB
Subcarrier input					
5,06 MHz input voltage (peak-to-peak value)	$V_{6\text{-}15(p\text{-}p)}$	250	–	–	mV
Input resistance	$R_{6\text{-}15}$	1,9	–	–	kΩ
Input capacitance	$C_{6\text{-}15}$	–	–	5	pF

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Measured with a 0,32 V (peak-to-peak), 627 kHz input signal on pin 13 ($-I_{12}$ = 1 mA).

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
4,43 MHz voltage controlled oscillator (VCO)					
Input resistance	$R_{10\text{-}15}$	–	430	–	Ω
Input capacitance	$C_{10\text{-}15}$	–	–	10	pF
Output resistance	$R_{11\text{-}15}$	–	–	200	Ω
PLL-controlled oscillator catching range	Δf	± 500	–	–	Hz
Phase difference between oscillator and burst signal for ± 400 Hz deviation of crystal frequency	φ	± 7	–	–	deg
4,43 MHz fixed oscillator					
Oscillator temperature coefficient*	TC	–	–	–3	Hz/K
Record/playback selector (pin 21)					
Input voltage for record**	$V_{21\text{-}15}$	–	–	4	V
Input current with $V_{21\text{-}15}$ = 4 V	I_{21}	–	–	130	μA
Input voltage for playback	$V_{21\text{-}15}$	8	–	–	V
Input current with $V_{21\text{-}15}$ = 8 V	I_{21}	–	–	430	μA
Input resistance	$R_{21\text{-}15}$	7	–	–	kΩ
Colour (on/off) killer delay					
Delay for chrominance signal OFF at ΔV = 1 V; C = 1 μF; PNP emitter follower with internal current of 0,1 mA	t_d	–	10	–	ms
Input voltage (pin 18) for forced colour ON	$V_{18\text{-}15}$	–	–	4	V
for forced colour OFF	$V_{18\text{-}15}$	5,5	–	9	V
Voltage stabilizer (pin 8)					
Range of external reference voltage	$V_{8\text{-}15}$	5,3	–	5,8	V
Input current	$-I_8$	–	–	120	μA

* Not considering the effects of external components.

** Pin open: record.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse input (pin 16)					
Input voltage for burst keying	$V_{16\text{-}15}$	7,1	–	–	V
Input current	I_{16}	–	–	5	μA
Delay time of BK	t_d	–	0,55	–	μs
Input voltage for triggering of flip-flop	$V_{16\text{-}15}$	2	–	–	V
Fast phase correction					
Input voltage* (peak-to-peak value)	$V_{19\text{-}15(p\text{-}p)}$	200	–	400	mV
Input resistance	$R_{19\text{-}15}$	3,3	–	–	kΩ
Output voltage					
without correction					
below phase differences of ± 50°					
at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} < 6{,}5$ V	$V_{20\text{-}15}$	–	–	5,2	V
with correction					
above phase differences of ± 65°					
at $I_{20} < \pm$ 20 μA and $V_{17\text{-}15} > 7{,}1$ V	$V_{20\text{-}15}$	9	–	–	V
Output resistance	$R_{20\text{-}15}$	–	35	–	kΩ

* Phase difference between output pin 14 and input pin 19 should be $\varphi = 90°$.

APPLICATION INFORMATION

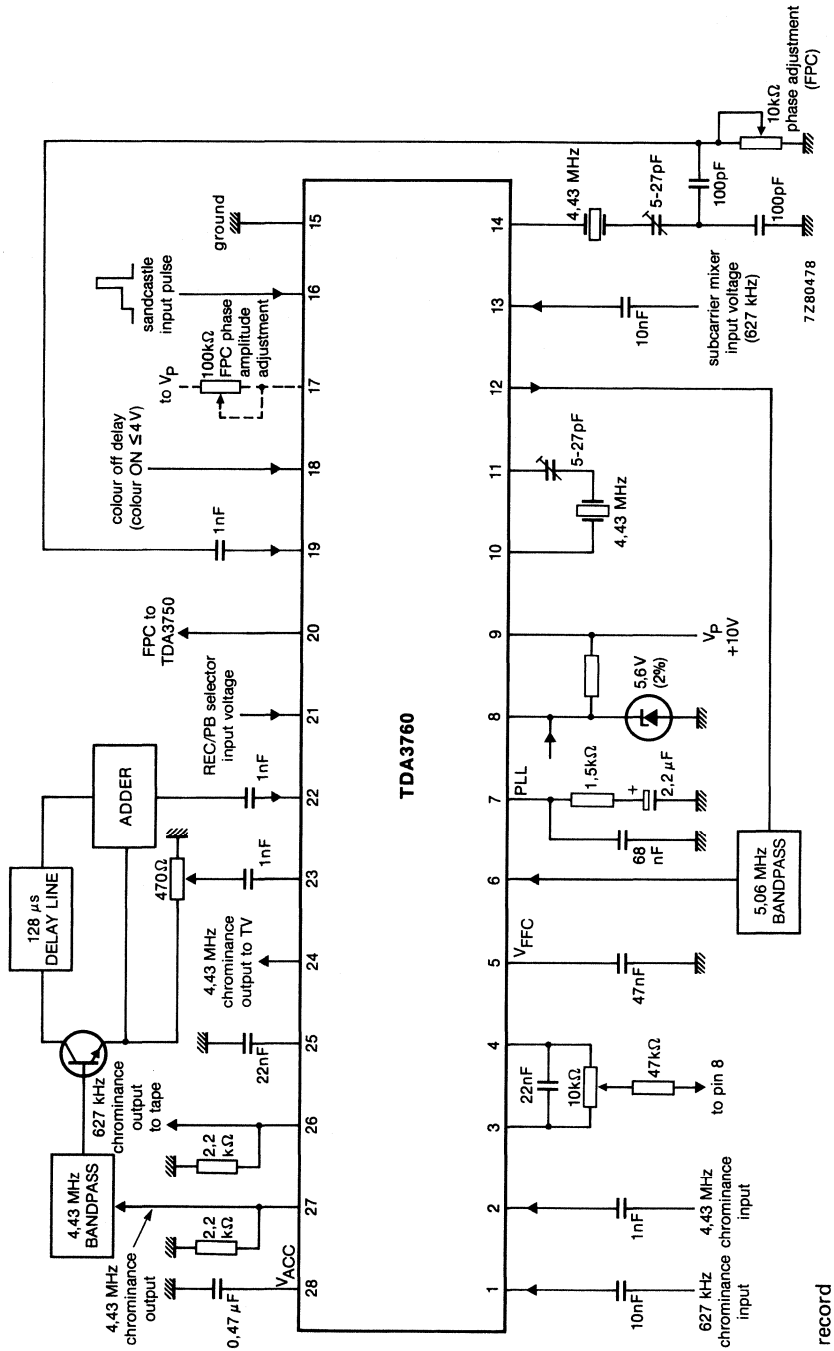


Fig. 2 Application diagram.

REC = record
PB = playback
FPC = fast phase correction
FFC = flip-flop correction

NTSC CHROMINANCE SIGNAL PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3765 is a monolithic integrated circuit for chrominance signal processing in video recorders.

Features

- Automatic gain controlled pre-amplifier with record/playback selection
- Signal mixer with balancing stage
- Output stage for the 629 kHz chrominance signal, with facility for being disabled by colour killer and record/playback mode switch
- Amplitude detector with automatic gain control for the preamplifier
- 3,58 MHz voltage controlled oscillator (VCO) for recording and playback
- 3,58 MHz fixed oscillator for playback
- Phase detector controlled synchronization of the VCO
- Subcarrier mixer
- Sandcastle pulse processing
- Colour killing stage with hysteresis
- Internal record/playback selection
- Second phase detector for fast phase correction of sub-carrier

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_P = V_{9\text{-}15}$	typ.	10 V
Supply current (pin 9)	$I_P = I_9$	typ.	45 mA
Inputs			
Chrominance signal			
3,58 MHz for record (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	typ.	200 mV
629 kHz for playback (peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	typ.	200 mV
Outputs			
Chrominance signal			
3,58 MHz (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	typ.	490 mV
629 kHz (peak-to-peak value)	$V_{26\text{-}15(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

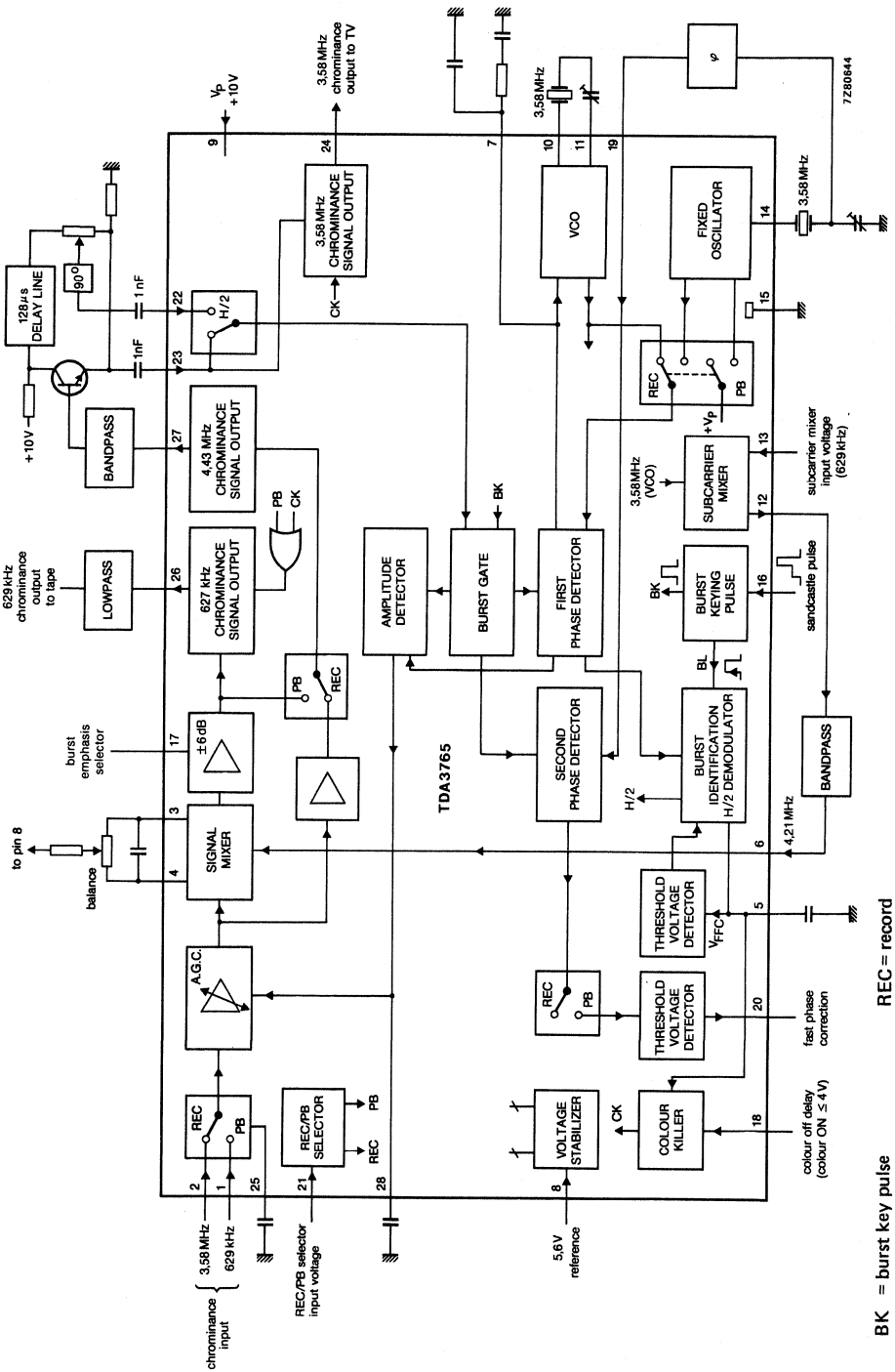


Fig. 1 Block diagram.

BK = burst key pulse
BL = blanking pulse
FFC = flip-flop correction
FPC = fast phase correction

REC = record
PB = playback
CK = colour killer

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_P = V_{9-15}$	max.	13,2	V
Voltage range at pins 1, 2, 5, 7, 8, 9, 16, 18, 19, 20, 21, 22, 23 to pin 15 (ground)	V_{n-15}		0 to V_P	V
Voltages ranges				
at pins 3, 4, 28*	$V_{3, 4, 28-15}$		3 to 6	V
at pin 6, 25*	$V_{6, 25-15}$		0 to 5	V
at pin 10*	V_{10-15}		1,5 to 4	V
at pin 13*, 17*	$V_{13, 17-15}$		0 to 3	V
at pin 14*	V_{14-15}		0 to 8	V
Voltages				
at pin 12	V_{12-15}	max.	V_P	V
at pin 24	V_{24-15}	max.	7	V
Currents				
at pins 11, 18	$-I_{11, 18}$	max.	2	mA
at pins 12, 26, 27	$-I_{12, 26, 27}$	max.	5	mA
at pin 24	$-I_{24}$	max.	3	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

* Measured with V_{8-15} = 5,6 V.

CHARACTERISTICS

$V_P = V_{9-15} = 10$ V; $V_{8-15} = 5{,}6$ V; $T_{amb} = 25$ °C; burst key duration 4 μs; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 9)					
Supply voltage	$V_P = V_{9-15}$	9,6	–	13,2	V
Supply current for playback and burst keying					
at $-I_{12, 18, 24, 26, 27} = 0$	$I_P = I_9$	–	47	–	mA
at $-I_{12, 18, 24, 26, 27} = 0$; $V_P = 12$ V	$I_P = I_9$	–	49	–	mA
A.G.C. preamplifier (pins 1 and 2)					
Input voltage* (f = 3,58 MHz) during record (peak-to-peak value)	$V_{2-15(p-p)}$	20	–	400	mV
Input voltage* (f = 629 kHz) during playback (peak-to-peak value)	$V_{1-15(p-p)}$	30	–	400	mV
Input resistance	$R_{1, 2-15}$	7	–	–	kΩ
Input capacitance	$C_{1, 2-15}$	–	–	5	pF
629 kHz chrominance signal (pin 26)* (transposed on to 629 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-15(p-p)}$	–	2	–	V
Signal suppression at output					
for f = 1,26 MHz	α_{26}	–	35	–	dB
for f = 4,21 MHz (externally balanced via pins 3 and 4)	α_{26}	–	40	–	dB
during colour killing (pin 25	α_{26}	40	–	–	dB
D.C. output voltage	V_{26-15}	–	6,7	–	V
3,58 MHz chrominance signal (pin 27)*					
Output voltage					
during record (peak-to-peak value)	$V_{27-15(p-p)}$	–	1,15	–	V
during playback after signal mixing (peak-to-peak value)	$V_{27-15(p-p)}$	–	–	3,1	V
Signal suppression at output					
for f = 4,21 MHz (externally balanced)	α_{27}	–	40	–	dB
for f = 7,16 MHz	α_{27}	–	30	–	dB
for f = 2,95 MHz	α_{27}	–	38	–	dB
for f = 2,32 MHz	α_{27}	–	30	–	dB
D.C. output voltage	V_{27-15}	–	7	–	V

* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	symbol	min.	typ.	max.	unit
3,58 MHz chrominance signal amplifier*					
Burst input signal					
at pin 22 (peak-to-peak value)	$V_{22\text{-}15(p\text{-}p)}$	–	225	–	mV
at pin 23 (peak-to-peak value)	$V_{23\text{-}15(p\text{-}p)}$	–	225	–	mV
Input resistance					
at pin 22	$R_{22\text{-}15}$	6	–	–	kΩ
at pin 23	$R_{23\text{-}15}$	6	–	–	kΩ
Output voltage of the chrominance signal at pin 24 (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	–	490	–	mV
Signal suppression at output (pin 24) during colour killing	α_{24}	35	–	–	dB
D.C. output voltage					
during colour-on	$V_{24\text{-}15}$	–	2,4	–	V
during colour-off (killed)	$V_{24\text{-}15}$	–	0,7	–	V
Subcarrier mixer					
629 kHz input voltage; sine-wave (peak-to-peak value)	$V_{13\text{-}15(p\text{-}p)}$	220	–	–	mV
Input resistance	$R_{13\text{-}15}$	1	–	–	kΩ
D.C. output voltage	$V_{12\text{-}15}$	–	7,9	–	V
4,21 MHz output voltage selective** (peak-to-peak value)	$V_{12\text{-}15(p\text{-}p)}$	–	800	–	mV
Signal suppression at output**					
for f = 3,58 MHz	α_{12}	20	–	–	dB
for f = 4,84 MHz	α_{12}	30	–	–	dB
Subcarrier input					
4,21 MHz input voltage (peak-to-peak value)	$V_{6,15(p\text{-}p)}$	250	–	–	mV
Input resistance	$R_{6\text{-}15}$	1,9	–	–	kΩ
Input capacitance	$C_{6\text{-}15}$	–	–	5	pF
3,58 MHz voltage controlled oscillator (VCO)					
Input resistance	$R_{10\text{-}15}$	–	430	–	Ω
Input capacitance	$C_{10\text{-}15}$	–	–	10	pF
Output resistance	$R_{11\text{-}15}$	–	–	200	Ω
PLL-controlled oscillator catching range	Δf	± 500	–	–	Hz
Phase difference between oscillator and burst signals for ± 400 Hz deviation of crystal frequency	φ	–	–	± 7	deg

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Measured with a 0,32 V (peak-to-peak), 629 kHz input signal on pin 13 ($-I_{12}$ = 1 mA).

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
3,58 MHz fixed oscillator					
Oscillator temperature coefficient*	TC	–	–	–3	Hz/K
Record/playback selector (pin 21)					
Input voltage for record**	$V_{21\text{-}15}$	–	–	4	V
Input current with $V_{21\text{-}15}$ = 4 V	I_{21}	–	–	130	μA
Input voltage for playback	$V_{21\text{-}15}$	8	–	–	V
Input current with $V_{21\text{-}15}$ = 8 V	I_{21}	–	–	430	μA
Input resistance	$R_{21\text{-}15}$	7	–	–	kΩ
Colour (on/off) killer delay					
Delay for chrominance signal OFF at AV = 1 V; C = 1 μF; PNP emitter follower with internal current of 0,1 mA	t_d	–	10	–	ms
Input voltage (pin 18)					
for forced colour ON	$V_{18\text{-}15}$	–	–	4	V
for forced colour OFF	$V_{18\text{-}15}$	5,5	–	9	V
Voltage stabilizer (pin 8)					
Range of external reference voltage	$V_{8\text{-}15}$	5,3	–	5,8	V
Input current	$-I_8$	–	–	120	μA
Sandcastle pulse input (pin 16)					
Input voltage for burst keying	$V_{16\text{-}15}$	7,1	–	–	V
Input current	I_{16}	–	–	5	μA
Delay time of BK	t_d	–	0,55	–	μs
Input voltage for triggering of flip-flop	$V_{16\text{-}15}$	2	–	–	V
Fast phase correction					
Input voltage▲ (peak-to-peak value)	$V_{19\text{-}15(p\text{-}p)}$	200	–	400	mV
Input resistance	$R_{19\text{-}15}$	3,3	–	–	kΩ
Output voltage without correction below phase differences of ± 50° at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} = < 6{,}5$ V	$V_{20\text{-}15}$	–	–	5,2	V
with correction above phase differences of ± 65° at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} = > 7{,}1$ V	$V_{20\text{-}15}$	9	–	–	V
Output resistance	$R_{20\text{-}15}$	–	35	–	kΩ

* Not considering the effects of external components.

** Pin open: record.

▲ Phase difference between output pin 14 and input pin 19 should be $\varphi = 90°$.

parameter	symbol	min.	typ.	max.	unit
Burst emphasis selector (pin 17)					
Input voltage active emphasis	V_{17-15}		open connection		
Input voltage inactive emphasis	V_{17-15}	–	–	0,5	V
Burst pre-emphasis at REC chroma output pin 26		–	6	–	dB
Burst de-emphasis at PB chroma output pin 27		–	5,3	–	dB

APPLICATION INFORMATION

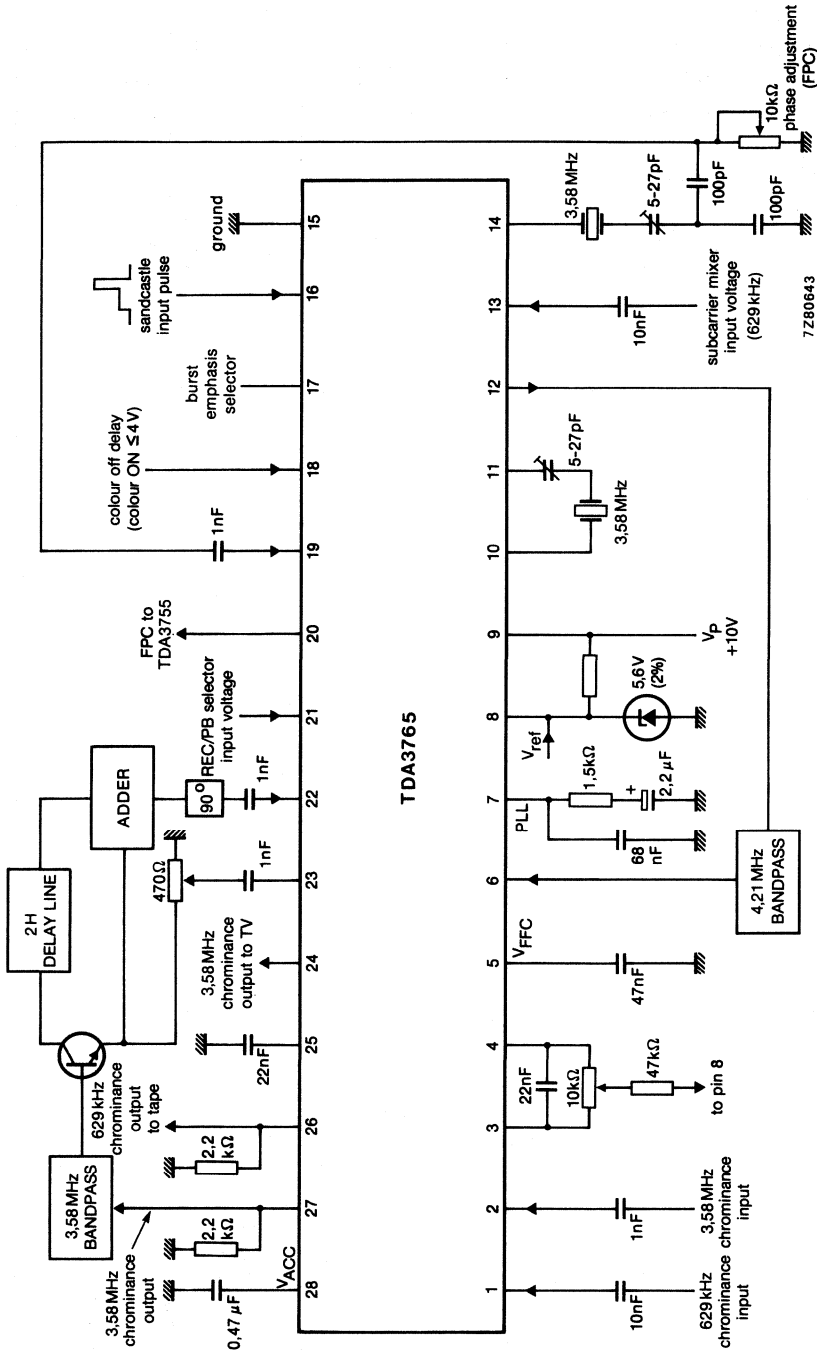


Fig. 2 Application diagram.

REC = record
PB = playback
FPC = fast phase correction
FFC = flip-flop correction

BAND SELECTOR AND WINDOW DETECTOR

GENERAL DESCRIPTION

The TDA3791 is a monolithic integrated circuit intended for application in search-tuning systems for video recorders. It is designed to select one out of four tuners, each representing a particular band. Band selection tuning is indicated by a variable voltage V_{AFC}.

Features

- Voltage window detector
- Band switch selector
- 4 short-circuit protected band switches
- Muting circuit
- Delay circuit
- Short-circuit protection circuit
- Power-on reset

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.		12	V
Supply current (pin 8)	$I_P = I_8$				
unloaded band switches ON		typ.		25	mA
all band switches OFF		typ.		12	mA
Power dissipation	P_{tot}	max.		1,8	W
Storage temperature range	T_{stg}	−65	to + 150		°C
Operating ambient temperature range	T_{amb}	0	to 70		°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

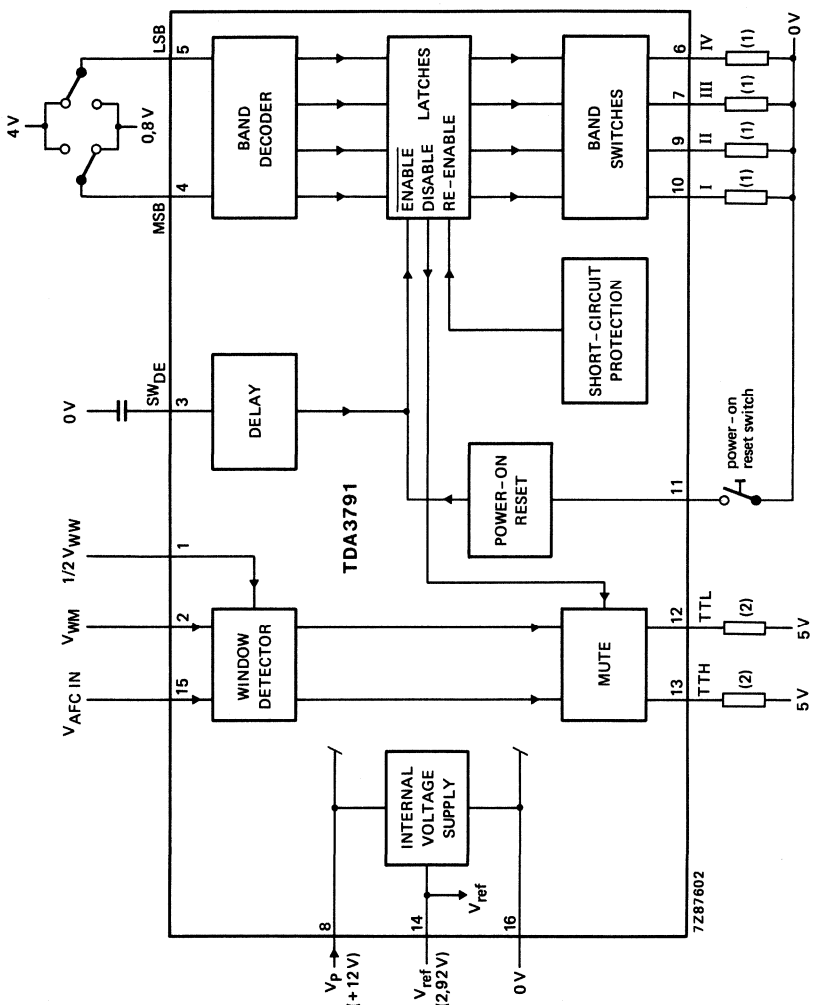


Fig. 1 Block diagram.

(1) $R = \frac{10\ V}{35\ mA}$. (2) $R = \frac{5\ V}{2\ mA}$.

FUNCTIONAL DESCRIPTION

Voltage window detector (see Table 1)

The voltage window is dependent upon two inputs; V_{WM} (pin 2) and $1/2V_{WW}$ (pin 1), which represent the centre of the window and the (window width)/2 respectively.

The voltage window range is from $V_{WM} - 1/2V_{WW}$ to $V_{WM} + 1/2V_{WW}$. A variable input voltage $V_{AFC\ IN}$ (pin 15) is compared with these window edges.

Table 1 Truth table; window detector

inputs	outputs	
$V_{AFC\ IN} = V_{15-16}$; $V_{WM} = V_{2-16}$; $V_{WW} = V_{1-16}$	V_{12-16}	V_{13-16}
$V_{AFC\ IN} < V_{WM} - 1/2V_{WW}$	HIGH	LOW
$V_{WM} - 1/2V_{WW} < V_{AFC\ IN} < V_{WM} + 1/2V_{WW}$	HIGH	HIGH
$V_{AFC\ IN} > V_{WM} + 1/2V_{WW}$	LOW	HIGH

Where: V_{12-16} = tuning too low (TTL); V_{13-16} = tuning too high (TTH).

During transitions of the outputs (V_{12-16} and V_{13-16}), a hysteresis value of approximately 20 mV is applied at the window edges.

Band-switch selector (see Table 2)

Selection of the band switches is determined by the input voltage levels of MSB (pin 4) and LSB (pin 5).

- If MSB or LSB > 4 V, the input is HIGH
- If MSB or LSB < 0,8 V, the input is LOW.

The band switches are selected as confirmed by Table 2.

Table 2 Truth table; band switch selector

MSB (V_{4-16})	LSB (V_{5-16})	switch	HIGH output
HIGH	HIGH	I	V_{10-16}
HIGH	LOW	II	V_{9-16}
LOW	HIGH	III	V_{7-16}
LOW	LOW	IV	V_{6-16}

Short-circuit protected band switches

A selected band switch has a minimum output voltage of $V_P - 0,3$ V provided the current is not more than 35 mA (I_{10}, I_9, I_7, I_6). If the output voltage at pins 10, 9, 7 or 6 is less than 9 V a short-circuit condition exists, and the output current will not be more than 80 mA. In this event the band switch is switched off, after an externally determined delay.

Muting

The muting circuit is active when a selected band switch is switched off. Both outputs TTL (pin 12) and TTH (pin 13) will then be LOW.

FUNCTIONAL DESCRIPTION (continued)

Delay circuit

After selection of a band switch, it will be in a conducting state. If after selection and a delay, the output voltage has not reached 9 V, the band is switched off. This delay is determined by an external capacitor on output SW_{DE} (pin 3).

Short-circuit protection

The short-circuit protection of each switch is provided by a flip-flop. If the condition of a band switch $V_o < 9$ V is detected, its flip-flop will be set and the band switch is switched off.

In the event of an incidental short-circuit to a band switch output, the band switch can be reset by applying 0 V to the power-on reset input (pin 11) or 0 V to the switch delay output SW_{DE} (pin 3).

Power-on reset

Before the voltage supply reaches 9,6 V, the short-circuit protection flip-flops are reset to enable the selection of a band switch.

The power-on reset circuit also supplies the voltage level for short-circuit detection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max.	13,2 V
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

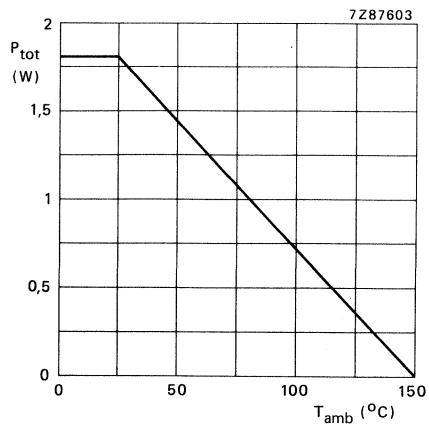


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = V_{8-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 8)	$V_P = V_{8-16}$	10	12	13,2	V
Supply current (pin 8)					
unloaded band switches ON	$I_P = I_8$	18	25	38	mA
all band switches OFF	$I_P = I_8$	9	12	16	mA
Voltage range					
$1/2V_{WW}$ (pin 1)	V_{1-16}	0,1	–	4,5	V
V_{WM} (pin 2)	V_{2-16}	1,8	–	10,5	V
$V_{WM} + 1/2V_{WW}$ at $V_{8-16} - 1,4$ V	$V_{2-16} \pm V_{1-16}$	1,7	–	10,6	V
$V_{AFC\ IN}$ (pin 15)	V_{15-16}	0,5	–	11,5	V
Input current					
$1/2V_{WW}$ (pin 1)	$-I_1$	–	–	2	μA
V_{WM} (pin 2)	I_2	–	–	0,2	μA
$V_{AFC\ IN}$ (pin 15)	I_{15}	–	0,2	0,4	μA
Hysteresis voltage V_{AFC}*	ΔV_{15-16}	–	20	50	mV
Delta current at $V_{AFC\ IN}$*	ΔI_{15}	–	–	25	nA
Temperature coefficient $I_{AFC\ IN}$	$TC(I_{15})$	–	–0,42	–	nA/°C
Temperature coefficient I_{WM}	$TC(I_2)$	–	–0,27	–	nA/°C
Deviation of applied voltage (pin 1)					
at $V_{1-16} = 100$ mV	ΔV_{1-16}	–35	–	+35	mV
at $V_{1-16} = 4,0$ V; $V_{2-16} = 6$ V	ΔV_{1-16}	–200	–	+200	mV
Input current (pin 4)					
at MSB $< 0,8$ V	I_4	–	–	0,1	μA
at MSB > 4 V	I_4	–	–	1,0	μA
Input current (pin 5)					
at LSB > 4 V	I_5	–	–	1,0	μA
at LSB $< 0,8$ V	I_5	–	–	0,1	μA
Voltage level (pin 4)					
at MSB HIGH	V_{4-16}	4	–	–	V
at MSB LOW	V_{4-16}	–	–	0,8	V
Voltage level (pin 5)					
at LSB HIGH	V_{5-16}	4	–	–	V
at LSB LOW	V_{5-16}	–	–	0,8	V
Short-circuit current of band switches I, II, III, IV (pins 10, 9, 7, 6)	$-I_{10, 9, 7, 6}$	35	50	80	mA
Voltage drop of band switches I, II, III, IV (pins 10, 9, 7, 6) at $I_{o(max)} = 35$ mA; $V_P = 10$ V	$V_{10, 9, 7, 6-16}$	–	–	0,3	V

* During switching of outputs V_{12-16} and/or V_{13-16}.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Voltage level short-circuit detection at $0{,}75V_P$	$V_{10,\,9,\,7,\,6\text{-}16}$	8,0	9,0	9,5	V
Output voltage (pin 13) TTH at $I_{13} = 2$ mA (LOW)	$V_{13\text{-}16}$	–	–	0,3	V
Output voltage (pin 12) TTL at $I_{12} = 2$ mA (LOW)	$V_{12\text{-}16}$	–	–	0,3	V
Leakage current (pin 13) TTH at $V_{13\text{-}16} = 13{,}2$ V	I_{13}	–	–	10	μA
Leakage current (pin 12) TTH at $V_{12\text{-}16} = 13{,}2$ V	I_{12}	–	–	10	μA
Output current (pin 3) SW_{DE} at $V_{3\text{-}16} = 6$ V	$-I_3$	5	12	20	μA
Maximum value of delay capacitor	C_3	–	–	40	nF
Maximum delay time at $\pm C_3$ (nF)/(I_3/10) ms	t_d	–	–	50	ms
Power-on-reset voltage	$V_{8\text{-}16}$	6	–	9,6	V
Leakage current unswitched band switches at $V_{10,\,9,\,7,\,6\text{-}16} = -12$ V	$I_{10,\,9,\,7,\,6}$	–	–	5	μA

STEREO/DUAL TV SOUND PROCESSING CIRCUITS

GENERAL DESCRIPTION

The TDA3800G; GS are stereo/dual TV sound decoder circuits for processing an a.f. and a sound i.f. signal in TV and VCR equipment, using active filters in selective frequency processing.

In deviation of our standard terms and conditions of sale the supply of the TDA3800 (ABS) does not imply any patent indemnity whatsoever with respect to the stereo-tone patent rights of I.G.R. Germany.

Features

- Signal processing of one a.f. signal and one i.f. signal
- 2nd i.f. limiter/amplifier and FM demodulator (5,742 MHz) for the second sound channel
- Pilot carrier processing with digital identification, hysteresis and short switching times
- De-matrixing of the signals for the two audio channels
- De-emphasis
- Two dual channel, independently controllable a.f. outputs
- Low-resistance a.f. outputs (short-circuit protected); can be used for headphone
- Standardized switched output for controlling external audio/video equipment
- Signal path control by an identification bit (also in audio/video mode)
- LED indication of selected mode (also in audio/video mode)
- Possibility to apply a.f. signals from external equipment via the de-emphasis inputs (audio/video mode)
- Mode selection of stereo/mono or sound I/sound II
  - TDA3800G dynamic selection with internal storage
  - TDA3800GS static selection

QUICK REFERENCE DATA

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	typ.	12 V
2nd sound i.f. input voltage for start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	50 μV
Pilot carrier amplifier control range	ΔG_v	min.	20 dB
A.F. input voltage (r.m.s. value)	$V_{i(rms)}$	typ.	1 V
A.F. demodulator output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	0,6 V
LED output current	I_{LED}	typ.	15 mA
Signal-to-noise ratio of the a.f. signal switches	S/N	typ.	80 dB
Crosstalk in stereo mode	α_S	min.	40 dB
Crosstalk in dual sound mode	α_{DS}	min.	60 dB

PACKAGE OUTLINES

28-lead DIL; plastic (SOT117).

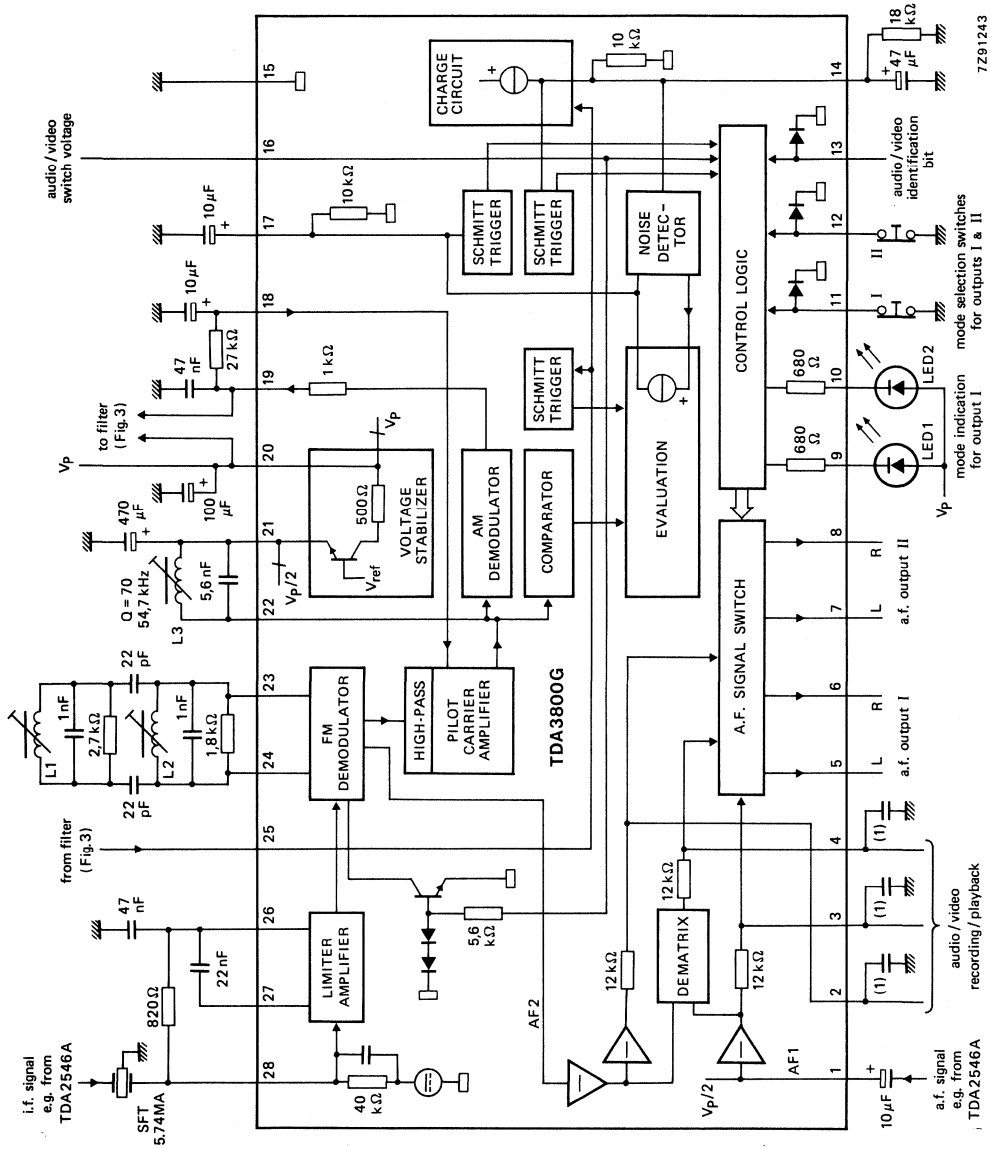


Fig. 1 TDA3800G block diagram and test circuit in accordance with Fig. 3.

(1) De-emphasis 3,9 nF.
(2) TDA3800G application using active filters.

Coil data

L1 and L2: TOKO 7 k;
Q = 25, f_o = 5,74 MHz.

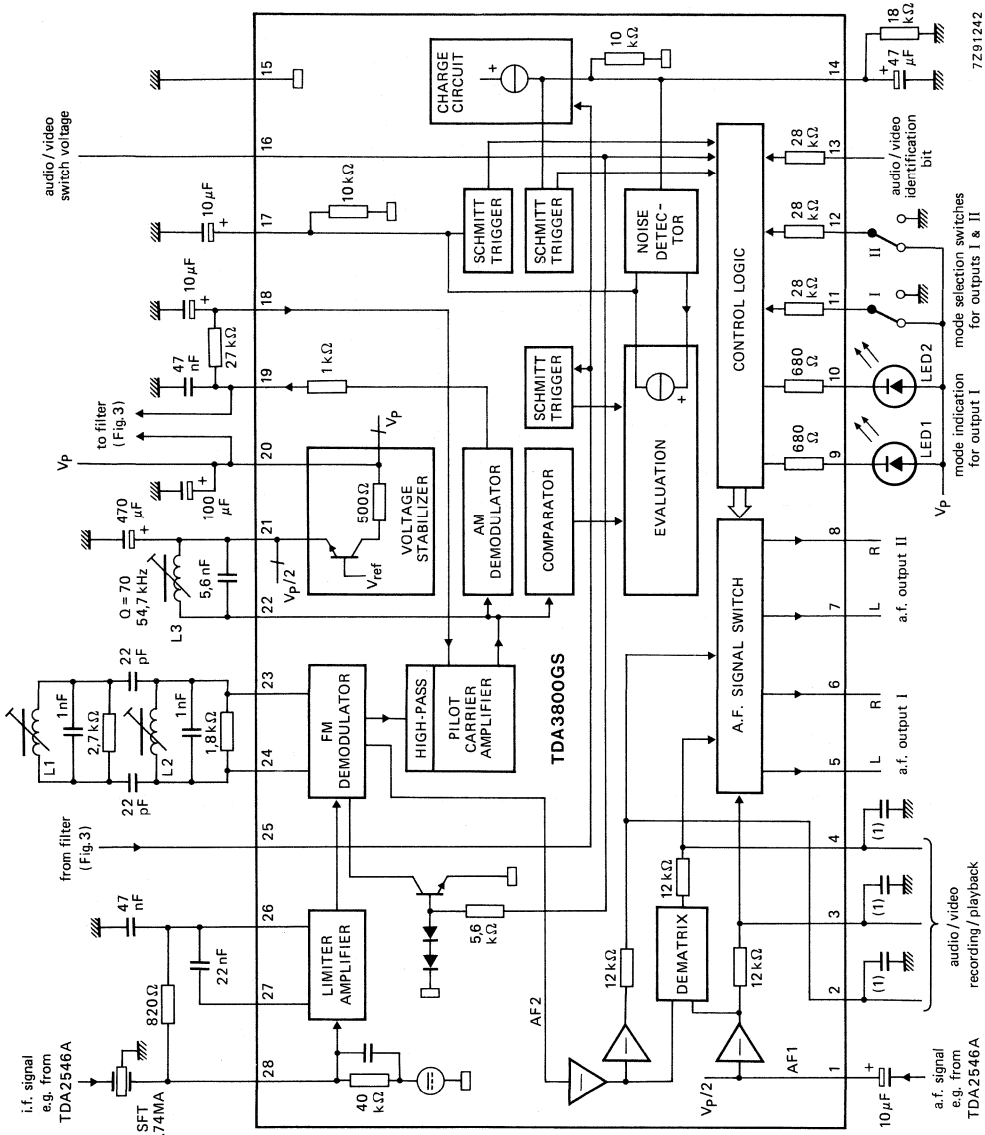


Fig. 2 TDA3800GS block diagram and test circuit in accordance with Fig. 3.

(1) De-emphasis 3,9 nF.
(2) TDA3800GS application using active filters.

Coil data

L1 and L2: TOKO 7 k;
Q = 25, f_o = 5,74 MHz.

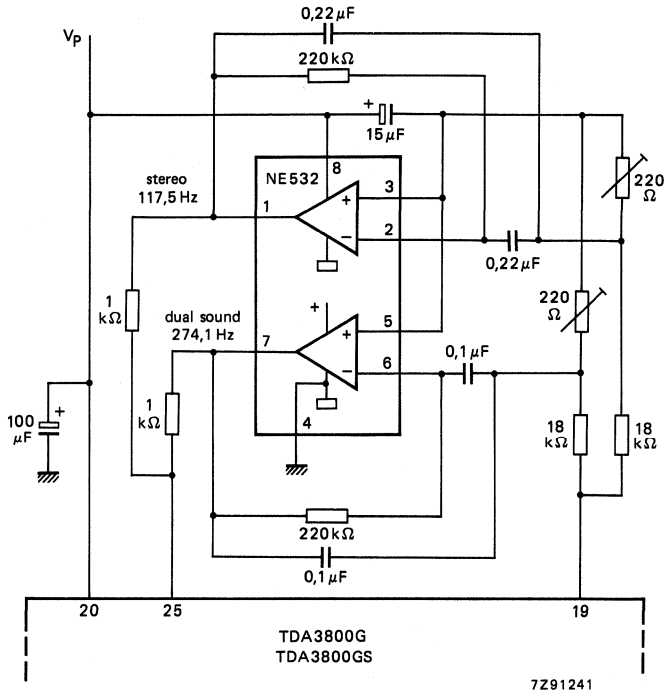


Fig. 3 External filter circuit for the identification frequencies 117,5 Hz and 247,1 Hz.

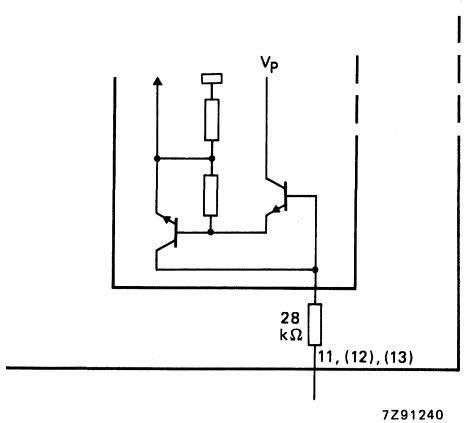


Fig. 4 TDA3800GS internal circuit for the control input leads 11, 12 and 13.

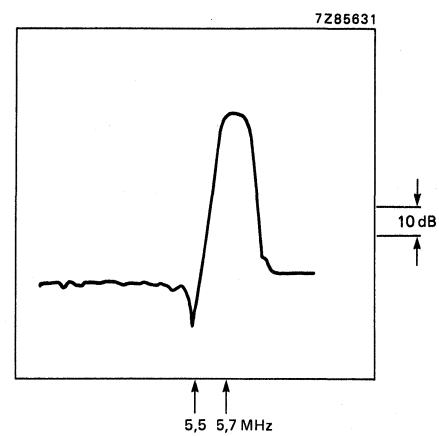


Fig. 5 IF2 filter selection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 20)	$V_P = V_{20-15}$	max.	14 V
Voltage			
at pins 1; 9; 10; 16 and 25	V_{n-15}	max.	V_P
at pins 11; 12 and 13*	$V_{11;12;13-15}$	max.	V_P
Current			
at pins 11; 12 and 13**	$I_{11;12;13}$	max.	1 mA
at pin 21	short-circuit protected		
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}		−25 to +150 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

* TDA3800GS only.
** TDA3800G only.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1/Fig. 2 with a 1 kHz signal. $V_{1\text{-}15(rms)}$ = 0,5 V, an i.f. signal $V_{28\text{-}15(rms)}$ = 5 mV (VC/2SC = 20 dB, $\Delta f = \pm 50$ kHz, f_m = 400 Hz) and with adjusted de-matrix circuit; i.f. filter selection at input pin 28 as in Fig. 5; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 20)					
Supply voltage range	$V_P = V_{20\text{-}15}$	10,8	12	13,2	V
Supply current (without LED current; mono)	$I_P = I_{20}$	40	–	87	mA
FM limiter/amplifier and demodulator					
Start of limiting	$V_{28\text{-}15(rms)}$	–	–	60	μV
Input resistance	$R_{28\text{-}15}$	–	40	–	kΩ
Input capacitance (Fig. 5)	$C_{28\text{-}15}$	–	4,5	–	pF
AM suppression at V_i = 0,5 mV; $\Delta f = \pm 30$ kHz	α_{AMS}	50	–	–	dB
Pilot carrier processing					
D.C. input voltage	$V_{18\text{-}15}$	–	7,2	–	V
D.C. voltage (reference via tuning coil)	$V_{22\text{-}15}$	–	6,0	–	V
AM demodulator output voltage	$V_{19\text{-}15}$	–	7,3	–	V
Controlled pilot carrier output voltage (peak-to-peak value)	$V_{22\text{-}21(p\text{-}p)}$	–	250	–	mV
Output resistance	$R_{22\text{-}15}$	50	–	–	kΩ
Identification frequency evaluation					
No identification signal (lower threshold)	$V_{14\text{-}15}$	–	–	2	V
Identification signal (upper threshold)	$V_{14\text{-}15}$	4	–	–	V
Stereo transmission	$V_{17\text{-}15}$	–	–	2	V
Dual sound transmission	$V_{17\text{-}15}$	4	–	–	V
De-matrixing					
Output voltages	$V_{2;3;4\text{-}15}$	–	5,3	–	V
De-emphasis output resistances	$R_{2;3;4\text{-}15}$	–	12	–	kΩ
A.F. output signal of 2nd i.f. (r.m.s. value)	$V_{2\text{-}15(rms)}$	–	0,6	–	V
Attenuation of the demodulator output signal AF2 at audio/video mode	α_{AF2}	75	–	–	dB
Distortion of the AF2 signal $V_{o2\text{-}15}$	d_{tot}	–	0,4	–	%

parameter	symbol	min.	typ.	max.	unit
AF1 input					
D.C. input voltage	$V_{1\text{-}15}$	–	6	–	V
Input resistance	$R_{1\text{-}15}$	–	14	–	kΩ
Maximum input signal (r.m.s. value)	$V_{1\text{-}15(rms)}$	–	2	–	V
A.F. signal switches					
D.C. output voltages	$V_{5;6;7;8\text{-}15}$	–	5,3	–	V
Output resistances	$R_{5;6;7;8\text{-}15}$	–	200	–	Ω*
Maximum a.f. output signals (r.m.s. value)					
for $V_{AFI(rms)}$	$V_{5;6\text{-}15(rms)}$	–	2	–	V
for $V_{AFII(rms)}$	$V_{7;8\text{-}15(rms)}$	–	2	–	V
Total distortion when applying a signal at $V_{2;3;4\text{-}15(rms)} = 0{,}5$ V	d_{tot}	–	–	0,1	%
Signal plus noise-to-noise ratio	S + S/N	–	80	–	dB
Crosstalk attenuation					
in stereo mode (f = 1 kHz at pin 2)	α_S	40	–	–	dB
in dual sound mode (f = 20 Hz to 20 kHz)	α_{DS}	60	–	–	dB
Audio/video switch					
Audio/video switch voltage					
for playback (HIGH)	$V_{16\text{-}15}$	7	–	V_P	V
for recording (LOW)	$V_{16\text{-}15}$	0	–	2,5	V
Audio/video identification bit (TDA3800G)					
for stereo mode (LOW)	$V_{13\text{-}15}$	0	–	0,2	V
for dual sound mode (HIGH) at $V_{13\text{-}15} \approx 0{,}7$ V	I_{13}	–	0	–	mA
Audio/video switch voltage (TDA3800GS) (stereo/dual sound)					
for stereo mode (LOW)	$V_{13\text{-}15}$	–	–	0,8	V
for dual sound mode (HIGH)	$V_{13\text{-}15}$	2,4	–	–	V
Mode selection switches for outputs I and II					
Active LOW (TDA3800G) input voltage LOW	$V_{11;12\text{-}15}$	0	–	0,2	V
switch open condition at $V_{11;12\text{-}15} \approx 0{,}7$ V	$I_{11;12}$	–	0	–	mA
Pulse duration	t_p	1	–	–	μs

* Connection of high-impedance headphones is possible.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Switching voltage (TDA3800GS)					
Mono transmission both equals I and II mono					
Dual sound transmission switching voltage to pin 11 (pin 12 not affected)					
a.f. output II sound I and a.f. output I sound II	V_{11-15}	–	–	0,8	V
a.f. output I sound I and a.f. output II and II	V_{11-15}	2,4	–	–	V
Stereo transmission switching voltage to pin 12 (pin 11 not affected)					
a.f. outputs I and II mono	V_{12-15}	–	–	0,8	V
a.f. outputs I and II stereo	V_{12-15}	2,4	–	–	V
Mode indication (pins 9 and 10; see also Table 1)					
Only the mode for output I is indicated					
Maximum output current	$I_{9;10}$	–	15	–	mA
Voltage stabilizer (pin 21)					
Output voltage	V_{21-15}	–	6	–	V
Maximum d.c. output current short-circuit protected	$\pm I_{21}$	–	0,5	–	mA

Notes to the characteristics (TDA3800G only)

1. Serial commands for stereo/mono or sound I/sound II selection are determined by the identification bit of the transmission.
2. The pushbuttons at pins 11 and 12 are assigned to the a.f. outputs I and II respectively.
3. When a transmitter changes its identification from dual sound to stereo and then back to dual sound again, the last selected dual sound signal is available automatically because of the internal storage of the choice. This is also applicable for mono/stereo selection.
4. Power-on reset: when applying the supply voltage, the stereo or the AF1 signal appears at both outputs I and II depending on the type of transmission.

Table 1 Mode indication possibilities

LED 1	LED 2	selected reception mode
OFF	OFF	mono at mono or stereo transmission
ON	ON	stereo at stereo transmission
OFF	ON	AF1 signal at dual sound transmission
ON	OFF	AF2 signal at dual sound transmission

STEREO/DUAL TV SOUND DECODER CIRCUIT

GENERAL DESCRIPTION

The TDA3803A is a stereo/dual TV sound decoder circuit with static switching for processing two AF signals in TV and VCR equipment. The LOW/HIGH static switching signals control the AF output selector. Two operational amplifiers perform bandpass filtering of the identification signals.

Features

- Amplification of the two AF input signals by integrated operational amplifiers
- Low distortion stereo de-matrix
- All operational amplifiers offset compensated
- De-emphasis with operational amplifiers, preferably applied to the output terminals
- Two output ports each with two channels for headphones and loudspeakers
- Dual sound information at one port, each port individually switchable from sound I to sound II and sound II to sound I
- Mute function; while mute is active, it is possible to connect an external mono AF input signal to pin 10 appearing at pins 20 to 23.
- Identification without additional signals (horizontal etc.)

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-12}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	28 mA
Pilot carrier amplifier gain control range	ΔG_v	>	40 dB
AF input signals; at G_v = 0 dB (r.m.s. value)	$V_{i(rms)}$	=	1 V
LED output current	I_{LED}	typ.	12 mA
Weighted signal-to-noise ratio of the a.f. signal switches (CCIR468/2)	(S+N)/N	≥	60 dB
Crosstalk in stereo mode	α_S	>	40 dB
Crosstalk in dual sound mode	α_{DS}	>	60 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

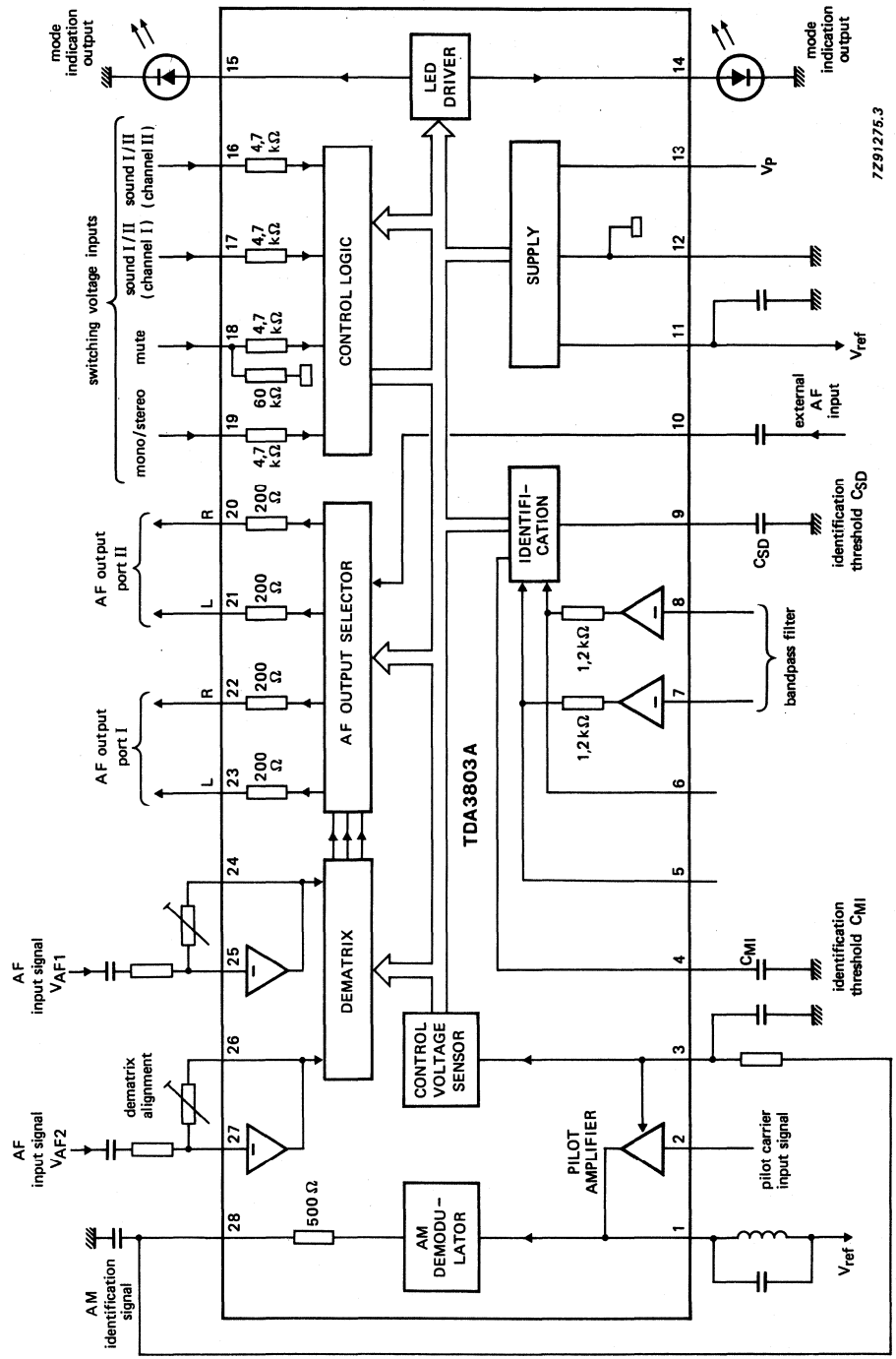


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-12}$	max.	14	V
Voltages with respect to pin 12 (ground)				
pins 25; 27 and 28	$V_{25;27;28-12}$	max.	V_P	
Voltages				
pin 1 to pin 10	V_{n-12}	max.	V_P	
pin 14 to pin 19	V_{n-12}	max.	V_P	
Currents				
pin 11	I_{11}	max.	3	mA
pins 20; 21; 22; 23	$I_{20;21;22;23}$	max.	10	mA
pin 28	$-I_{28}$	max.	3	mA
Total power dissipation	P_{tot}	max.	1,5	W
Storage temperature range	T_{stg}		−25 to +125	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; overall voltage gain (G_v) = 1; ($R_S = R_R$); measured in Fig. 2 with a 1 kHz signal. AF input AF2 = AF1 = 0,5 V, pilot carrier input signal $V_{2\text{-}12(rms)}$ = 16 mV, m = 0,5 and with adjusted de-matrix circuit; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13\text{-}12}$	10,8	12	13,2	V
Supply current (without LED current)	$I_P = I_{13}$	–	28	35	mA
Reference voltage (pin 11)	V_{ref}	–	6	–	V
Input resistance (dynamic)	$R_{11\text{-}12}$	–	4	–	kΩ
AF part					
Amplification	G_v	–40	–	18	dB
Input signal at G_v = 1	$V_{AF1} = V_{AF2}$	–	–	1	V
Mono AF input signal (pin 10)*					
Input signal	$V_{10\text{-}12}$	–	–	2	V
DC input voltage level	$V_{10\text{-}12}$	–	6	–	V
Input resistance	$R_{10\text{-}12}$		16	–	kΩ
Stereo mode AF output port I pin 22: right pin 23: left					
AF output port II pin 20: right pin 21: left					
Output signal (THD ≤ 0,5%)					
port I ($V_{23\text{-}12} = V_{22\text{-}12}$)	V_{oI}	–	–	2	V
port II ($V_{21\text{-}12} = V_{20\text{-}12}$)	V_{oII}	–	–	2	V
Weighted signal-to-noise ratio of the AF signal switches (in accordance with CCIR468/2)	(S+N)/N		65	–	dB
Unweighted signal-to-noise	(S+N)/N	60	–	–	dB
Total harmonic distortion ($V_{20;21;22;23\text{-}12}$ = 0,5 V; G_v = 1)	THD	–	0,05	–	%
Crosstalk attenuation (selective)					
stereo mode (f_1 = 1 kHz; f_2 = 400 Hz)	α_S	40	–	–	dB
dual sound mode (f = 250 Hz to 12,5 kHz)	α_{DS}	60	–	–	dB

* An input signal at pin 10 appears at pins 20 to 23 if the mute input (pin 18) is activated ($V_{18\text{-}12} \geq 2$ V).

parameter	symbol	min.	typ.	max.	unit
DC input voltage level at pins 25 and 27	$V_{25;27-12}$	–	6	–	V
DC output voltage level at pins 20; 21; 22 and 23	V_{n-12}	–	6	–	V
Output resistance at pins 20; 21; 22 and 23	V_{n-12}	–	200	–	Ω
Identification part					
Pilot carrier amplifier					
input signal (pin 2)	V_{2-12}	5	–	–	mV
gain control range	ΔG_v	40	–	–	dB
controlled output signal (pin 1) (peak-to-peak value)	$V_{1-12(p-p)}$	–	300	–	mV
Input resistance (pin 2)	R_{2-12}	–	60	–	kΩ
Output resistance (pin 1)	R_{1-12}	1	–	–	MΩ
DC input voltage level (pin 2) applied externally (see Fig. 2)	V_{2-12}	–	6	–	V
DC output voltage level (pin 28)					
without gain control	V_{28-12}	–	6	–	V
with gain control	V_{28-12}	–	7,9	–	V
Identification signal (pin 28) (peak-to-peak value)	$V_{28-12(p-p)}$	–	2,0	–	V
Filter operational amplifiers open loop gain	G_o	78	–	–	dB
Identification frequency evaluation					
No identification signal (lower threshold)	V_{4-12}	–	–	2,5	V
Identification signal (upper threshold)	V_{4-12}	4,7	–	–	V
Stereo transmission (lower threshold)	V_{9-12}	–	–	2,5	V
Dual sound transmission (upper threshold)	V_{9-12}	4,7	–	–	V
Control logic part					
Mute input voltage (pin 18)					
mute OFF	V_{18-12}	–	–	0,8	V
mute ON (see the remarks to pin 10)	V_{18-12}	2	–	–	V
Switching stereo/mono and sound I/sound II					
Stereo transmission					
switching voltage to pin 19 (pin 17 and 16 not affected)					
output ports I and II mono	V_{19-12}	–	–	0,8	V
output ports I and II stereo	V_{19-12}	2	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Control logic part (continued)					
Mono transmission both output ports I and II mono					
Dual sound transmission					
switching voltage to pin 16 (pin 19 and 17 not affected)					
output port II sound I	$V_{16\text{-}12}$	2	–	–	V
output port II sound II	$V_{16\text{-}12}$	–	–	0,8	V
switching voltage to pin 17 (pin 16 and 19 not affected)					
output port I sound I	$V_{17\text{-}12}$	–	–	0,8	V
output port I sound II	$V_{17\text{-}12}$	2	–	–	V
Mode indication (pins 14 and 15; see also Table 1)					
Output current	$-I_{14;\ 15}$	9	12	15	mA
Output voltage (note 2)	$V_{14;\ 15\text{-}12}$	0	–	8	V
Stereo/mono transmission: LED indication is valid for the transmission mode					
Dual sound transmission: LED indication is valid for port I					

Table 1 Mode indication (note 1)

transmission mode	LED pin 15	LED pin 14
mono	OFF	OFF
stereo:		
stereo selection; $V_{19\text{-}12} \geqslant 2$ V	ON	ON
mono selection; $V_{19\text{-}12} \leqslant 0{,}8$ V	ON	ON
dual sound:		
sound I selection; $V_{17\text{-}12} \leqslant 0{,}8$ V	ON	OFF
sound II selection; $V_{17\text{-}12} \geqslant 2$ V	OFF	ON

Notes to the characteristics

1. With mute (pin 18) ON both LEDs (pin 14 and 15) are switched OFF.
2. Pin 14 and 15 are also suitable as output switches to control TDA3810. At LED OFF and $I_{14,\ 15} \leqslant 100\ \mu A$, then $V_{14,\ 15\text{-}12} \leqslant 200$ mV.

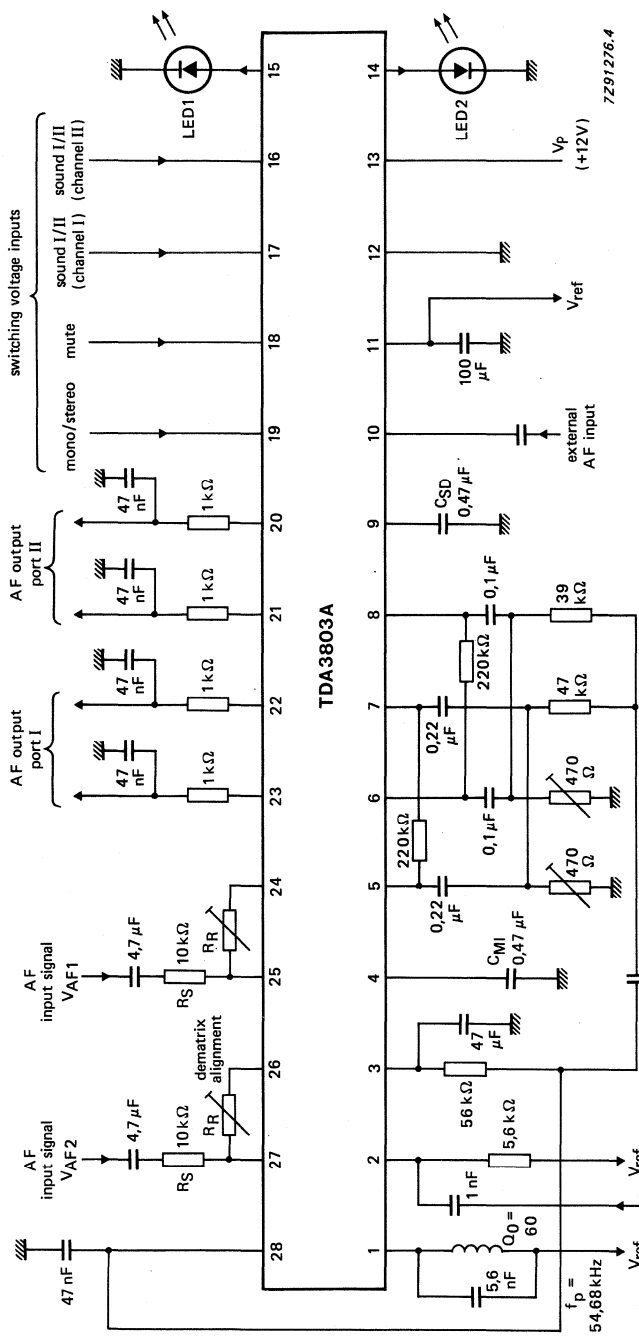


Fig. 2a Application diagram and test circuit; external components.

APPLICATION INFORMATION (continued)

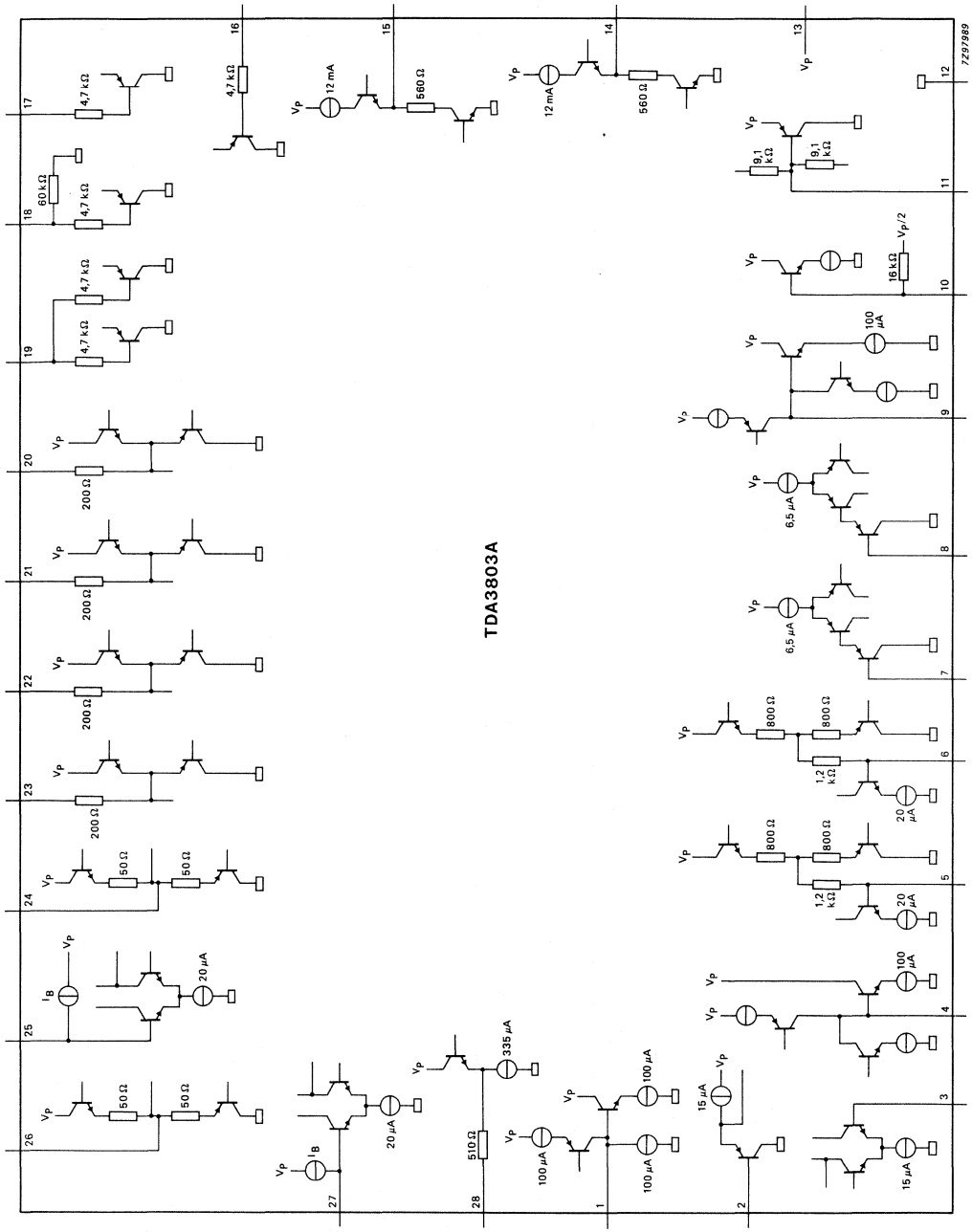


Fig. 2b Application diagram and test circuit; part of internal circuitry.

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

Features

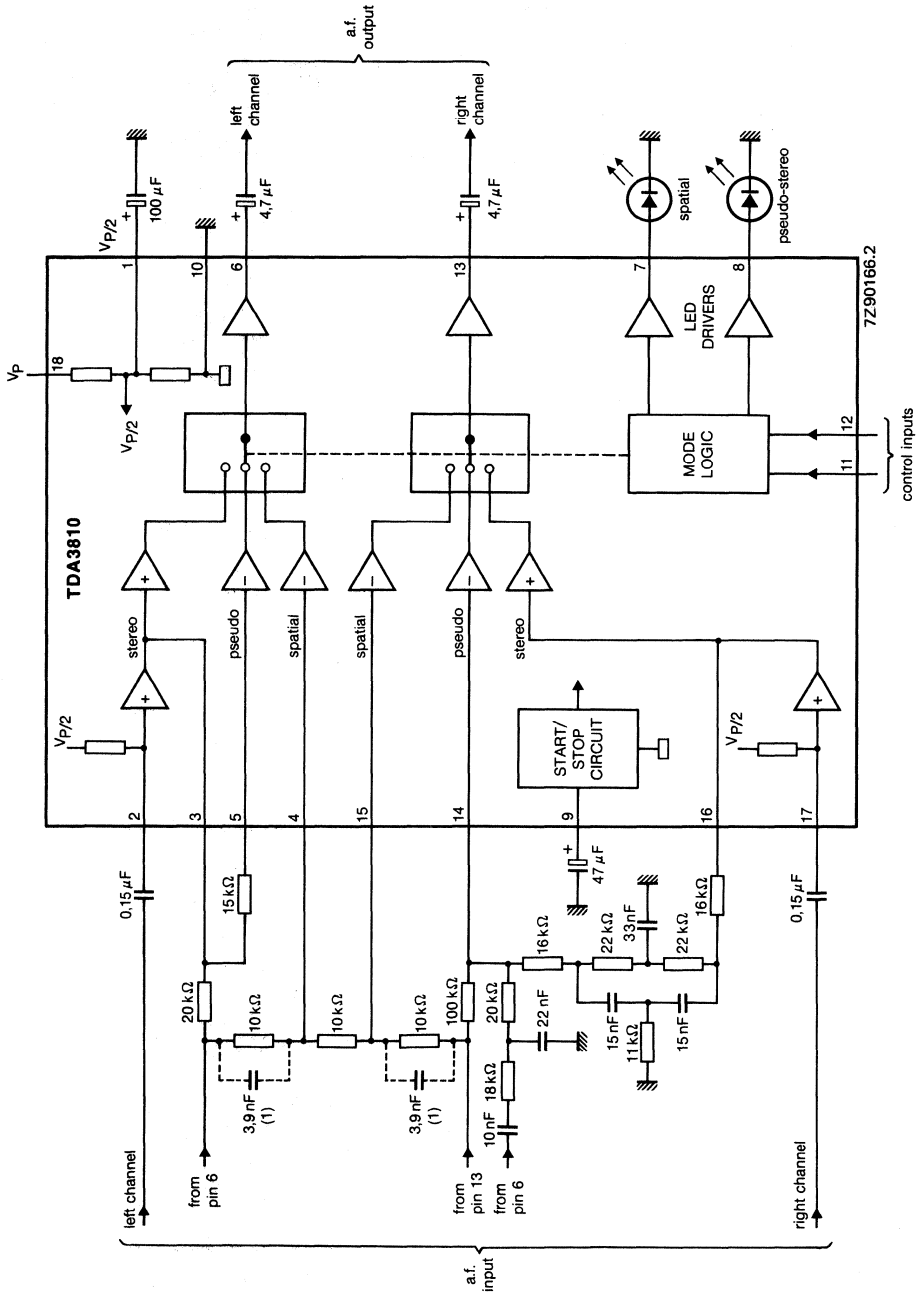
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_P	typ.	12 V
Supply current (LEDs off)	I_P	typ.	6 mA
Operating ambient temperature range	T_{amb}	0 to	+ 70 °C
Input signal (r.m.s. value)	$V_{i(rms)}$	<	2 V
Total harmonic distortion (stereo)	THD	typ.	0,1 %
Channel separation (stereo)	α	typ.	70 dB
Gain (stereo)	G_v	typ.	0 dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	18 V
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10,13\text{-}10} \geqslant 4{,}7$ kΩ; $C_{6\text{-}10,13\text{-}10} \leqslant 150$ pF.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2% (stereo mode)	$V_{i(rms)}$	–	–	2	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH) Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	$-I_o$	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3825 is a single FM demodulator system with external AF input and mute.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- Multiple input AF operational amplifier with offset compensation
- External AF input
- High AF output voltage with low distortion
- AF gain of 0 dB without external components
- Frequency response can be determined by external components
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Source selector						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; V_u = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

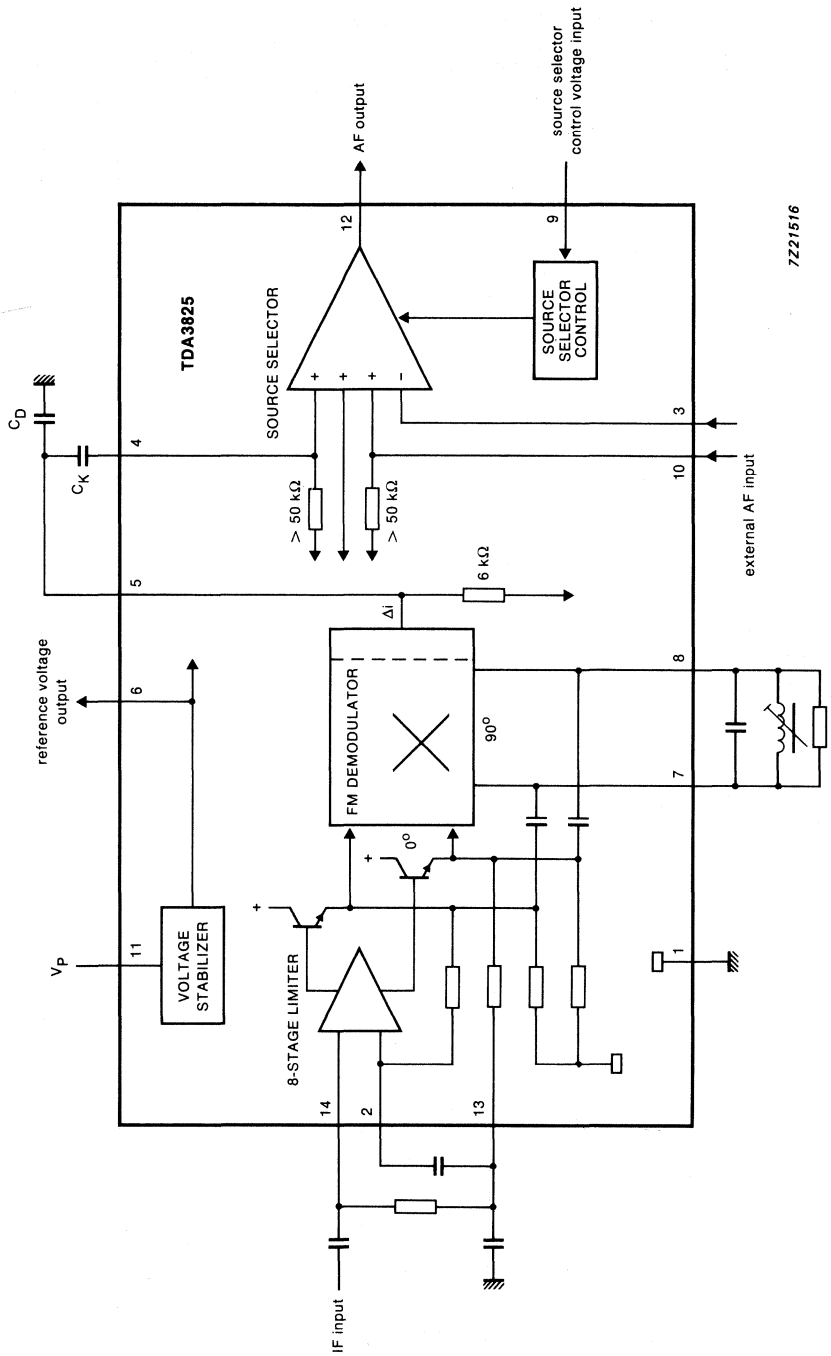


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	15	–	–	kΩ
Input capacitance		C_{14-13}	–	–	6	pF
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Output impedance (pin 5)		$\lvert Z_{5-1}\rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz, V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ⩽ 0.1%; G_V = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance (pin 4)		$\lvert Z_{4-1}\rvert$	50	–	–	kΩ
(pin 10)		$\lvert Z_{10-1}\rvert$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 6)		R_{3-6}	–	–	10	kΩ
(pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression for mute		α_{mute}	70	76	–	dB
Crosstalk attenuation		$\alpha_{4/10}$	64	70	–	dB
Offset voltage between any two source selector positions		V_{12-6}	–	–	50	mV
Source selector control	see Fig.3					
Source coltrol voltage (pin 9)						
Mute active input voltage		V_{9-1}	0	–	1/3 V_P−1	V
input current		I_9	10	–	500	μA
Input 1 active (pin 4) input voltage		V_{9-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_9	−200	–	+200	μA
Input 2 active (pin 10) input voltage		V_{9-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_9	−600	–	−40	μA
Input voltage at pin 9 for I_9 = 0 μA		V_{9-1}	–	$\frac{V_P-0.7}{2}$	–	V
Reference source (pin 6)						
Reference voltage input		V_{ref}	2.17	2.27	2.37	V
Output current		$\lvert I_6\rvert$	–	250	–	μA

DEVELOPMENT DATA

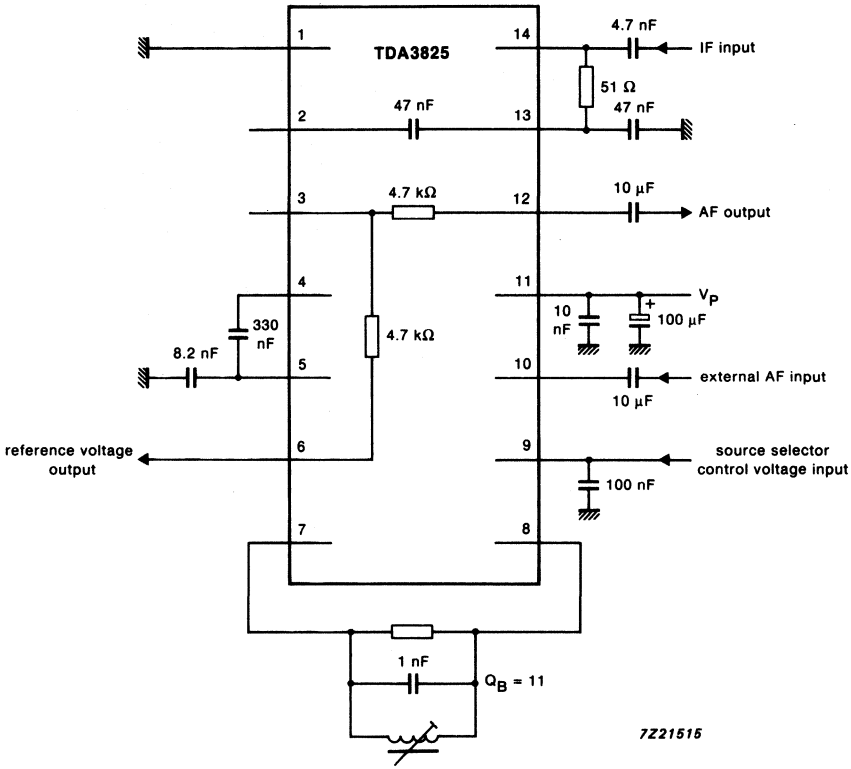


Fig. 2 Test circuit.

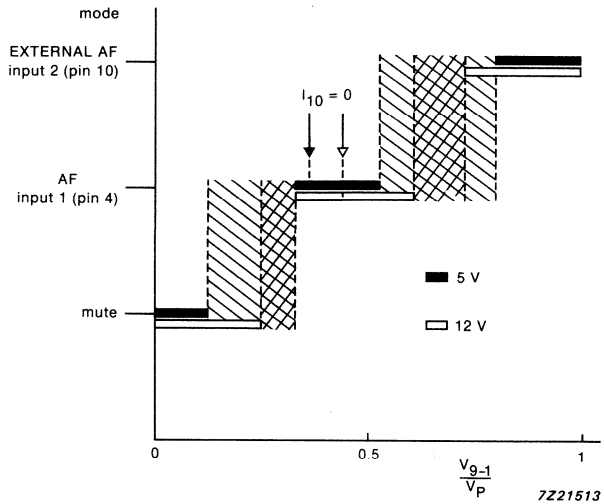


Fig. 3 Source selector logic diagram.

DEVELOPMENT DATA

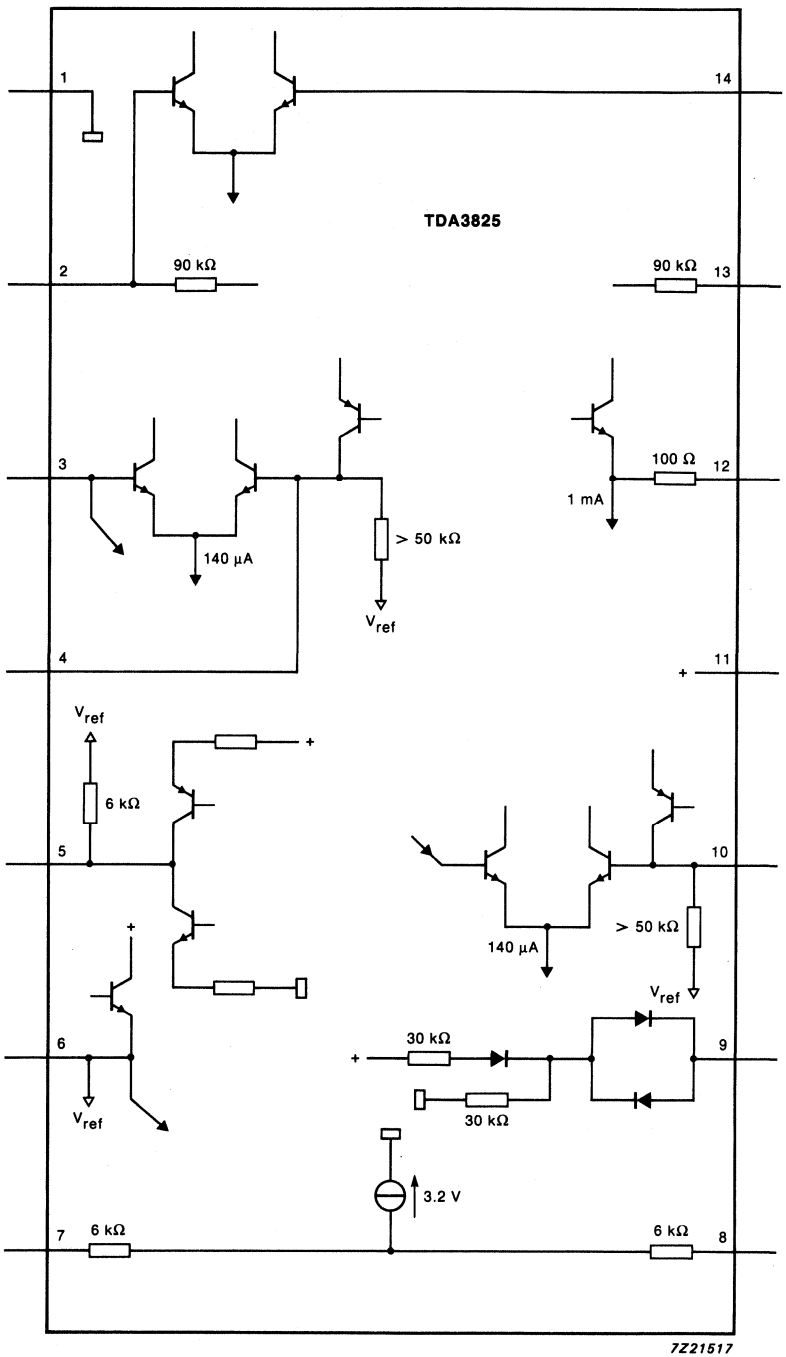


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

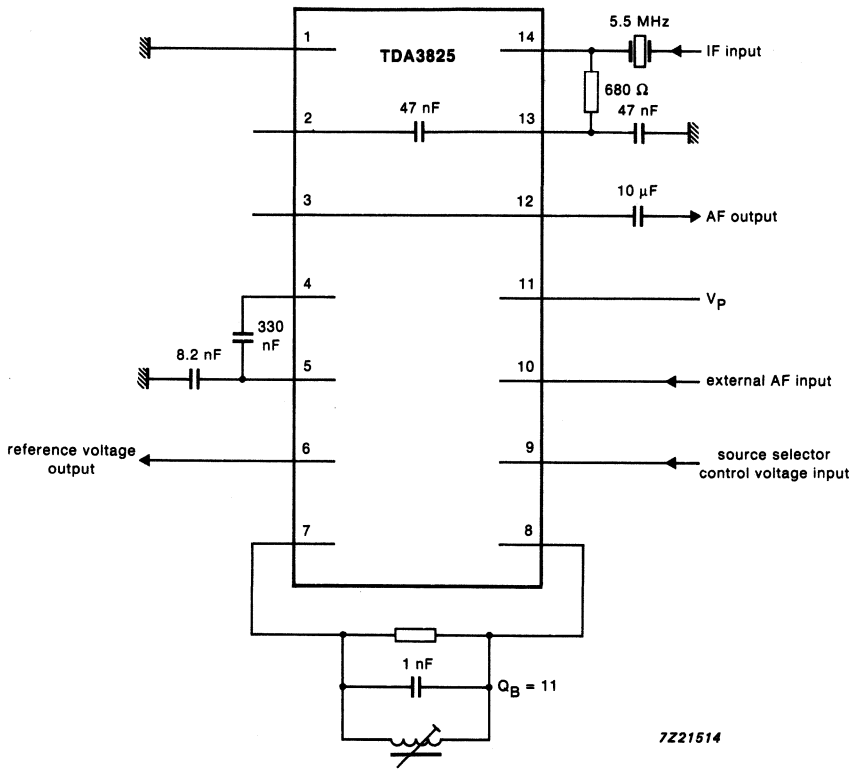


Fig. 5 Application diagram.

DEVELOPMENT DATA

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3826 is a single FM demodulator system with mute and 6 dB AF amplifier.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- AF operational amplifier output with offset compensated input stage
- High AF output voltage with low distortion
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	–	%
AF switch						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; G_V = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

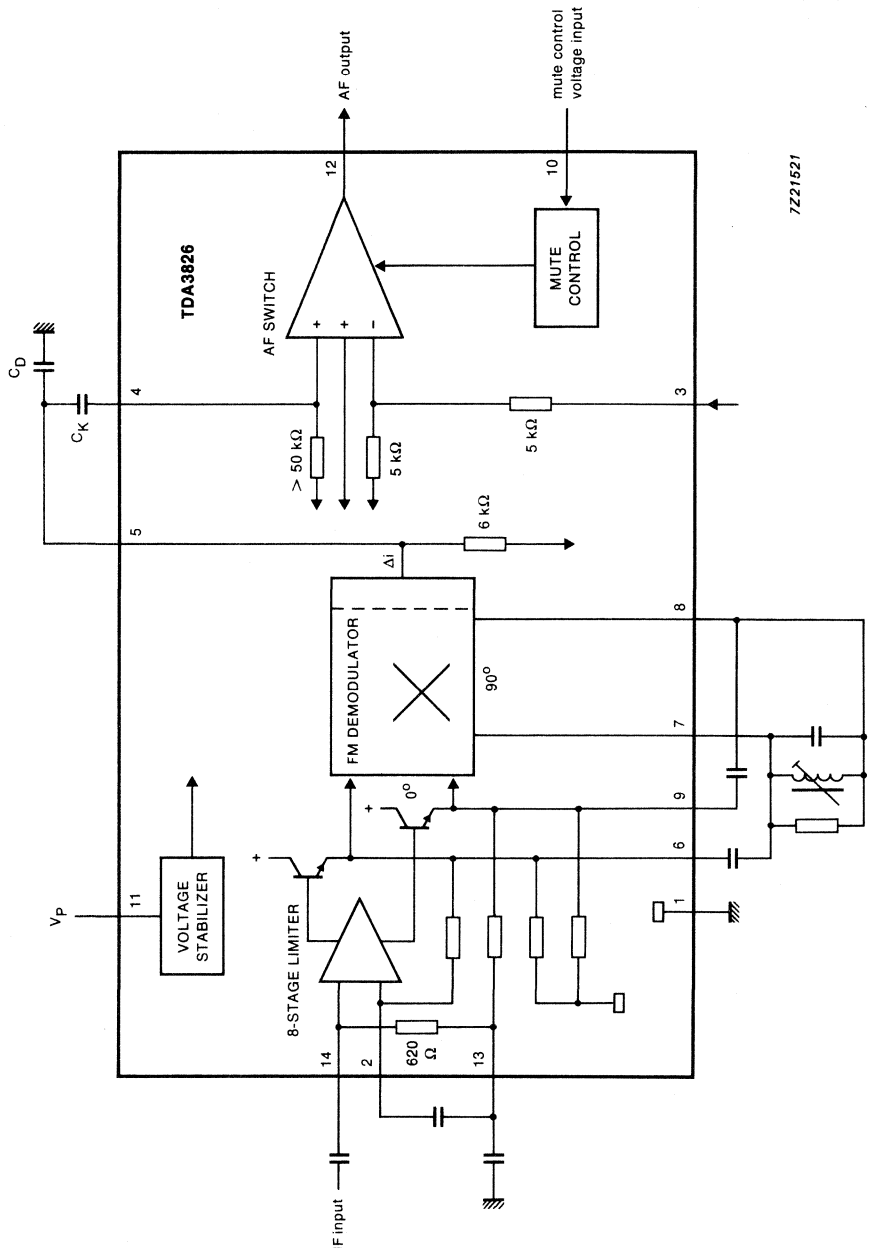


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	–	620	–	Ω
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output impedance (pin 5)		$\|Z_{5-1}\|$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz; V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
AF switch (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ≤ 0.1%; G_v = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance						
(pin 4)		$\lvert Z_{4-1}\rvert$	50	–	–	kΩ
(pin 10)		$\lvert Z_{10-1}\rvert$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression in case of mute		α_{mute}	70	76	–	dB
Mute control	see Fig. 3					
Mute control voltage (pin 10)						
Input (pin 4) active						
input voltage		V_{10-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_{10}	−200	–	+200	μA
Mute active						
input voltage		V_{10-1}	0	–	1/3 V_P−1	V
input current		I_{10}	10	–	500	μA
input voltage		V_{10-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_{10}	−600	–	−40	μA
Input voltage at pin 10 for I_{10} = 0 μA		V_{10-1}	–	$\frac{Vp-0.7}{2}$	–	V

DEVELOPMENT DATA

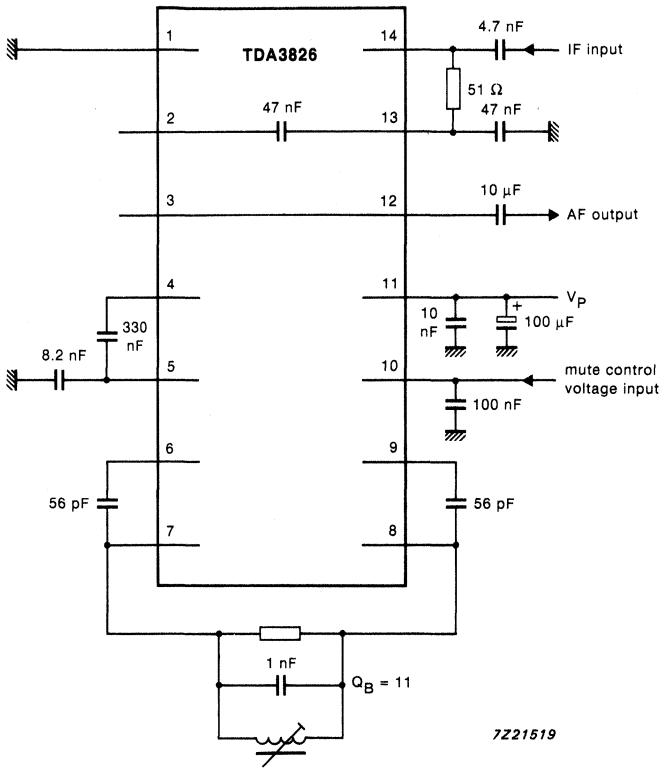


Fig. 2 Test circuit.

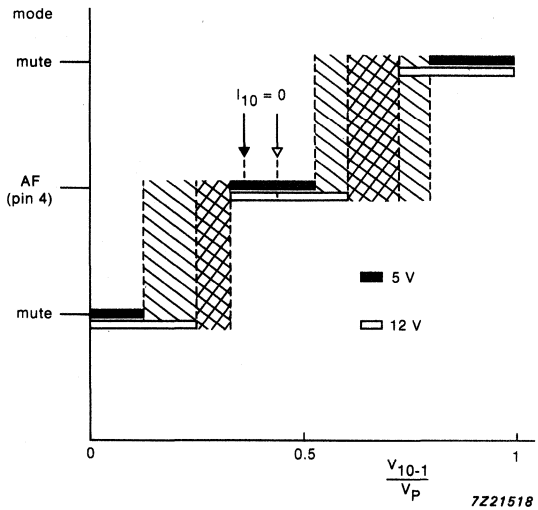


Fig. 3 Mute control logic diagram.

DEVELOPMENT DATA

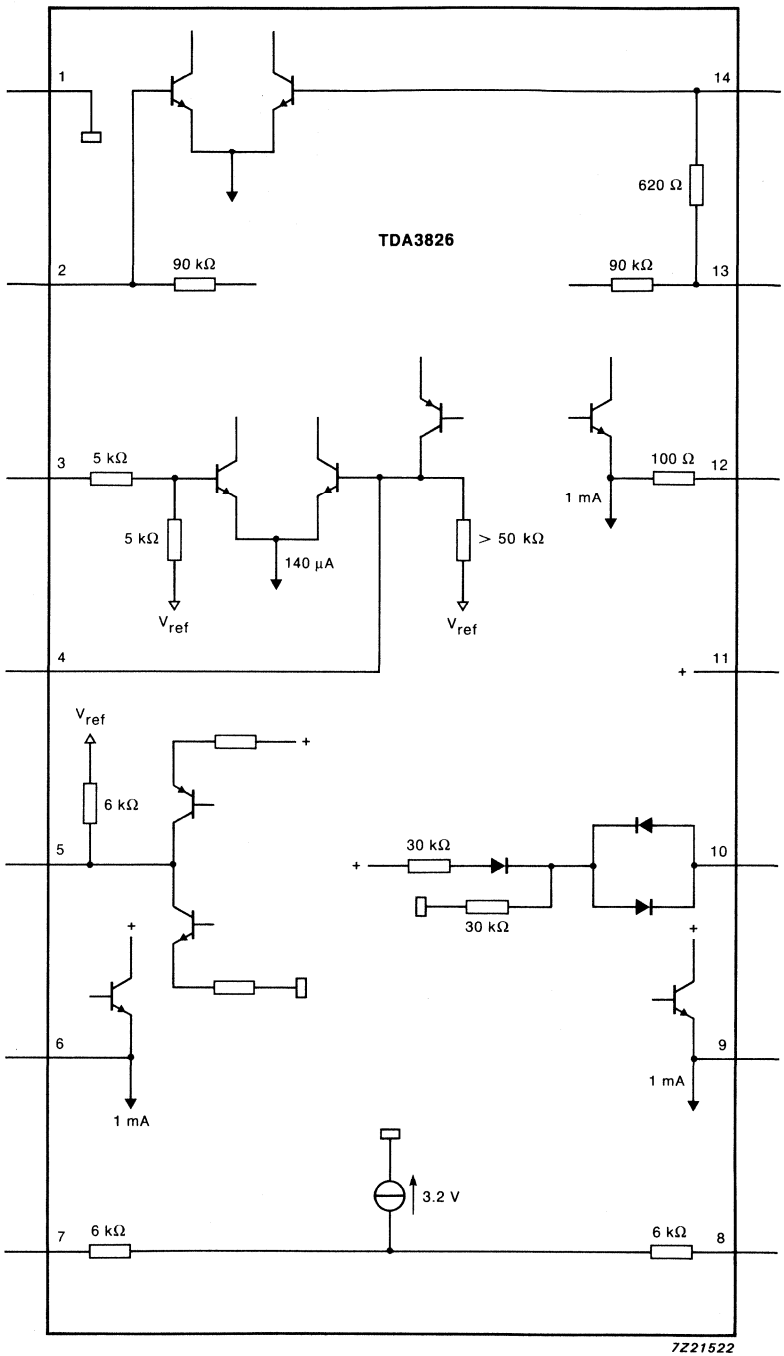


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

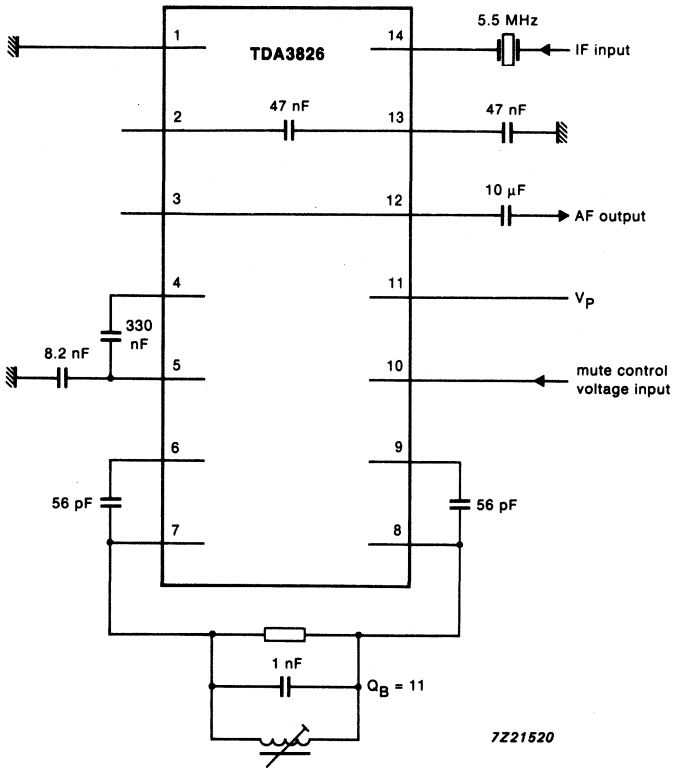


Fig. 5 Application diagram.

DEVELOPMENT DATA

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA3827

TV-sound demodulator circuit with SCART switches and AF control

FEATURES

- Wide supply voltage range from 4.5 V to 13.2 V
- Wide frequency range from 4 to 12 MHz
- High ripple rejection
- High precision and temperature compensated FM-demodulator output
- Multiple-input AF operational amplifiers with offset compensation
- SCART AF input / AF output (low impedance)
- External AF input
- High-level AF output voltage with low distortion
- External selection of the source selector AF gain
- Low switching noise between AF and mute
- Wide volume-control range

GENERAL DESCRIPTION

The TDA3827 contains a single FM demodulator with SCART switches, a mute function and volume control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5 V	–	26	–	mA
		V_P = 12 V	–	28	–	mA
(S+N)/N	signal to weighted noise		73	78	–	dB
$V_{5(rms)}$	FM demodulator output voltage (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	450	500	550	mV
$V_{13(rms)}$	SCART output signal (RMS value)		–	1.0	–	V
G_v	volume control range		80	85	–	dB
$V_{17(rms)}$	AF output signal (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	–	1.0	–	V
THD	total harmonic distortion (pin 17)		–	0.5	–	%

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3827	18	DIL	plastic	SOT102

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

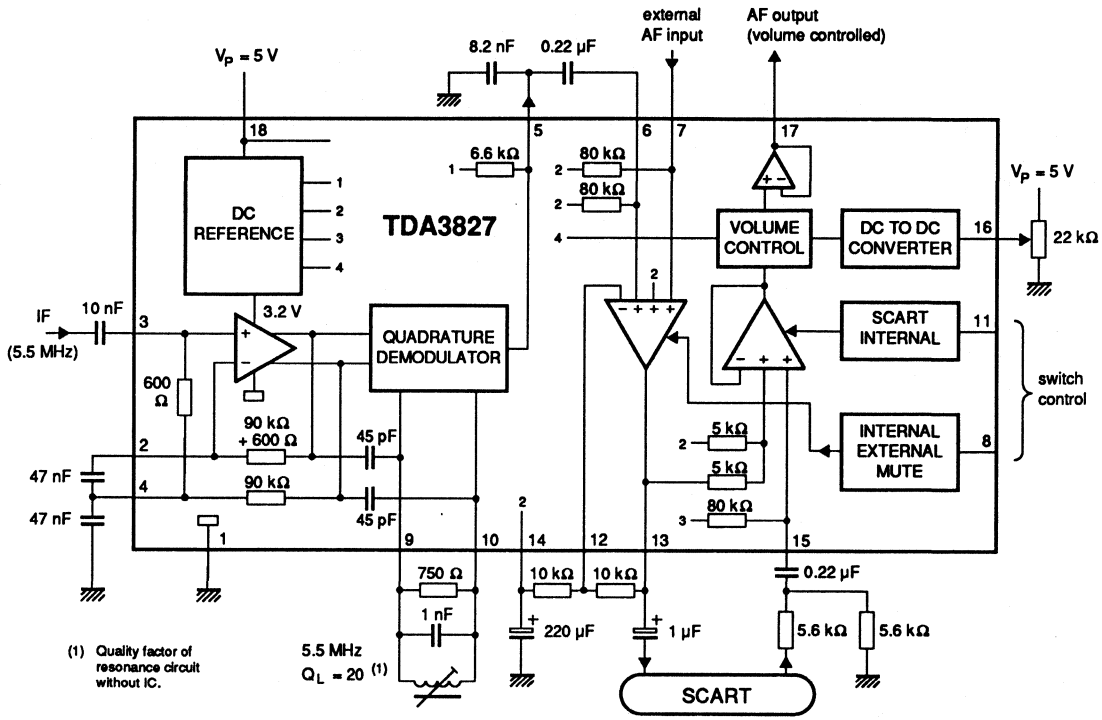


Fig.1 Block diagram.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

PIN CONFIGURATION

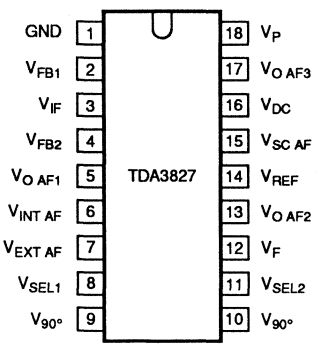


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{FB1}	2	limiter amplifier feedback
V_{IF}	3	FM IF input signal
V_{FB2}	4	limiter amplifier feedback
$V_{O\ AF1}$	5	AF output signal
$V_{INT\ AF}$	6	internal AF input signal
$V_{EXT\ AF}$	7	external AF input signal
V_{SEL1}	8	selection voltage for internal / external AF input and mute
$V_{90°}$	9	quadrature demodulator
$V_{90°}$	10	tuned circuit reference
V_{SEL2}	11	selection voltage for internal / external or SCART audio
V_F	12	source selector feedback
$V_{O\ AF2}$	13	output signal to SCART
V_{REF}	14	reference voltage
$V_{SC\ AF}$	15	input signal from SCART
V_{DC}	16	DC volume control voltage
$V_{O\ AF3}$	17	AF output signal from volume control
V_P	18	supply voltage

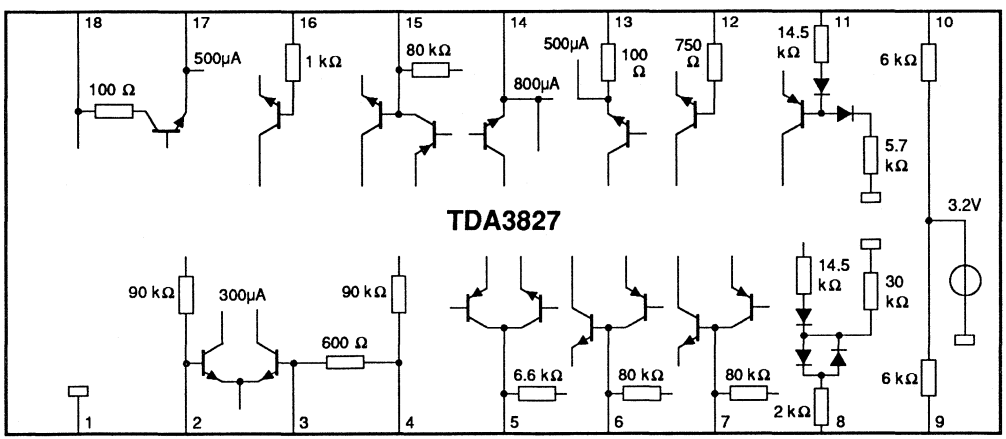


Fig.3 Internal circuits.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	–0.5	V_P + 6.8	V
V_{ext}	external voltage (pins 2 to 10, 12 to 15 and 17)	–0.3	V_P – 0.7	V
	external voltage at pin 11	–0.3	13.2	V
	external voltage at pin 16	–0.3	V_P	V
R_L	external DC load resistance (pin 13 and pin 17)	5.0	–	kΩ
C_L	capacitive output load (pin 13 and pin 17)	–	1500	pF
P_{tot}	total power dissipation	–	450	mW
T_{stg}	storage temperature range	–40	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD-protection (note 1)	± 2000	–	V

Note to the limiting values

1. Measured with a 100 pF capacitor in series with a 1.5 kΩ resistor.

CHARACTERISTICS

All voltages are measured to GND (pin 1); V_P = 5 V; V_{IF} = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5.0 V	–	26	30	mA
		V_P = 12.0 V	–	28	32	mA
V_{14}	reference voltage		2.2	2.3	2.4	V
I_{14}	output current		–	± 250	–	µA
IF limiting amplifier						
$V_{i(rms)}$	input signal at pin 3 (RMS value)		–	–	200	mV
		3 dB below nominal AF level at pin 5	–	30	50	µV
R_{3-1}	input resistance		–	600	–	Ω
$V_{2,3,4}$	DC voltage		–	2.1	–	V

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator (Q_L = 20)						
$V_{5(rms)}$	AF-output signal (RMS value)		450	500	550	mV
	residual $2f_o$-signal (RMS value)	without de-emphasis	–	–	30	mV
TC	temperature coefficient (pin 5)		–	1	2	mV/K
α_{AM}	AM suppression	f_{AM} = 400 Hz, m = 0.3, $V_{i(rms)}$ = 500 µV; Fig.8	50	62	–	dB
THD	total harmonic distortion	see Fig.8	–	0.3	0.5	%
Z_o	output impedance (pin 5)		–	6.6	–	kΩ
B_{AF1}	small signal bandwidth (pin 5)	at –1 dB; without de-emphasis	100	–	–	kHz
(S+N)/N	signal to weighted noise ratio	CCIR468-3, DIN45405; see Fig.8	73	78	–	dB
RR	ripple rejection	f_R = 70 Hz, V_R = 100 $mV_{(p-p)}$	30	35	–	dB
$V_{9,10}$	DC voltage		–	3.2	–	V
Source selector						
$V_{i\ 6,7(rms)}$	input signal (RMS value)		–	500	1000	mV
$Z_{6,7}$	input impedance		50	80	–	kΩ
G_o	open loop gain		–	60	–	dB
$G_{13/6,7}$	gain	see Fig.4	–	0	–	dB
	gain (typical application)	see Fig.1	–	6	–	dB
V_{13}	DC voltage		–	2.3	–	V
I_{13}	DC output current		–	–	1.0	mA
Z_{13}	output impedance dynamic		–	–	10	Ω
C_L	capacitive output load (pin 13)		–	–	1500	pF
$V_{13(rms)}$	output signal (RMS value)	handling THD < 0.1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	20	–	µV
B_{AF2}	small signal bandwidth	at –1 dB	100	–	–	kHz
dV/dt	slew rate (pin 13)		1	–	–	V/µs
ΔV_{13}	offset-voltage between any two source selector positions		–	5	20	mV
α_{mute}	AF suppression at mute		80	90	–	dB
$\alpha_{7/6}$	crosstalk attenuation		70	76	–	dB

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source selector control (see Fig.5)						
V_8	voltage for internal selection of AF-input (pin 6)		1/3 V_P	–	2/3 V_P –0.7	V
I_8	selection input current		–	–	200	µA
V_8	voltage for external selection of AF-input (pin 7)		2/3 V_P +0.7	–	V_P	V
I_8	selection input current		40	–	600	µA
V_8	voltage for mute active		0	–	1/3 V_P – 1	V
I_8	input current		–10	–	–500	µA
SCART switch and level control						
$V_{15(rms)}$	AC input signal (RMS value)		–	500	1000	mV
Z_{15}	input impedance		50	80	–	kΩ
$G_{17\text{-}15}$	voltage gain	V_{16} = 4.1 V	–1.5	0	+ 1.5	dB
G_{max}	maximum voltage gain	V_{16} = 5.0 V	+ 4.0	+ 5.0	+ 6.0	dB
ΔG_V	volume control range	see Fig.7	80	86	–	dB
V_{17}	DC voltage		–	2.3	–	V
I_{17}	DC output current		–	–	–1	mA
Z_{17}	dynamic output impedance		–	–	10	Ω
C_L	capacitive output load (pin 17)		–	–	1500	pF
$V_{17(rms)}$	output signal (RMS value)	THD ≤ 1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	100	–	µV
B_{AF3}	small signal bandwidth (pin 17)	at –3 dB	50	100	–	kHz
THD	distortion (pin 17)	at maximum gain	–	0.5	1.0	%
ΔV_{17}	offset voltage between internal and SCART		–	5	20	mV
V_{16}	control voltage	minimum gain –80 dB; see Fig.7	0.7	1.0	–	V
I_{16}	control current		–	–	50	µA
$\alpha_{6,7/15}$	crosstalk attenuation between IF-stage and control-stage	IF sound modulated; SCART switch on; source-selector on position input 1	80	90	–	dB
SCART switch control (see Fig.6)						
V_{11}	voltage for internal active		0	–	4/5 V_P –3	V
I_{11}	current		0	–	–100	µA
V_{11}	voltage for SCART active		4/5 V_P –1	–	13.2	V
I_{11}	current		$\frac{V_{11} - 1.4}{20.000}$	–	700	µA

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

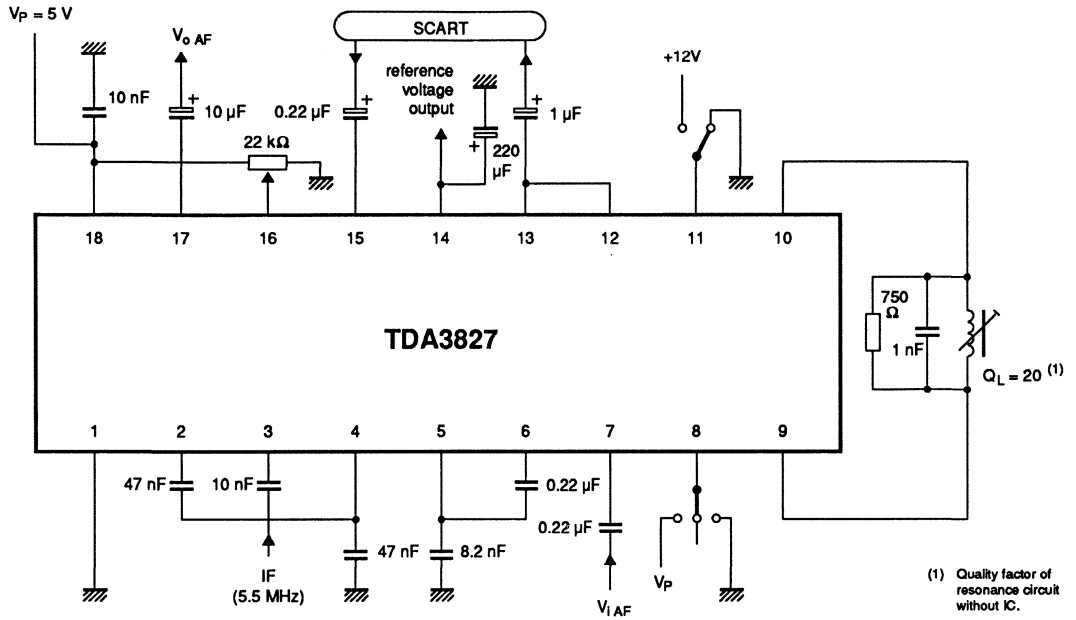


Fig.4 Test circuit.

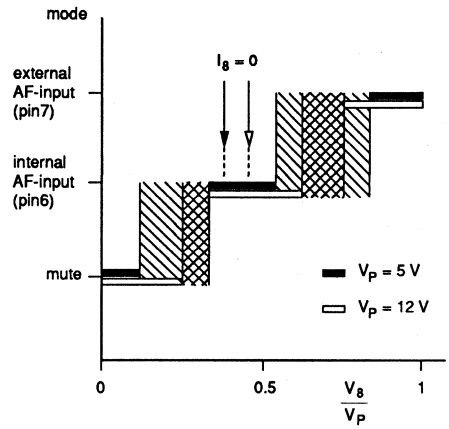


Fig.5 Source selector switching levels.

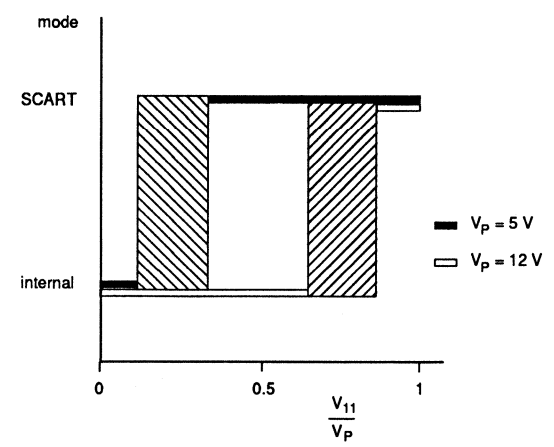


Fig.6 SCART switching levels.

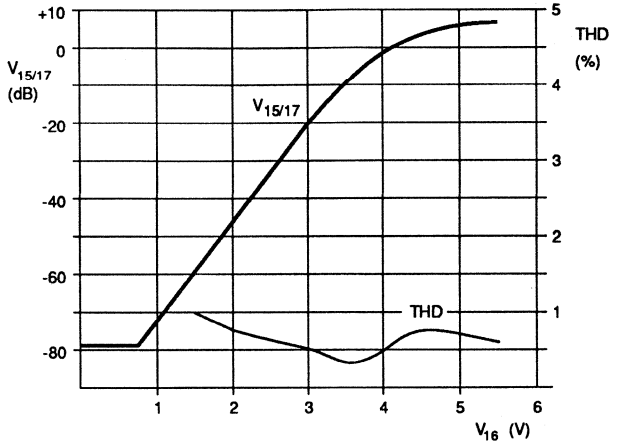


Fig.7 Volume control diagram.

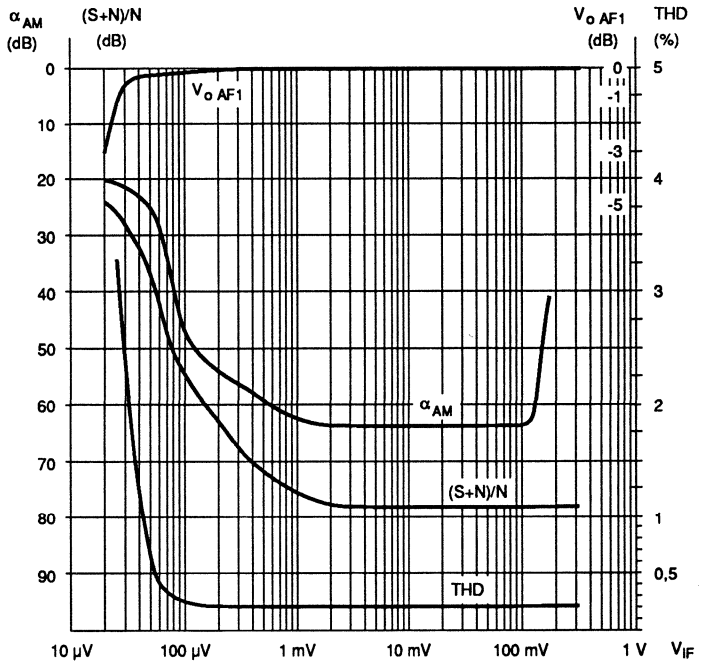


Fig.8 AF output voltage at pin 5, THD, (S+N)/N in accordance with to CCIR468-3 and AM suppression α_{AM} as functions of IF input voltage V_{IF} at pin 3.

BTSC-STEREO / SAP / DBX DECODER

GENERAL DESCRIPTION

The TDA3830 is a sound processor for stereo/second audio programme (SAP) baseband signals in accordance with the BTSC-standard for TV receivers and VTRs.

Features

- DBX-decoder, MPX-decoder and SAP-decoder on-chip
- Extensive switching possibilities for the AF outputs and the extra headphone output
- Stereo and SAP signal available at the same time
- Reliable stereo/SAP identification by means of noise detectors
- Integrated filters
- Shrink DIL 32-pin package
- Supply voltage of 5 V
- Power consumption of 0.2 W (typ.)
- DAC control possible for most alignments
- Few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	5	–	V
Supply current		I_P	–	42	–	mA
AF output voltage, pins 23, 24, 7-25*		V_O	–	500	–	mV
Signal-to-noise ratio, weighted		S/N(W)	–	50	–	dB
Stereo channel separation		α	–	26	–	dB
Crosstalk attenuation		αL/N	–	60	–	dB
Total harmonic distortion pins 23 and 24		THD	–	0.5	–	%

* Composite baseband RMS input voltage (100% modulated mono): typ. 100 mV.

PACKAGE OUTLINE

32-lead shrink DIL; plastic (SOT232)

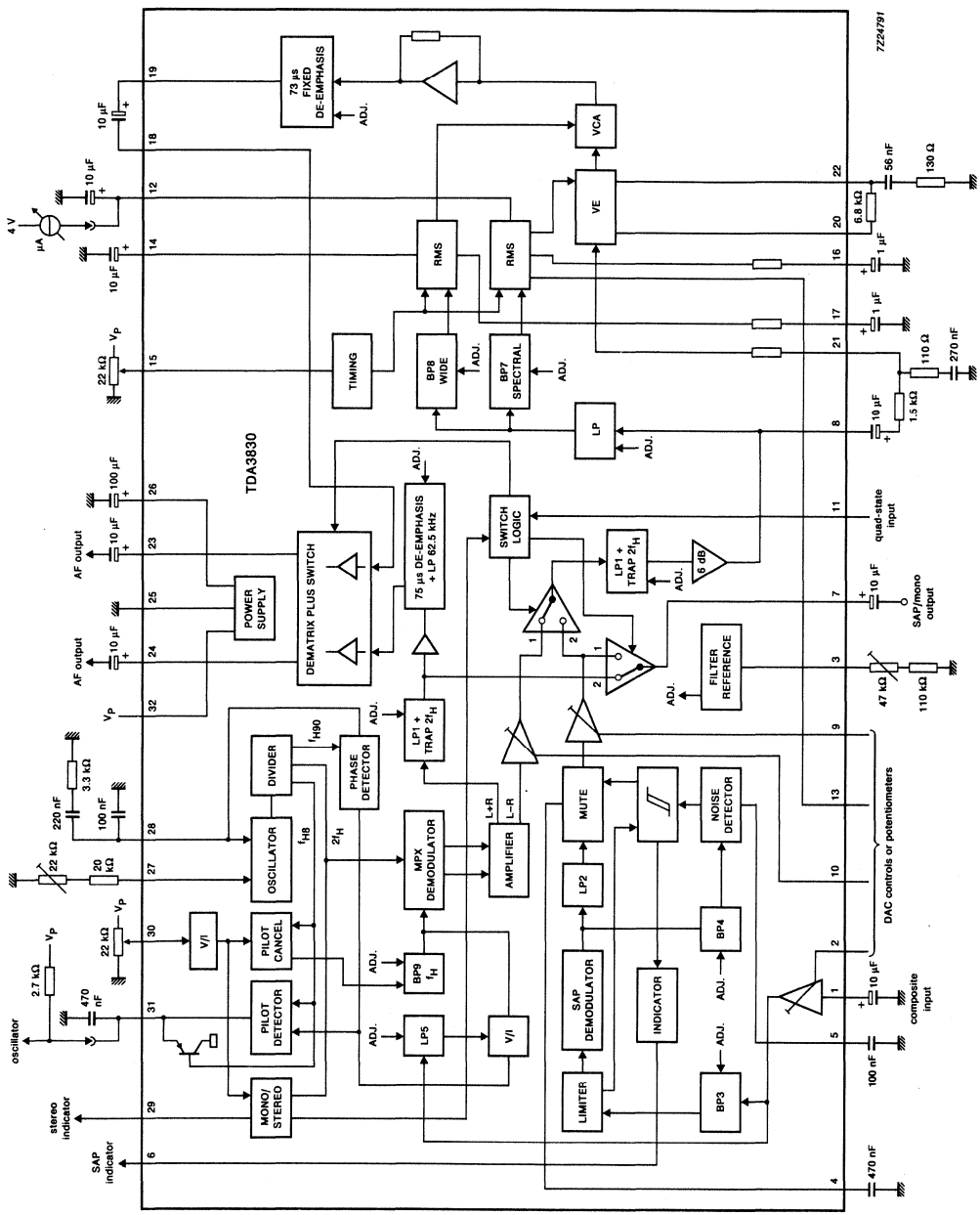


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

pin	description
1	Composite input
2	Input level control
3	Filter adjustment
4	SAP identity smoothing
5	SAP noise detector smoothing
6	SAP indicator output
7	Headphone output
8	Output of SAP/(L + R) without DBX
9	SAP level control
10	(L + R) level control
11	Quad-state input
12	Timing capacitor
13	DBX spectral adjustment
14	Timing capacitor
15	Timing adjustment
16	Spectral RMS-detector smoothing
17	Wideband RMS-detector smoothing
18	Dematrix input
19	DBX-output
20	Time constant for variable emphasis
21	Time constant for variable emphasis
22	DBX-input
23	AF-out (R, SAP or mono)
24	AF-out (L, SAP or mono)
25	Ground
26	Reference voltage smoothing
27	VCO free running frequency adjustment
28	Phase detector loop filter
29	Stereo indicator output
30	Pilot cancelling adjustment
31	Pilot identity smooting and VCO/4 output
32	Power supply

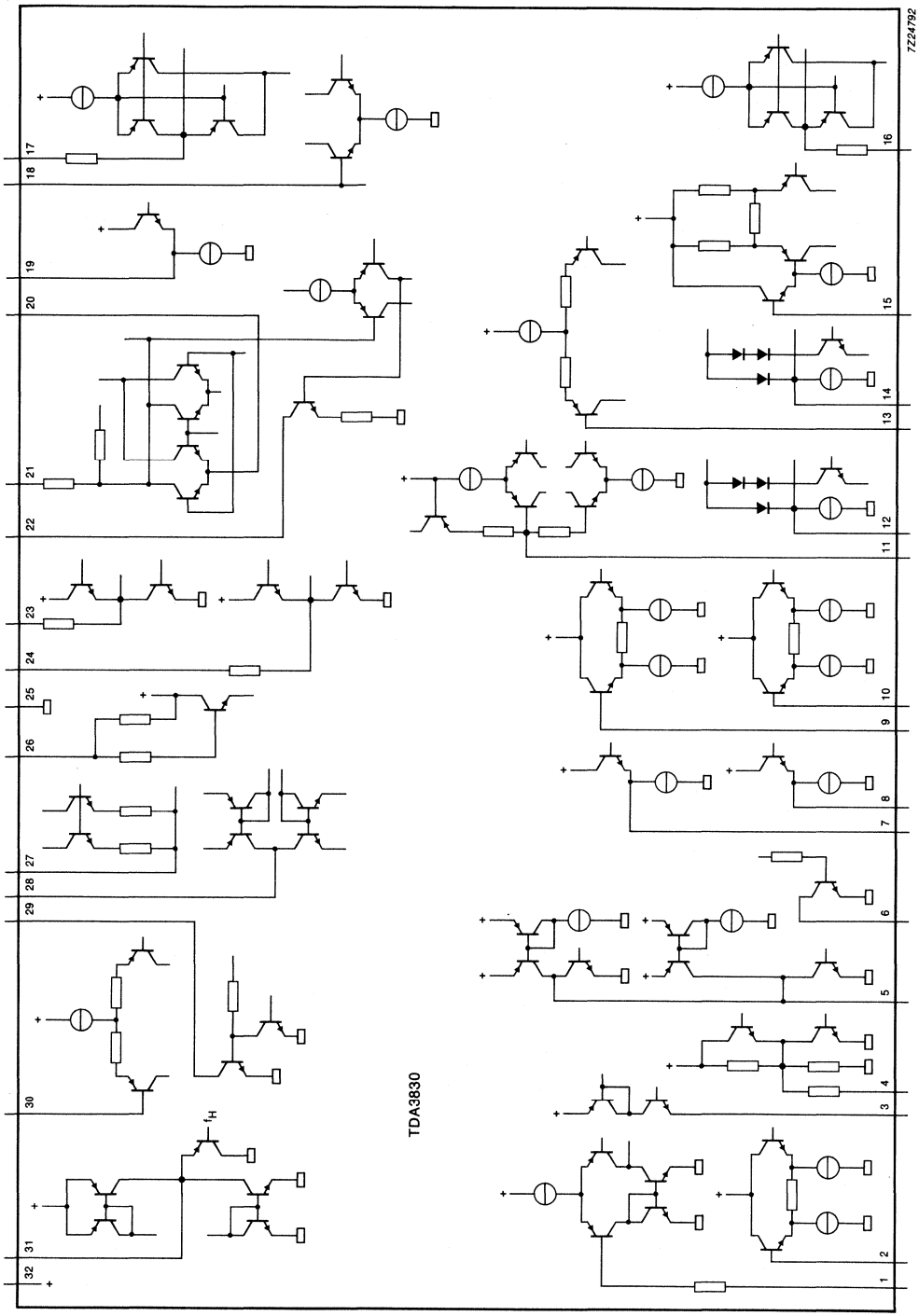


Fig.2 Input/output loading diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	–	8	V
Output current (pins 23, 24, 7-25)		I_O	–	–	5	mA
Composite input		$V_{1\text{-}25}$	–	–	V_P	V
Quad-state input		$V_{11\text{-}25}$	–	–	8	V
Stereo/SAP indication		$I_{6,29}$	–	–	5	mA
Total power dissipation		P_{tot}	–	–	500	mW
Storage temperature range		T_{stg}	−55	–	+150	°C
Operating ambient temperature range		T_{amb}	0	–	+70	°C
ESD protection (all pins)	1.5 kΩ; 100 pF; 5 pulses	V_{ESD}	–	–	±4000	V

DEVELOPMENT DATA

CHARACTERISTICS

Conditions: T_{amb} = 25 °C; V_P = 5 V; MPX: Δf = 25 kHz for L + R (100% modulation), f_{mod} = 1 kHz; SAP: Δf = 10 kHz, f_{mod} = 1 kHz, unless otherwise specified. Measured in the test circuit of Fig.3.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	4.75	5.0	5.35	V
Supply current		I_P	–	42	–	mA
DC input, –output level for pins 1, 7, 8, 21, 19, 18, 23 and 24		$V_{I/O}$	–	0.5 V_P	–	V
Operating ambient temperature range		T_{amb}	0	25	70	°C
Composite input						
Composite input resistance		R_I	14	20	34	kΩ
Composite input signal (RMS) (L + R, all other signals according to BTSC system specification)			70	100	140	mV
Adjustment range			±5	±7.5	–	dB
Control input voltage range			–	1 to 4	–	V
Input current	control voltage = 0.5 V_P	I_I	–	–	5	μA
Pilot threshold (RMS value)	stereo on		–	–	14	mV
	stereo off		5	–	–	mV
Hysteresis			–	2.5	–	dB
Pilot threshold (RMS value)	SAP on		–	–	45	mV
	SAP off		18	–	–	mV
Hysteresis			–	2.0	–	dB
Stereo indication						
Stereo present						
Output voltage		V_O	–	–	0.5	V
Output current		I_O	3	–	–	mA
Stereo not present						
Output voltage		V_O	V_P–0.5	–	V_P	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SAP indication						
SAP present						
Output voltage		V_O	–	–	0.5	V
Output current		I_O	3	–	–	mA
SAP not present						
Output voltage		V_O	V_P–0.5	–	V_P	V
Quad-state terminal	see Table 1					
Quad-state level						
Mono						
Input voltage		V_I	V_P+1.4	–	8	V
Input current	V_{11} = 7.2 V	I_I	–	–	0.3	mA
Stereo						
Input voltage		V_I	V_P/2+1	–	V_P	V
Input current		I_I	–	–	5	μA
Mono/SAP						
Input voltage		V_I	0	–	V_P/2–1	V
Input current		I_I	–	–	15	μA
SAP						
Input voltage		V_I	V_P/2–0.4	–	V_P/2+0.4	V
Input current		I_I	–	–	15	μA
SAP/mono output						
Output level (RMS value)	note 1	V_O	–	500	–	mV
Output resistance		R_O	70	100	130	Ω
Load resistance		R_L	10	–	–	kΩ
Load capacitance		C_L	–	–	500	pF
Frequency response 50 Hz to 10 kHz (Mono, external 75 μs de-emphasis)			–3	–	–	dB
Total harmonic distortion (1 kHz)	SAP - signal	THD	–	1	–	%
Total harmonic distortion (1 kHz)	Mono - signal	THD	–	0.5	–	%
Signal-to-noise ratio, weighted (CCIR 468-2)	Δf = 25 kHz; f_{mod} = 1 kHz; 75 μs de-emphasis; mono	S/N(W)	–	50	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Audio outputs						
Output voltage (RMS value)	note 1	V_O	–	500	–	mV
Output voltage headroom			–	6	–	dB
Output resistance		R_O	–	100	130	Ω
Load resistance		R_L	10	–	–	kΩ
Load capacitance		C_L	–	–	500	pF
Switching offset voltage (stereo/mono/SAP)			–	–	150	mV
L, R frequency response	50 Hz to 10 kHz		–3	–	–	dB
	12 kHz related to 1 kHz		–	–	–3	dB
SAP frequency response	50 Hz to 8 kHz		–3	–	–	dB
Total harmonic distortion for L, R (1 kHz)		THD	–	0.5	–	%
Total harmonic distortion for SAP (1 kHz)		THD	–	0.25	–	%
Signal-to-noise ratio weighted for mono (CCIR 468-2)	L + R: Δf = 25 kHz; f_{mod} = 1 kHz	S/N(W)	–	50	–	dB
Crosstalk, L, R into SAP at 1 kHz			50	60	–	dB
Crosstalk, SAP into L, R at 1 kHz			50	60	–	dB
Output voltage difference between L and R	250 Hz to 6.3 kHz		–	–	3	dB
Output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz		–	–	3	dB
Channel separation						
According to DBX requirements: 10% 75 μs equiv. input modulation	100 Hz to 5 kHz		20	26	–	dB
1% to 100% 75 μs equiv. input modulation	100 Hz to 5 kHz		15	20	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
DBX section						
Control input voltage range						
Stereo wideband level			–	1 to 4	–	V
SAP wideband level			–	1 to 4	–	V
Spectral band level			–	1.8 to 3.2	–	V
Input current	control voltage = 0.5 V_P		–	–	5	μA
Wideband RMS detector release rate			112.5	125	137.5	dB/s
Spectral RMS detector release rate			343	381	419	dB/s
Timing current for nominal release rate of spectral RMS detector		I_{12}	–	22.5	–	μA
Adjustment range	note 2		–	11 to 45	–	μA
Timing current for nominal release rate of wideband RMS detector		I_{14}	–	$7.5(I_{12}/3)$	–	μA
Adjustment range	note 2		–	4 to 15	–	μA
Adjustment voltage			–	1.5 to 3.8	–	V
Voltage controlled oscillator						
Nominal VCO frequency	note 3	f_{VCO}	–	$62.94(4f_H)$	–	kHz
Capture range (nominal pilot)			–	–	1	kHz
Temperature coefficient			–	–	50	10^{-6}/K

DEVELOPMENT DATA

Notes to the characteristics

1. Can also be aligned to 600 mVrms (Identification threshold and AF output headroom will be decreased by 1.6 dB).
2. I_{12}, I_{14} can be measured via an ammeter connected to 4 V (3.5 to 4.1 V).
3. Adjustable at pin 27, measurement (f_H) at pin 7 with a 2.7 kΩ resistor connected between V_P and pin 31.
4. Requirements for the MPX/SAP input signal to ensure proper system performance:
   a. Maximum variation of MPX/SAP signal under operating conditions: to be found (1 dB)
   b. 3 dB bandwidth, Δf = 25 kHz: 50 Hz to 100 kHz
   c. THD (L + R, Δf = 25 kHz, f_{mod} = 1 kHz): to be found (0.2%).
   d. S/N CCIR 468-2 weighted (L + R, Δf = 25 kHz for sound carrier f_{mod} = 1 kHz, 75 μs de-emphasis; with critical picture modulation): $>$ 44 dB.
   e. Spectral spurious attenuation, (mainly nxf_H; L + R, Δf = 25 kHz for sound carrier, f_{mod} = 1 kHz, 50 Hz to 100 kHz, no de-emphasis): 30 dB.
   f. Maximum white-noise level (unweighted, 200 Hz to 100 kHz) to avoid malfunctioning of the identification circuits: 500 mVrms.

Table 1 Quad-state terminal

quad-state	SAP carrier	AF outputs		SAP/mono output
		pin 24	pin 23	pin 7
mono	on	mono	mono	SAP without DBX
stereo	on	L	R	SAP without DBX
SAP	on	SAP	SAP	mono
mono/SAP	on	mono	SAP	SAP without DBX
mono	off	mono	mono	mono
stereo	off	L	R	mono
SAP	off	L	R	mono
mono/SAP	off	mono	mute	mono

DEVELOPMENT DATA

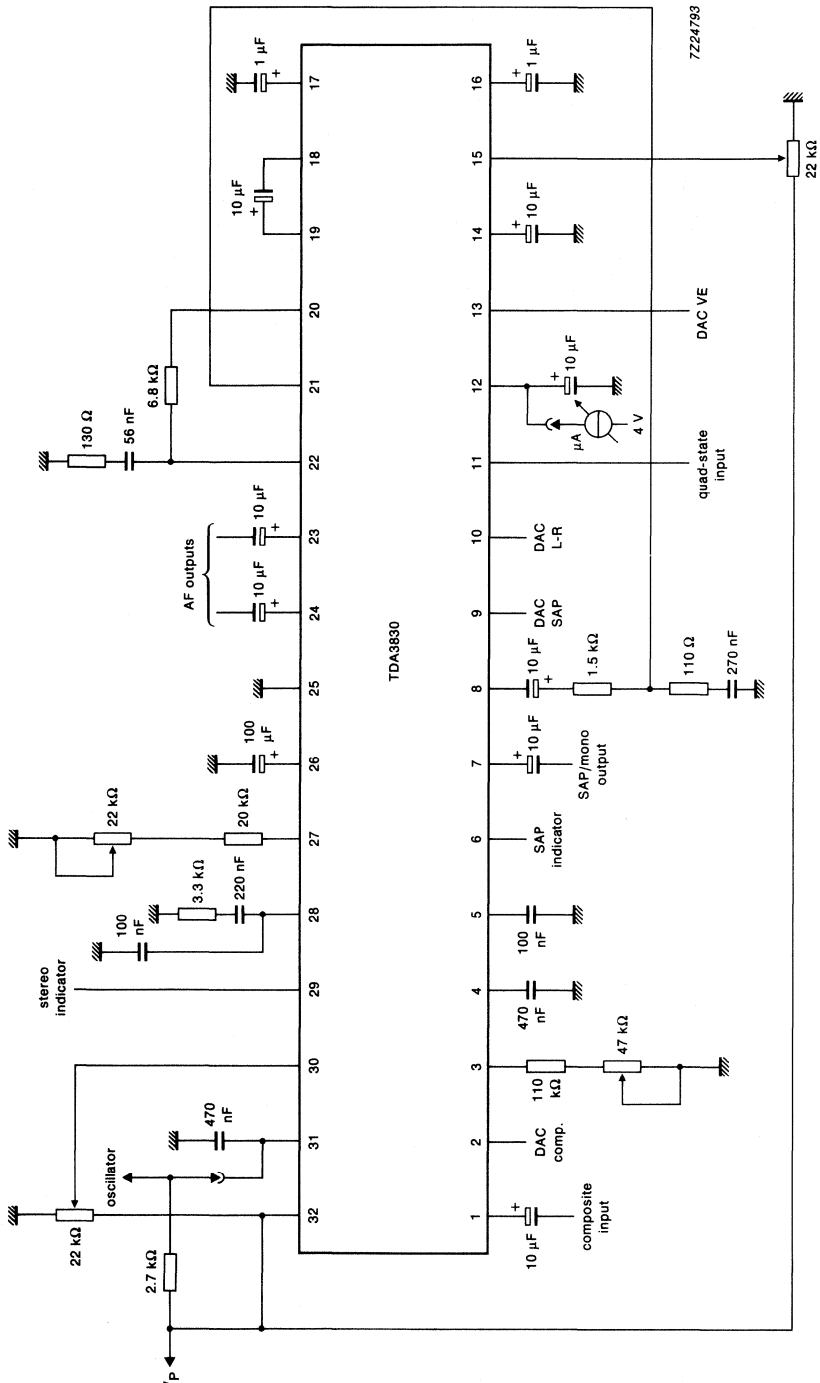


Fig.3 Test circuit.

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA3833

BTSC-stereo / SAP / DBX decoder and DBX expander

FEATURES

- DBX decoder, MPX decoder and SAP decoder on chip
- Extensive switching possibilities for the AF outputs and the extra headphone output
- Stereo and SAP signal available simultaneously
- Reliable stereo/SAP identification by means of the noise detector
- Integrated filters
- DAC control possible for most alignments
- Few external components
- Low power consumption (200 mW)
- +5 V supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 32)	-	5	-	V
I_P	supply current	-	42	-	mA
V_i	input signal, 100% modulated, mono (RMS value, pin 1)	-	100	-	mV
V_o	AF output signal (RMS value, pins 7, 23 and 24)	- -	550	-	mV
S/N(W)	signal-to-noise ratio, weighted	-	50	-	dB
S/N	signal-to-noise ratio (RMS)	-	60	-	dB
α_{CH}	stereo channel separation	-	26	-	dB
α_{CR}	crosstalk attenuation	-	60	-	dB
THD	total harmonic distortion	-	0.2	-	%

GENERAL DESCRIPTION

The TDA3833 is a sound processor for stereo/second audio programme (SAP) baseband signals in accordance with the BTSC standard for television receivers and video tape recorders.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3833	32	shrink DIL	plastic	SOT232

BTSC-stereo / SAP / DBX decoder and DBX expander

TDA3833

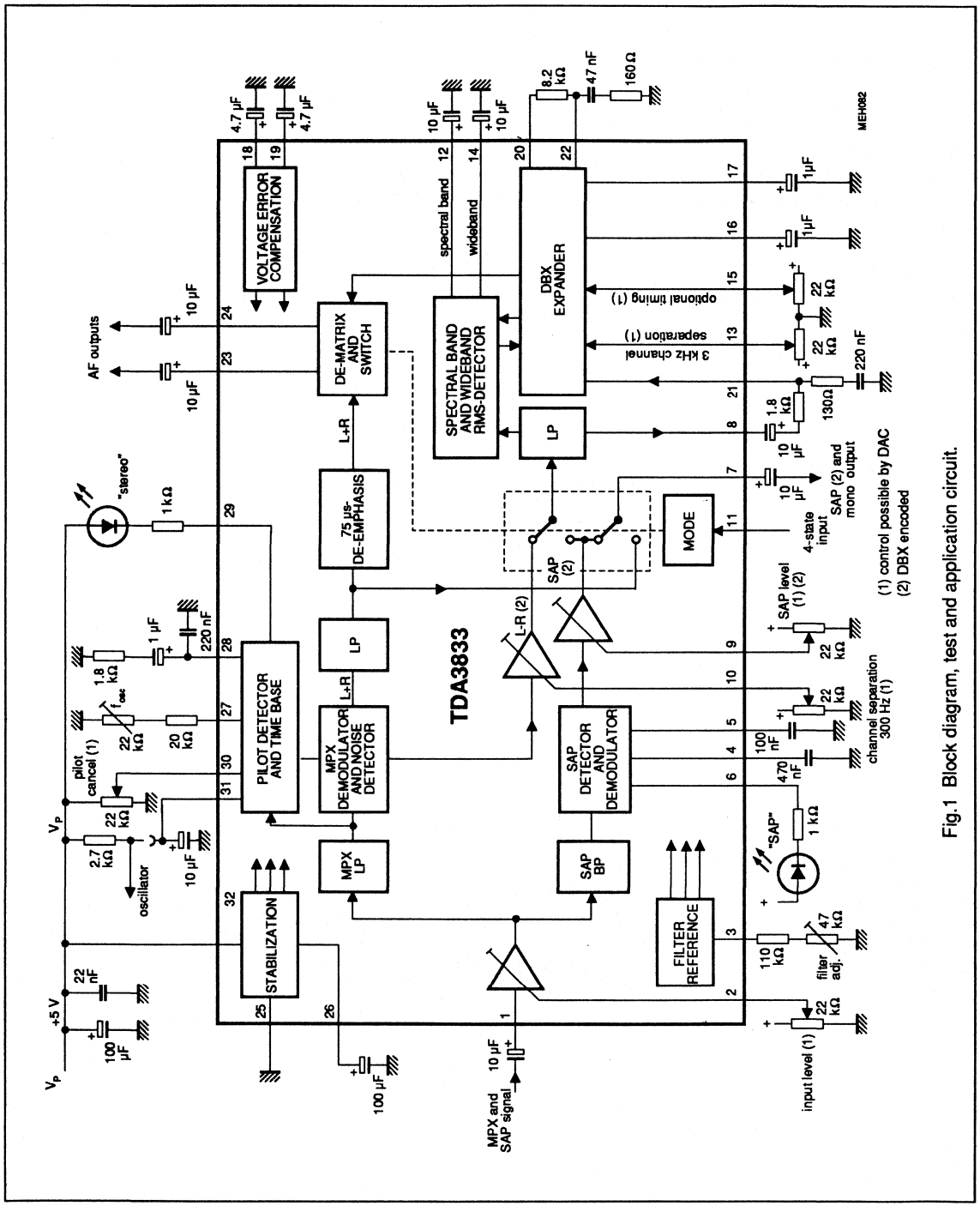


Fig.1 Block diagram, test and application circuit.

BTSC-stereo / SAP / DBX decoder and DBX expander

TDA3833

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	composite input signal (MPX/SAP)
ILV	2	input level control
f_{ref}	3	adjustment of filter reference
C_{SAP}	4	SAP identity smoothing capacitor
C_{ND}	5	SAP noise detector smoothing capacitor
SAPI	6	SAP indicator output (sink)
$V_{o\ HP}$	7	SAP/mono headphone output
$V_{o\ SAP}$	8	output signal SAP/(L – R) without DBX
SAPLV	9	SAP level control
LRLV	10	(L – R) level control
MODE	11	4-state mode control
$C1_{SPB}$	12	spectral band timing capacitor
DBXLV	13	DBX spectral adjust
$C1_{WB}$	14	wideband timing capacitor
DBXT	15	DBX timing adjust
$C2_{SPB}$	16	spectral RMS-detector smoothing capacitor
$C2_{WB}$	17	wideband RMS-detector smoothing capacitor
$C1_{DC}$	18	DC decoupling capacitor 1 for offset compensation
$C2_{DC}$	19	DC decoupling capacitor 2 for offset compensation
EMPH1	20	time constant for variable emphasis
DBXIN	21	DBX signal input
EMPH2	22	time constant for variable emphasis
V_{oAF1}	23	AF output signal right/SAP or mono
V_{oAF2}	24	AF output signal left/SAP or mono
GND	25	ground (0 V)
C_{ref}	26	smoothing capacitor for internal reference voltage
VCO	27	VCO free running frequency adjustment
LOOP	28	phase detector loop filter
STERI	29	stereo indicator output (sink)
PILOT	30	pilot cancel adjustment
C_{pil}	31	pilot detector smoothing capacitor, VCO/4 output
V_P	32	+5 V supply voltage

PIN CONFIGURATION

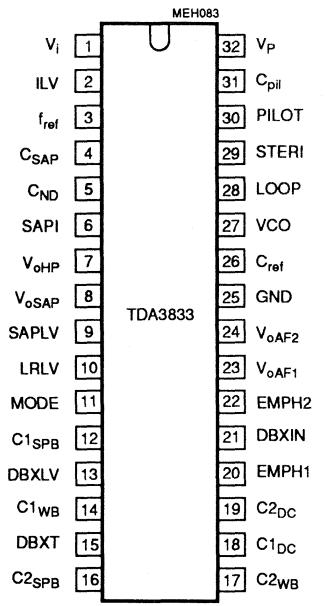


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 32)	0	8	V
V_1	composite input voltage	0	V_P	V
V_{11}	MODE input voltage	0	8	V
$I_{7, 23, 24}$	output current (AF outputs)	0	5	mA
$I_{6, 29}$	output current (indication outputs)	0	5	mA
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins	-	±4000	V

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; for MPX: Δf = 25 kHz for L+R (100% modulation); f_{mod} = 1 kHz; and for SAP: Δf = 10 kHz; f_{mod} = 1 kHz, unless otherwise specified. Measurements taken in Fig.1 including all adjustments.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 32)		4.75	5	5.35	V
I_P	supply current		-	42	-	mA
V_n	DC input/output voltage at pins 1, 7, 8, 18, 19, 21, 23 and 24		-	$V_P/2$	-	V
MODE select 4-state input see Table 1						
V_{11}	input voltage for mono/SAP		0	-	$V_P/2-1$	V
	input voltage for SAP		$V_P/2-0.4$	-	$V_P/2+0.4$	V
	input voltage for stereo		$V_P/2+1$	-	V_P	V
	input voltage for mono		$V_P+1.4$	-	8	V
I_{11}	input current for mono/SAP		-	-	15	µA
	input current for SAP		-	-	15	µA
	input current for stereo		-	-	5	µA
	input current for mono	V_{11} = 7.2 V	-	-	300	µA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite input, pin 1						
R_i	input resistance on pin 1		14	20	26	kΩ
V_i	input signal on pin 1 (RMS value)	note 1				
	L+R (all other signals according to BTSC system specification)		70	100	140	mV
	pilot threshold for MPX	stereo on	-	-	16	mV
		stereo off	5	-	-	mV
	hysteresis of threshold	MPX	-	2.5	-	dB
	pilot threshold for SAP	SAP on	-	-	37	mV
		SAP off	16	-	-	mV
	hysteresis of threshold	SAP	-	2	-	dB
G_v	gain control range	dependent on V_2	±5	±7.5	-	dB
V_2	control voltage range		-	1 to 4	-	V
I_2	input current pin 2	$V_2 = V_P/2$	-	-	5	µA
Voltage controlled oscillator (VCO), pin 27						
f_{VCO}	nominal VCO frequency ($4f_H$)	note 2	-	62.94	-	kHz
Δf_{29}	capture range	nominal pilot	-	-	1	kHz
TC	temperature coefficient		-	-	50	10^{-6}/K
Stereo indication output, pin 29						
V_{29}	output voltage range	stereo present	-	-	0.5	V
		stereo not present	V_P–0.5	-	V_P	V
I_{29}	output current active LOW	stereo present	3	-	-	mA
SAP/Mono output, pin 7						
V_o	output signal (RMS value, pin 7)	note 3	-	550	-	mV
	output signal headroom	mono	-	9.5	-	dB
R_7	output resistance		-	100	200	Ω
R_L	load resistance		10	-	-	kΩ
C_L	load capacitance		-	-	500	pF
THD	total harmonic distortion	SAP signal	-	0.5	-	%
		mono signal	-	0.2	-	%
B	frequency response 50 to 10000 Hz	mono, external 75 µs de-emphasis	–3	-	-	dB
S/N(W)	weighted signal-to-noise ratio (CCIR 468-3)	mono, external 75 µs de-emphasis	-	50	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SAP indication output, pin 6						
V_6	output voltage range	SAP present	-	-	0.5	V
		SAP not present	V_P–0.5	-	V_P	V
I_6	output current active LOW	SAP present	3	-	-	mA
Audio outputs, pins 23 and 24						
V_o	output signal (RMS value, pins 23, 24)	note 3	-	550	-	mV
	output signal headroom		-	9.5	-	dB
$\Delta V_{L,R}$	output signal difference between L and R	f = 250 to 6300 Hz	-	-	3	dB
ΔV_o	output signal difference after switching from L or R to SAP	f = 250 to 6300 Hz	-	-	3	dB
$\Delta V_{23, 24}$	DC offset voltage after switching	stereo/mono/SAP	-	-	±100	mV
$R_{23, 24}$	output resistance		-	200	300	Ω
R_L	load resistance		10	-	-	kΩ
C_L	load capacitance		-	-	500	pF
THD	total harmonic distortion	L and R signal	-	0.2	-	%
		SAP signal	-	0.5	-	%
B	L and R frequency response	f = 50 to 10000 Hz	–3	-	-	dB
		12 kHz related to 1 kHz	-	–3	-	dB
	SAP frequency response	f = 50 to 8000 Hz	–3	-	-	dB
S/N(W)	weighted signal-to-noise ratio	L+R signal; CCIR 468-3	-	50	-	dB
S/N	unweighted signal-to-noise ratio (RMS value)	L + R signal; f = 20 to 20000 Hz	-	60	-	dB
α_{CR}	crosstalk	L or R into SAP	50	63	-	dB
		SAP into L or R	50	70	-	dB
α_{CH}	channel separation (according to DBX requirements)	f = 100 to 5000 Hz				
		10% 75 µs equivalent input modulation	20	26	-	dB
		1 to 100% 75 µs equivalent input modulation	15	20	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DBX section						
V_9	SAP level control voltage range		-	1 to 4	-	V
V_{10}	(L–R) level control voltage range		-	1 to 4	-	V
V_{13}	spectral band level control voltage range		-	1.8 to 3.2	-	V
$I_{9, 10, 13}$	input current	$V_I = 0.5\ V_P$	-	-	5	µA
S_1	spectral RMS-detector release rate		343	381	419	dB/s
I_{12}	timing current for nominal release rate of spectral RMS-detector	note 4	-	22.5	-	µA
	current adjustment range		-	11 to 45	-	µA
S_2	wideband RMS-detector release rate		112.5	125	137.5	dB/s
I_{14}	timing current for nominal release rate of wideband RMS-detector	note 4 $0.33\ I_{12}$	-	7.5	-	µA
	current adjustment range		-	4 to 15	-	µA
V_{15}	timing adjustment		-	1.5 to 3.8	-	V

Notes to the characteristics

1. Requirements for the MPX/SAP input signal to ensure correct system performance:
   a. Maximum variation of MPX/SAP signal under operating conditions: to be found (1 dB).
   b. 3 dB bandwidth ≥130 kHz (Δf = 25 kHz).
   c. THD (L + R, Δf = 25 kHz, f_{mod} = 1 kHz): 0.2%.
   d. S/N(W), weighted in accordance to CCIR468-3 (L+R, Δf = 25 kHz for sound carrier f_{mod} = 1 kHz, 75 µs de-emphasis; with critical picture modulation): S/N(W) > 44 dB; with sync only: S/N(W) > 54 dB.
   e. Spectral spurious attenuation: 40 dB (mainly n x f_H ; L + R, Δf = 25 kHz for sound carrier, f_{mod} = 1 kHz, 50 Hz to 100 kHz, no de-emphasis).
   f. Maximum white noise level (unweighted, 200 Hz to 100 kHz) to avoid malfunctioning of the identification circuits: 500 mV (RMS).
2. Adjustable on pin 27, measurement (f_H) on pin 7 with a 2.7 kΩ resistor connected between V_P and pin 31.
3. Can also be aligned to 600 mV (RMS), then identification threshold and AF output headroom will be decreased by 1.6 dB.
4. I_{12} and I_{14} can be measured via an ammeter connected to 4 V (3.5 to 4.1 V).

Table 1 MODE select, 4-state terminal pin 11

MODE	V_{11} (V_P = 5 V) (V)	SAP carrier	AF outputs pin 23	AF outputs pin 24	SAP/mono output pin 7
mono	8	on	mono	mono	SAP without DBX
stereo	V_P	on	right	left	SAP without DBX
SAP	$V_P/2$	on	SAP	SAP	mono
mono/SAP	0	on	SAP	mono	SAP without DBX
mono	8	off	mono	mono	mono
stereo	V_P	off	right	left	mono
SAP	$V_P/2$	off	right	left	mono
mono/SAP	0	off	mute	mono	mono

Philips Components

Data sheet	
status	Preliminary specification
date of issue	September 1990

TDA3842/T

Multistandard TV IF amplifier and demodulator with TV signal identification

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC for negative modulation, e.g. B/G
- Peak white AGC for positive modulation, e.g. L
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit, suitable for MAC-on-cable

GENERAL DESCRIPTION

The TDA3842/T is a bipolar integrated circuit for vision IF-signal processing in multistandard TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
$V_{1\text{-}20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	f = 38.9 MHz	–	70	–	μV
	minimum IF input signal for TV ident at pin 6 (RMS value)	maximum G_V	–	20	40	μV
V_o	video output signal (pin 12)	buffered	–	2.0	–	V
G_V	IF voltage gain control range		–	66	–	dB
S/N_{video}	signal-to-noise ratio	$V_{1\text{-}20}$ = 10 mV	55	60	–	dB
V_{18}	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	μA/kHz
RR_{video}	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3842	20	DIL	plastic	SOT146
TDA3842T	20	DIL	plastic	SO20; SOT163A

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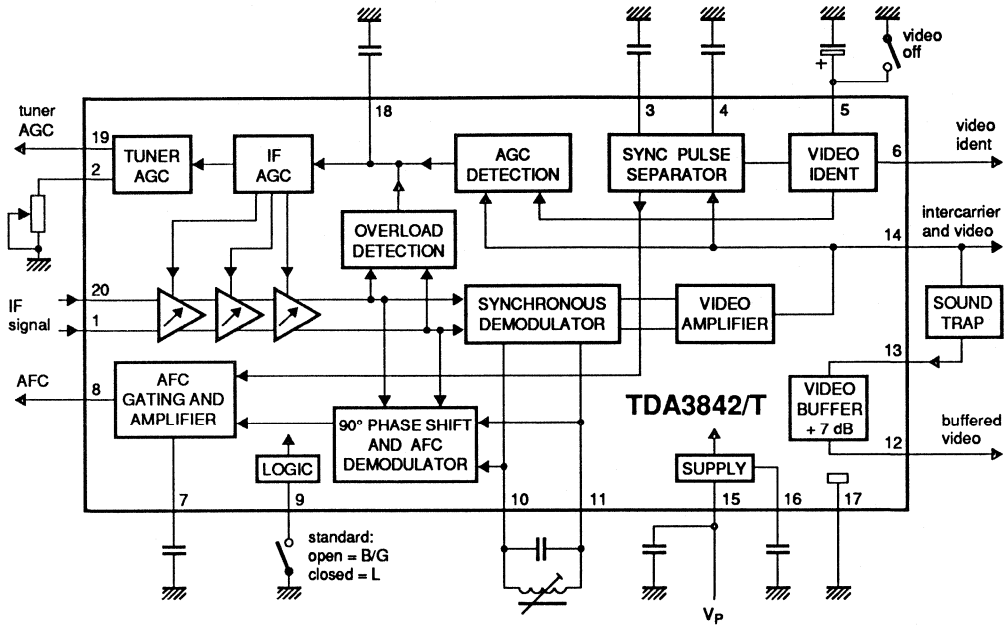

Fig.1 Block diagram.

PIN CONFIGURATION

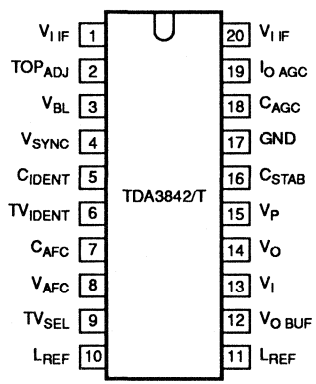

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I\,IF}$	1	IF input (balanced)
TOP_{ADJ}	2	tuner AGC take-over point adjustment
V_{BL}	3	black level voltage
V_{SYNC}	4	sync pulse amplitude voltage
C_{IDENT}	5	ident capacitor
TV_{IDENT}	6	video ident (identification) output
C_{AFC}	7	AFC capacitor
V_{AFC}	8	AFC output signal
TV_{SEL}	9	video standard selection switch
L_{REF}	10	LC reference tuned circuit
L_{REF}	11	LC reference tuned circuit
$V_{O\,BUF}$	12	buffered video output signal
V_I	13	video input signal for buffer
V_O	14	video output signal with intercarrier signal
V_P	15	supply voltage
C_{STAB}	16	supply voltage stabilization
GND	17	ground
C_{AGC}	18	AGC capacitor
$I_{O\,AGC}$	19	tuner AGC output signal
$V_{I\,IF}$	20	IF input (balanced)

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FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video ident (identification)
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer
15. Standard switch

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal polarity is switched according to the TV standard selected. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth. The DC level is shifted according to the TV standard to provide the same sync level for positive and negative IF modulation.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

With negative modulation (B/G) a peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion

Positive modulation (L) uses a peak white AGC detector.

To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector. The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When however, the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video ident (identification) output. The bandwidth is limited to reduce the noise and increase the ident sensitivity.

11. Video ident (identification)

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier is fed to the AFC demodulator. The demodulated signal is fed to the AFC gating stage.

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FUNCTIONAL DESCRIPTION (continued)

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector output).

At positive modulation the AFC operates continuously.

AFC function can externally be switched off for test purposes. For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

15. Standard switch

The operating mode of the AGC detector and video IF demodulator for positive and negative IF modulation is selected by the logic level on pin 9.

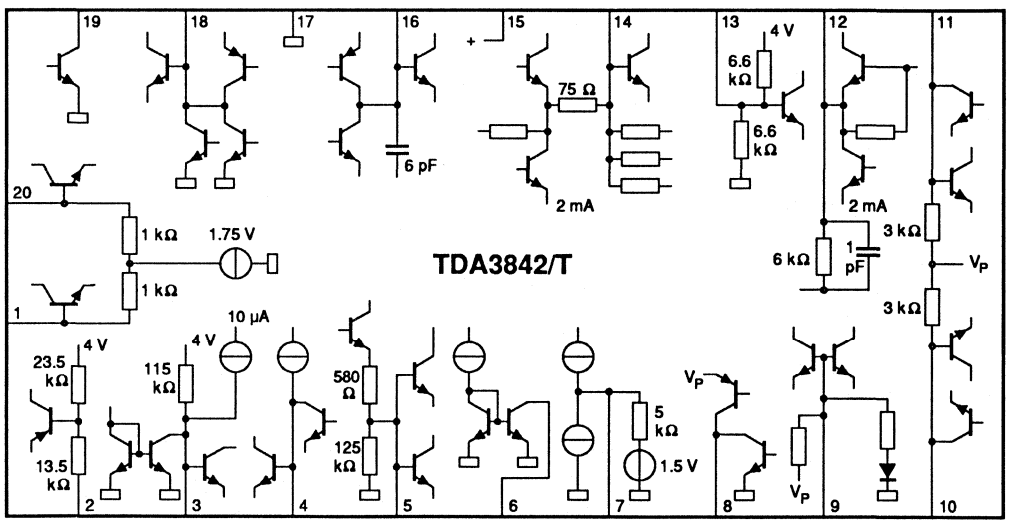

Fig.3 Internal circuits.

Multistandard TV IF amplifier and demodulator with TV signal identification

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 15)	DIL-package	–	8.8	V
		SO-package	–	6.0	V
V_{19}	tuner AGC voltage		–	13.2	V
V_8	permissible voltage at AFC output		–	V_P	V
I_{15}	supply current		–	55	mA
T_{stg}	storage temperature range		–25	+ 150	°C
T_{amb}	operating ambient temperature range		0	+ 70	°C
V_{ESD}	ESD sensitivity		–	± 300	V

CHARACTERISTICS

All voltages are measured to GND (pin 17); V_P = 5 V and T_{amb} = 25 °C; measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R_i	input resistance (pins 1 and 20)		–	2	–	kΩ
C_i	input capacitance (pins 1 and 20)		–	1.5	–	pF
$V_{1\text{-}20(rms)}$	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G_V; note 1	100	–	–	mV
G_V	gain control range		63	66	–	dB
IF AGC: negative modulation						
I_{18}	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video ident	–	13	–	μA
	charging current AGC capacitor	without video ident	–	35	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_1	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms

Multistandard TV IF amplifier and demodulator with TV signal identification

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AGC: standard L		note 2				
I_{18}	leakage current AGC capacitor		–	–	20	nA
	charging current AGC capacitor	with video ident	–	280	–	nA
		without video ident	–	22	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_2	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	300	–	ms
Tuner AGC		note 3				
$V_{1\text{-}20(rms)}$	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R_2 = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R_2 = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I_{19}	tuner AGC output current	V_{19} = 0.5 V	1	2	–	mA
Sync demodulator and video amplifier		note 4				
V_{14}	composite video output signal		0.9	1.0	1.1	V
	sync level voltage	standard B/G	–	1.5	–	V
	zero carrier level voltage	negative modulation	–	2.6	–	V
		positive modulation	–	1.47	–	V
I_{14}	output current	DC and AC	–	–	± 1.0	mA
R_{14}	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	$C_{load} \leq$ 20 pF (pin 14)	7	8	–	MHz
V_{14}	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V_{12}	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I_{12}	output current	DC and AC	–	–	± 1.0	mA
R_{12}	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	$C_{load} \leq$ 20 pF (pin 12)	–	10	–	MHz
R_i	input resistance (pin 13)		–	3.3	–	kΩ
C_i	input capacitance (pin 13)		–	2	–	pF

Multistandard TV IF amplifier and demodulator with TV signal identification

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall video performance (see Fig.6)		R_{13-14} = 270 Ω				
V_o	video output signal (pin 12)	negative modulation	–	2	–	V
		positive modulation (note 4)	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	$C_{load} \leq$ 20 pF (pin 12)	7	8	–	MHz
S/N	signal to noise ratio (see Fig.7)	note 5	55	60	–	dB
α_1	intermodulation for blue (note 6)	f = 1.1 MHz f = 3.3 MHz	56 62	58 –	– –	dB dB
α_2	intermodulation for yellow (note 6)	f = 1.1 MHz f = 3.3 MHz	53 60	56 –	– –	dB dB
α_3	signal harmonic suppression		–	26	–	dB
V_5	video switch off voltage	note 7	–	–	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	–	dB
ΔG	differential gain	EBU test line 330	–	2	–	%
ΔΦ	differential phase	EBU test line 330	–	2	–	deg
ΔV/V	variation of video output signal (pin 14)	gain control 50 dB; V_{1-20} = 0.3 to 100 mV_{rms}	–	–	0.5	dB
V_{res1}	residual vision carrier (pin 12)		–	1	–	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		–	1	–	mV
Video identification						
$V_{1-20(rms)}$	minimum IF input signal for TV ident at pin 14 (RMS value)	maximum G_V	–	20	40	μV
V_6	video ident voltage (signal unidentified)	V_{1-20} = < 40 μV_{rms} I_6 = 0.5 mA	–	–	0.4	V
	video ident voltage (signal identified)	$V_{1-20} = \geq 40\ \mu V_{rms}$ $I_6 = -1\ \mu A$	4.5	–	–	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	x 10^{-3}
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 8	–	13	–	dB
I_5	allowed leakage current		–	–	3	μA
	sync pulse suppression for correct TV signal identification		–	–	75	%
t_d	delay time of mute output signal		–	100	150	ms

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC (see Fig.9 and Fig.10)		note 9				
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	–	4.7	V
	lower output voltage		0.3	–	0.7	V
S	control steepness	QB = 40; V_{1-20} = 10 mV_{rms}	–	2	–	µA/kHz
I_7	leakage current at AFC gating		–	–	± 1	µA
Standard switch						
V_9	voltage for negative modulation	standard switch open	2.5	n.c.	V_P	V
	voltage for positive modulation (L)	standard switch closed	0	–	0.8	V

Notes to the characteristics

1. The video signal is still gain-controlled, V_{14} = 1 V_{p-p}, but intermodulation figures are degraded.
2. In multi-standard applications the capacitor at pin 18 must be a low-leakage (foil) type.
3. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
4. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.2). The IF input signal is fed from 50 Ω via a 1:1 transformer, DSB, to pins 1 and 20. With a 10 mV_{rms} IF input signal, the residual vision carrier is:
   = 10 % for white (standard B/G),
   = 3 % for sync (standard L).
5. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

$$S/N = \frac{V_{14\ (black\ to\ white)}}{V_{14\ noise}\ (RMS,\ black)}$$

6. Intermodulation figures are defined as follows:

$$\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4\ MHz}{V_o \text{ at } 1.1\ MHz} + 3.6\ dB$$

and

$$\alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4\ MHz}{V_o \text{ at } 3.3\ MHz}$$

7. When $V_5 < 1$ V (short-circuited ident capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to "zero carrier level ("ultra white" (2.6V) for negative modulation or "top sync" (1.5 V) for positive modulation).
   During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3$ µA).
8. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
9. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz.

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842/T

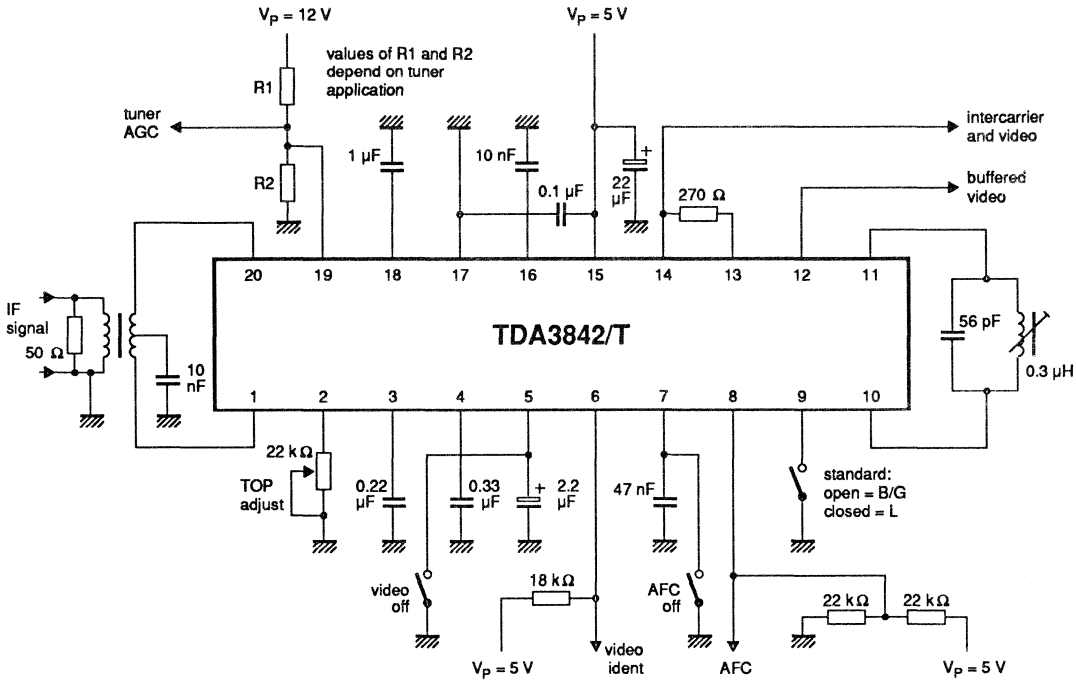


Fig.4 Test circuit.

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842/T

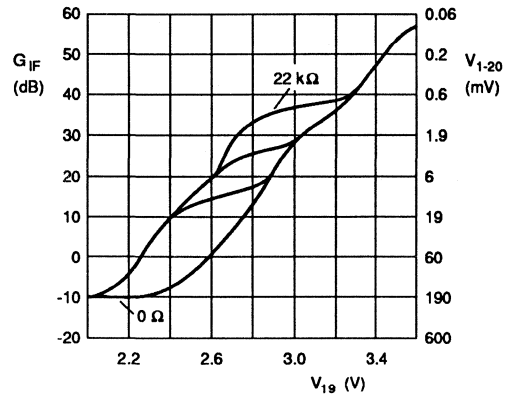


Fig.5 AGC characteristics with different values of R_2.

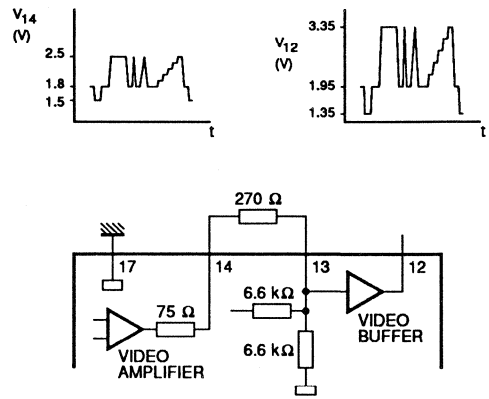


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

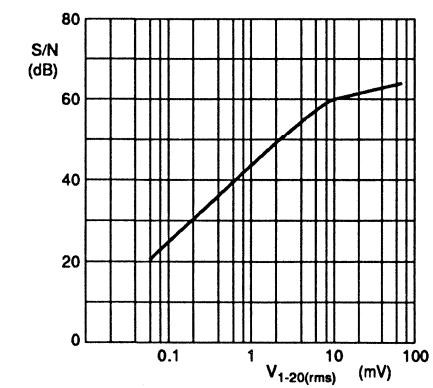
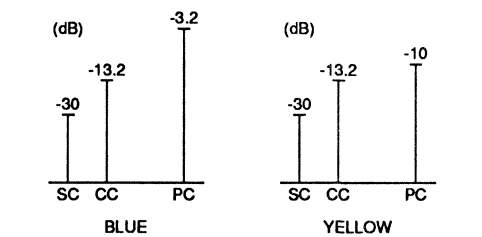


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound trap attenuation: 17 dB.

Fig.8 Input conditions for intermodulation measurements.

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842/T

APPLICATION INFORMATION

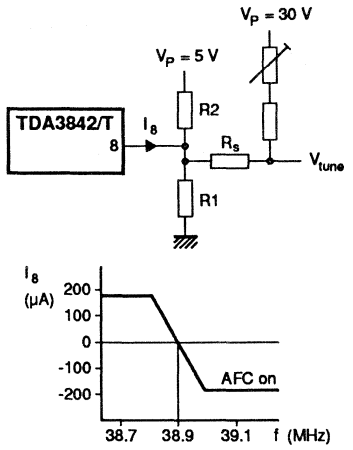


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

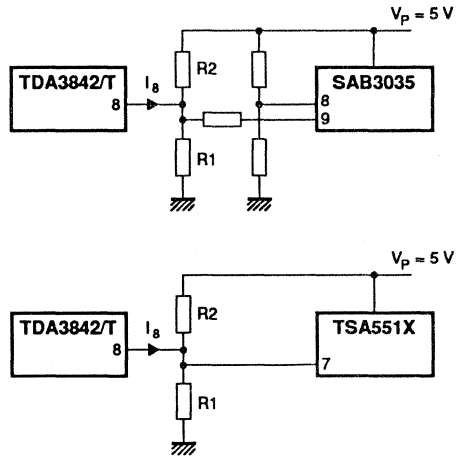
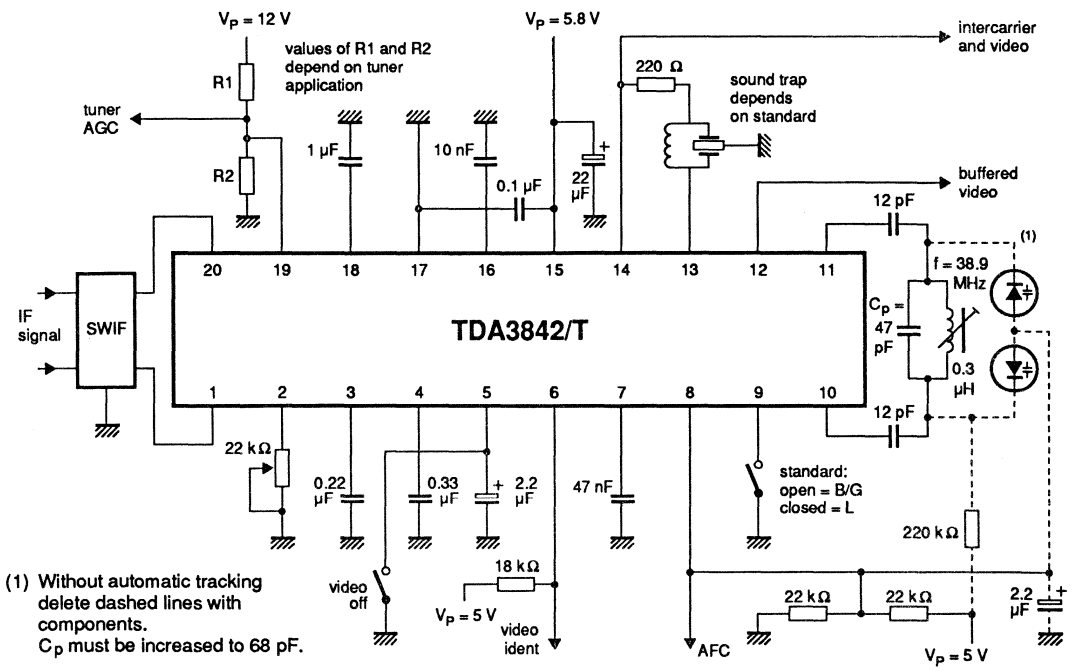


Fig.10 AFC interfacing for μP controlled systems.



(1) Without automatic tracking delete dashed lines with components.
C_p must be increased to 68 pF.

Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

APPLICATION INFORMATION (continued)

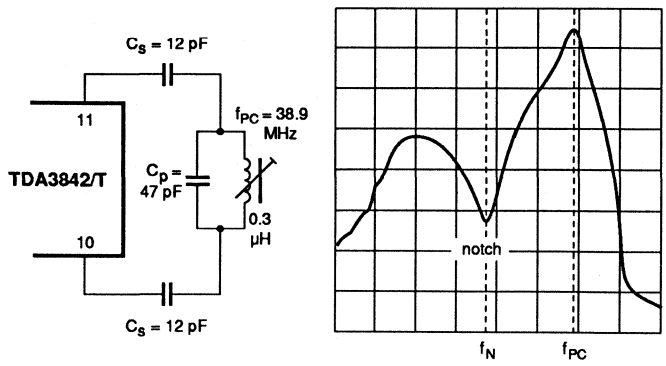


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

Note to Fig.12

Recommended for reception of data signals e.g. in Teletext and D2-MAC. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_S and C_P are calculated as follows:

$$C_S = 2\,C_P\left\{\frac{f_{PC}^2}{f_N^2} - 1\right\}$$

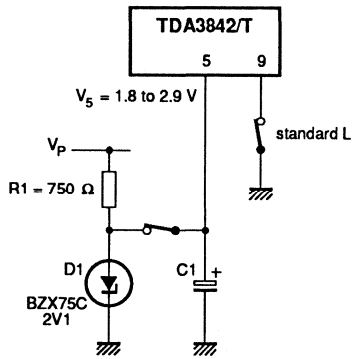


Fig.13 Modification of Fig.11 for MAC/D2-MAC application.

Note to Fig.13

When the TDA3842/T is used in a MAC/D2-MAC receiver the voltage at pin 5 must be stabilized between 1.8 and 2.9 V by zener diode D1 and resistor R1. Standard switch at pin 9 must be in position 'standard L' to activate the peak-related slow AGC mode.

SOUND-IF CIRCUIT FOR TV AM-SOUND STANDARD L AND L'

GENERAL DESCRIPTION

The TDA3843 performs the AM-sound demodulation for the L- and L'- standard.

Features

- 5 to 8 V power supply and an alternative 12 V power supply
- Low power consumption (200 mW) at 5 V supply voltage
- New AC-coupled wideband IF-amplifier (high dynamic ranges, less intermodulation)
- In-phase wideband AM demodulator without external reference circuit
- Reduced THD figures even for low AF frequencies (typical 1%)
- Stabilizer circuit for ripple rejection and constant output signals
- All pins are ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	12	13.2	V
Supply current	$I_{11, 14\text{-}13}$	–	40	48	mA
Minimum IF input (RMS value)	$V_{1\text{-}16}$	–	70	100	μV
IF control range	ΔG_V	60	63	–	dB
AF output signal (RMS value)	$V_{6\text{-}13}$	–	550	–	mV
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	S+W/W	50	56	–	dB

PACKAGE OUTLINE

16-lead DIL; plastic (opposite bent leads) (SOT38WBE)

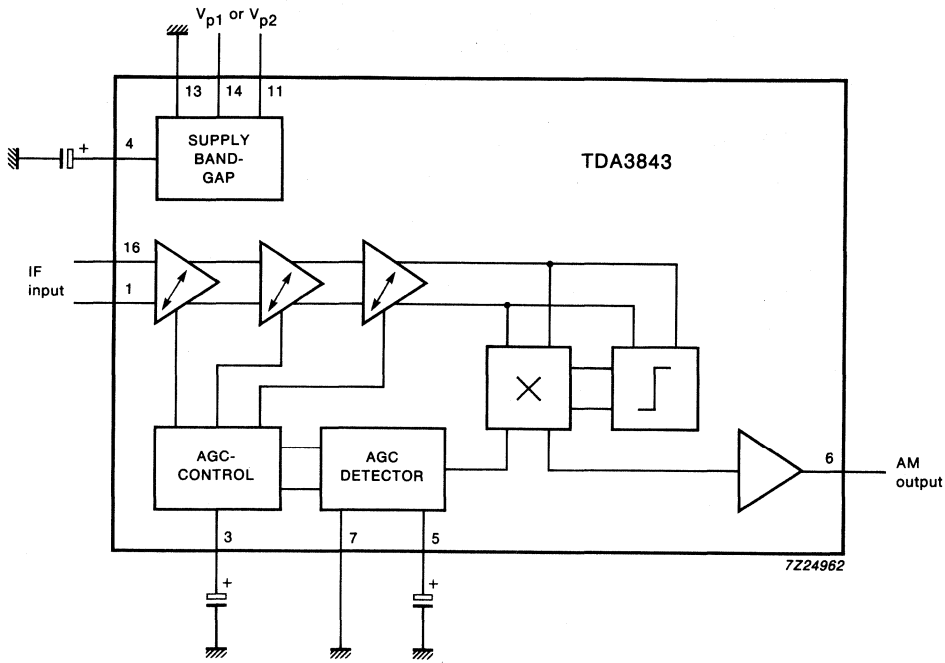


Fig.1 Block diagram.

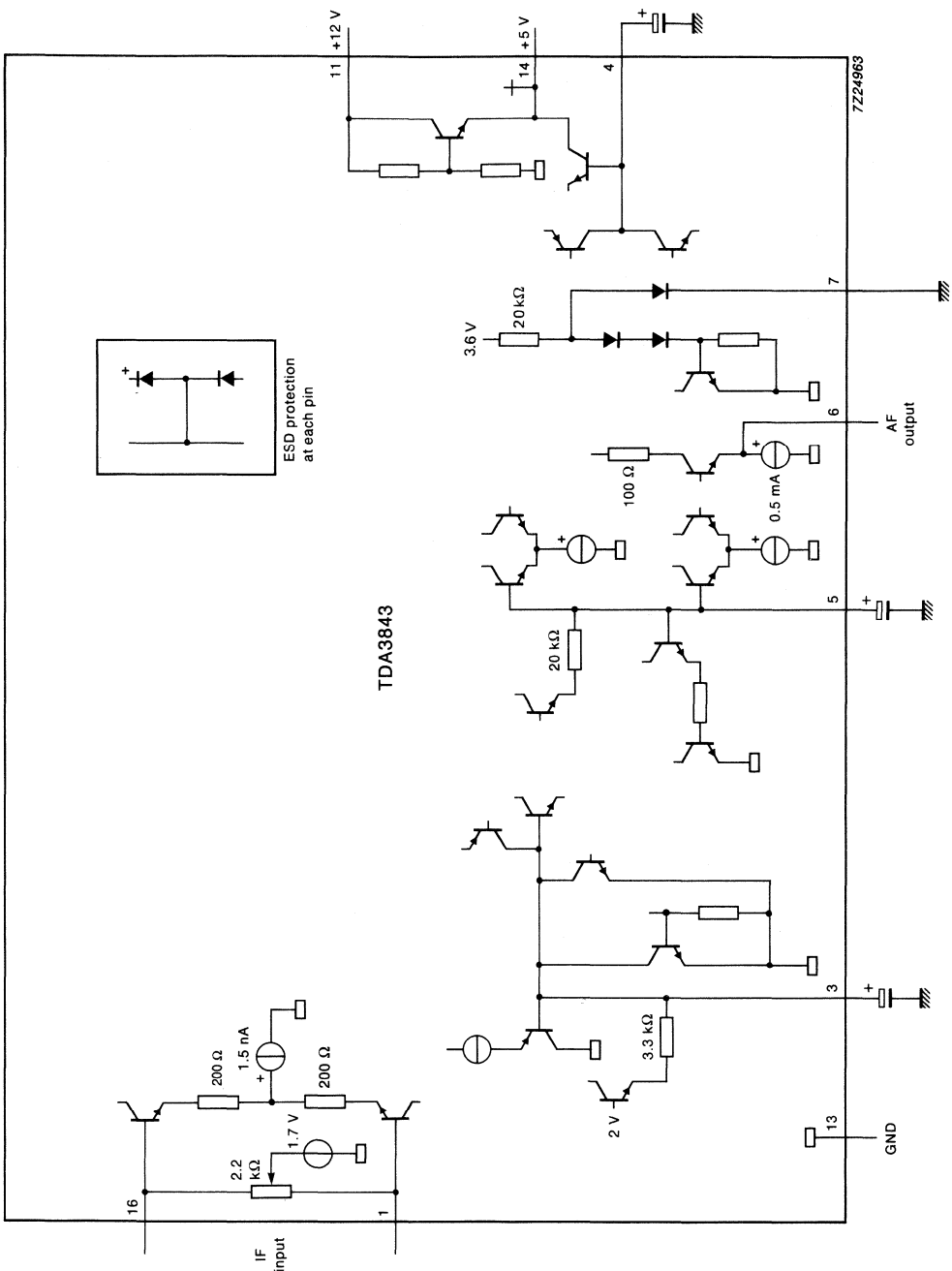


Fig.2 Input/output loading diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	13.2	V
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−25	+ 125	°C
Total power dissipation at V_{P2}	P_{tot}	−	635	mW

CHARACTERISTICS

V_{P1} = 5 V (see note 1); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current consumption		I_{11}	−	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	−	2	−	kΩ
Input capacitance		$C_{1\text{-}16}$	−	2.5	−	pF
Minimum IF input signal (RMS value)	note 2	$V_{1\text{-}16}$	−	70	100	μV
Maximum IF input signal (RMS value)	note 3	$V_{1\text{-}16}$	70	100	−	mV
Gain control range			60	63	−	dB
IF bandwidth	−3 dB		50	70	−	MHz
DC potential		$V_{1/16\text{-}3}$	−	1.7	−	V
AM demodulator	note 4					
AF output signal (RMS value)		$V_{6\text{-}13}$	440	550	660	mV
AF bandwidth	−3 dB, note 5	$V_{6\text{-}13}$	0.02	−	>100	kHz
Total harmonic distortion		THD	−	1	2	%
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	note 6	S+W/W	50	56	−	dB
DC potential		$V_{6\text{-}13}$	−	1.8	−	V
Output resistance	emitter follower with 0.5 mA bias current	R_6	−	200	−	Ω
Allowable AC output current (peak-to-peak value)	note 7	$\pm I_6$	−	−	0.3	mA
Allowable DC output current		$-I_6$	−	−	1	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection	$V_{ripple} < 200$ mV (peak-to-peak), 50 to 100 Hz, measured at 70 Hz					
AF signal output	$\alpha RR = V_{ripple}$ on V_P / V_{ripple} on V_O	αRR	30	40	–	dB
IF filter						
Proposal for sound carrier filter for L-standard	Fig.5					

Notes to the characteristics

1. Using the power supply voltage range V_{P1} = 5 to 8 V, the performance will not essentially change. Using the power supply voltage range, V_{P2} = 12 V, the performance will be comparable with the performance at V_{P1} = 5 to 8 V. The unused power supply pin must not be connected.
2. Start of gain control (low IF input signal) at –3 dB AF signal reduction at pin 6.
3. End of gain control (high IF input signal) at +1 dB AF signal expansion at pin 6.
4. Sound carrier = 32.4 MHz modulated with f = 1 kHz and a modulation depth m = 80%. IF input signal $V_{1\text{-}16}$ = 10 mV (RMS value).
5. A maximum value of 100 kHz is guaranteed, but, typically a maximum value of 700 kHz is found.
6. The capacitor at pin 4 may be omitted, but then the S+W/W figure will be degraded by up to 8 dB in the IF voltage range 1 mV up to 100 mV.
7. If a higher AC output current is required, an external resistor must be connected from the output to ground. This is to increase the bias current of the emitter follower (note, the maximum allowable DC output current).

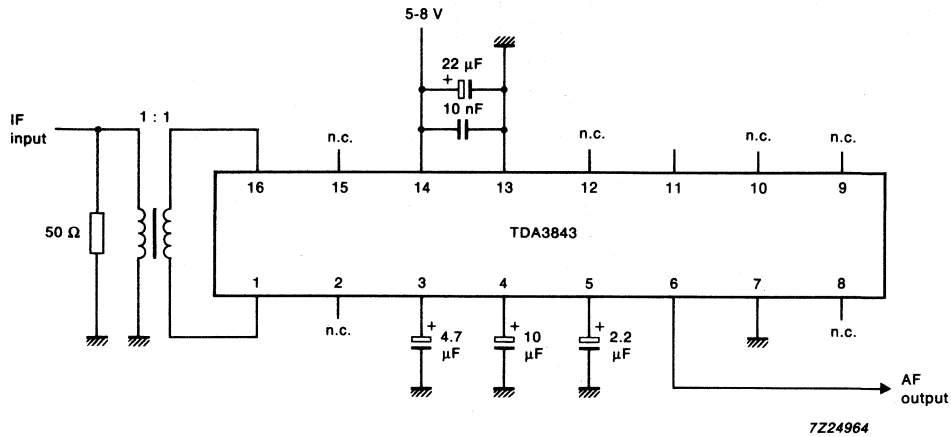


Fig.3 Test circuit, 5 V supply.

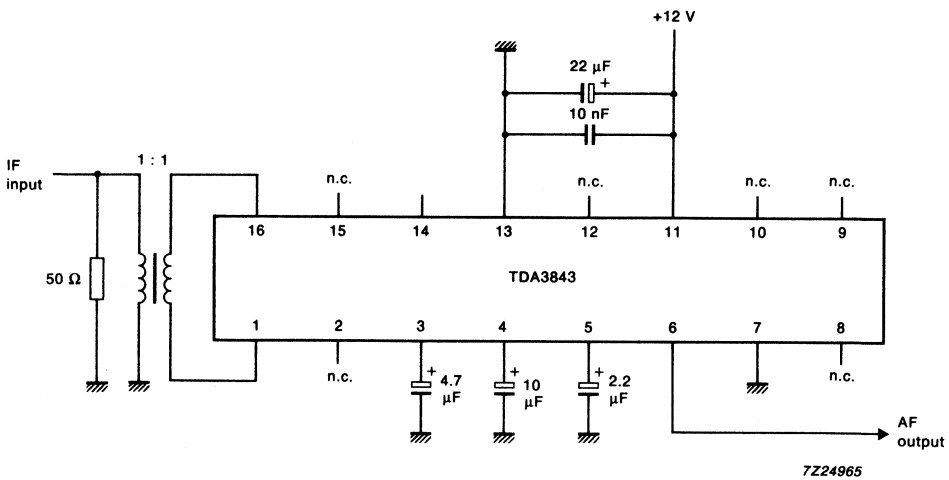
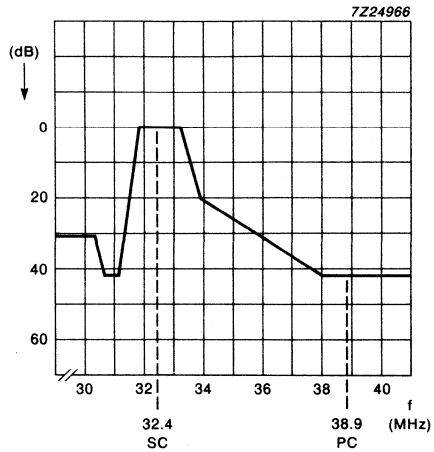


Fig.4 Test circuit, 12 V supply.



Where SC = sound carrier and PC = picture carrier.

Fig.5 AM IF filter for standard L.

QUASI-SPLIT-SOUND CIRCUIT AND AM DEMODULATOR

The TDA3845 is a quasi-split-sound IF circuit which is designed to give high performance television FM/AM sound.

Features

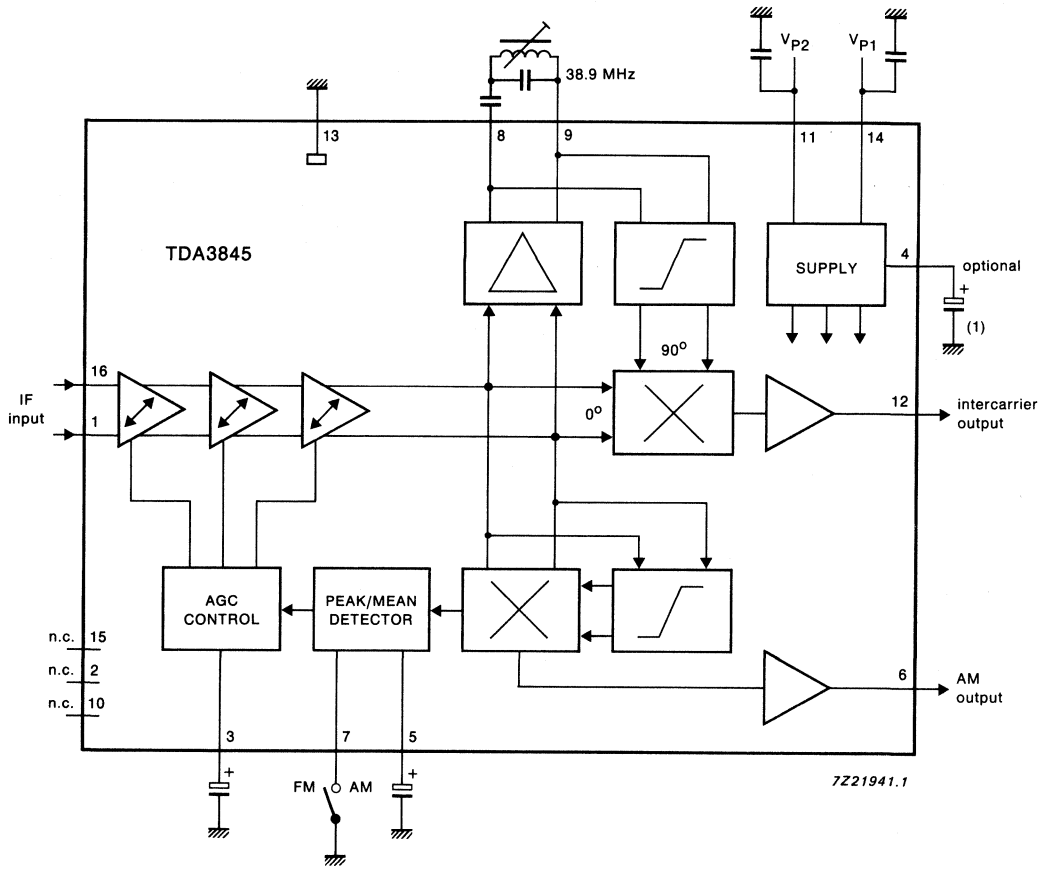
- Power supply from 5 V (200 mW) to 8 V source as well as an alternative 12 V source
- Gain controlled wideband IF amplifier (AC coupled with three stages)
- High precision internal 90° phase shifter for quadrature demodulator
- Amplitude detector for gain control which operates as a peak detector for FM sound and as a mean level detector for AM sound (switchable)
- Inphase wideband synchronous demodulator for AM detection
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection for all pins
- Suitable for all FM standards and L standard
- NICAM compatible

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 14		V_{P1}	4.5	5.0	8.8	V
or pin 11		V_{P2}	10.8	12.0	13.2	V
Supply current		I_P	–	40	–	mA
Minimum IF input voltage (RMS value)		$V_{1\text{-}16(rms)}$	–	70	100	μV
IF control range			60	63	–	dB
Intercarrier output voltage 5.5 MHz (RMS value)		$V_{12\text{-}13(rms)}$	70	100	–	mV
Signal-to-weighted-noise ratio (relative to 1 kHz; 50 kHz deviation)						
at 5.5 MHz for 2T/20T		(S + W)/W	–	60	–	dB
at 5.742 MHz for 2T/20T		(S + W)/W	–	58	–	dB
AF output voltage AM (RMS value)		$V_{6\text{-}13(rms)}$	440	550	660	mV
Signal-to-weighted-noise ratio; AM mode		(S + W)/W	–	56	–	dB
Total harmonic distortion (AM mode)		THD	–	1	2	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) See note 10 to the characteristics.

Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
pin 14		V_{P1}	4.5	8.8	V
or pin 11		V_{P2}	10.8	13.2	V
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C
Total power dissipation at V_{P2}		P_{tot}	−	635	mW

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1} = 5 V (see note 11); all measurements are with respect to ground (pin 13) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
pin 14		V_{P1}	4.5	5.0	8.8	V
or pin 11		V_{P2}	10.8	12.0	13.2	V
Total current consumption		I_{tot}	−	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	−	2	−	kΩ
Input capacitance		$C_{1\text{-}16}$	−	2.5	−	pF
Minimum IF input voltage (RMS value)	note 1	$V_{1\text{-}16(rms)}$	−	70	100	μV
Maximum IF input voltage (RMS value)	note 2	$V_{1\text{-}16(rms)}$	70	100	−	mV
Gain control range		ΔG	60	63	−	dB
Gain control voltage range		$G_{v3\text{-}16}$	1.5	−	3.0	V
IF bandwidth	−3 dB	B_{IF}	50	70	−	MHz
DC potential		$V_{1\text{-}16}$	−	1.7	−	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Intercarrier mode (FM mode; standard B/G)	notes 3, 4 and 5					
Reference amplifier						
Picture carrier amplitude (peak-to-peak value)		$V_{8\text{-}9(p\text{-}p)}$	–	270	–	mV
Operating resistance		$R_{8\text{-}9}$	–	4	–	kΩ
DC potential		$V_{8\text{-}9}$	–	3.9	–	V
Intercarrier mixer and output stage						
Output signal (RMS value) at 5.5 MHz		$V_{12(rms)}$	70	100	–	mV
at 5.74 MHz		$V_{12(rms)}$	32	45	–	mV
Intercarrier bandwidth at −1 dB		B_{12}	–	8	–	MHz
at −3 dB		B_{12}	–	9	–	MHz
Residual video AM on intercarrier signal	note 6		–	3	10	%
Output resistance		R_{12}	–	30	–	Ω
DC potential		V_{12}	–	1,8	–	V
Allowable AC output current (peak value)	note 7	$\pm I_{12(peak)}$	–	–	0.7	mA
Allowable DC output current		$-I_{12}$	–	–	2	mA
AF signal performance	note 8					
Black picture		(S + W)/W	60/58	68/64	–	dB
2T/20T pulses with white bars		(S + W)/W	57/55	60/58	–	dB
6 kHz sinewave (black-to-white modulation)		(S + W)/W	53/51	57/55	–	dB
250 kHz square wave (black-to-white modulation)		(S + W)/W	50/44	56/50	–	dB
AM mode (standard L)	notes 4 and 9					
S/N weighted in accordance with CCIR 468-2						
AF output signal (RMS value)		$V_{6(rms)}$	440	550	660	mV
AF bandwidth	−3 dB; note 12	B_{AF}	0.02	–	120	kHz
Total harmonic distortion		THD	–	1	3	%

parameter	conditions	symbol	min.	typ.	max.	unit
Signal-to-weighted-noise	note 10	(S + W)/W	50	56	–	dB
DC potential		V_6	–	1.8	–	V
Output resistance		R_6	–	200	–	Ω
Allowable AC output current (peak value)	note 7	$\pm I_{6(peak)}$	–	–	0.3	mA
Allowable DC output current		$-I_6$	–	–	1	mA
Standard switch	note 4					
Peak signal AGC (FM mode)	V_{P1}	V_7	1.8	–	V_{P1}	V
or switch open-circuit	V_{P2}	V_7	1.8	–	5.5	V
Mean signal AGC (AM mode)		V_7	–	–	0.8	V
Switch current						
at 0 V		$-I_7$	–	–	200	μA
at V_{P1}		I_7	–	–	10	μA
at V_{P2} (via a 2.2 kΩ series resistor)		I_7	–	–	2.5	mA
Ripple rejection						
Voltage ripple < 200 mV (peak-to-peak value) at 70 Hz						
AM/AF signal						
αRR = voltage ripple on V_P/voltage ripple on output signal		αRR	30	40	–	dB
FM phase noise						
Δf_{rms} intercarrier signal		$\Delta f_{(rms)}$	–	10	20	Hz

Notes to the characteristics

1. Start of gain control (LOW IF input signal) at –3 dB intercarrier signal reduction at pin 12, AGC mode set to FM or –3 dB AF signal reduction at pin 6, AGC mode set to AM.
2. End of gain control (HIGH IF input signal) at + 1 dB intercarrier signal expansion at pin 12, AGC mode set to FM or + 1 dB AF signal expansion at pin 6, AGC mode set to AM.
3. Picture carrier (38.9 MHz) to sound carriers (33.4 MHz/33.158 MHz) ratio: 13/20 dB.
   IF input signal (picture carrier at sync pulse); $V_{1\text{-}16}$ = 10 mV (RMS value), Transmitter mode: DSB.
   Reference for the (S + W)/W ratio (0 dB) corresponds to the sound modulation where f = 1 kHz and frequency deviation Δf = ± 50 kHz.
   With reduced frequency deviation Δf = ± 30 kHz and the (S + W)/W figures will decrease by 4.5 dB.
4. If the device is used only for the B/G standard (no AM), the capacitor at pin 5 can be omitted (pin 5 has to be disconnected). In this instance the AGC will always operate as a peak-signal AGC and is independent of the voltage at pin 7.

Notes to the characteristics (continued)

The AM mode can also be used for the B/G standard, consequently standard switching is not required. However, the intercarrier level depends on the video modulation and the AF performance may decrease.
When the IC is operated from a 12 V power supply pin 7 can be connected to a 12 V logic level via a 2.2 kΩ series resistor.

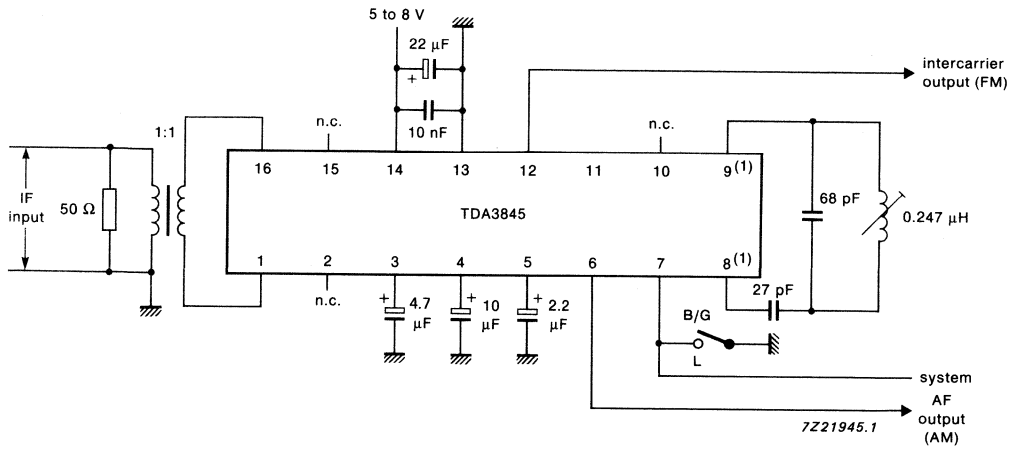
5. LC reference circuit for the picture carrier (pins 8 and 9); 68 pF//0.247 μH; in series with 27 pF: Q-loaded = 40 (Qo = 90); tuned to 38.9 MHz yields quadrature demodulation for the picture carrier which gives optimal video suppression at the intercarrier output (e.g. black-to-white jump of the video modulation).
The series capacitor provides a notch at the sound carrier frequency in order to produce more attenuation for the sound carrier in the PC reference channel. The ratio of parallel to series capacitance depends on the ratio of picture to sound carrier frequency which has to be adapted to other TV transmission standards, if required, in accordance with the formula:

$$C_S = C_P(F_{PC}/F_{SC})^2 - C_P$$

where:
C_S = series capacitor
C_P = parallel capacitor
F_{PC} = picture carrier frequency
F_{SC} = sound carrier frequency

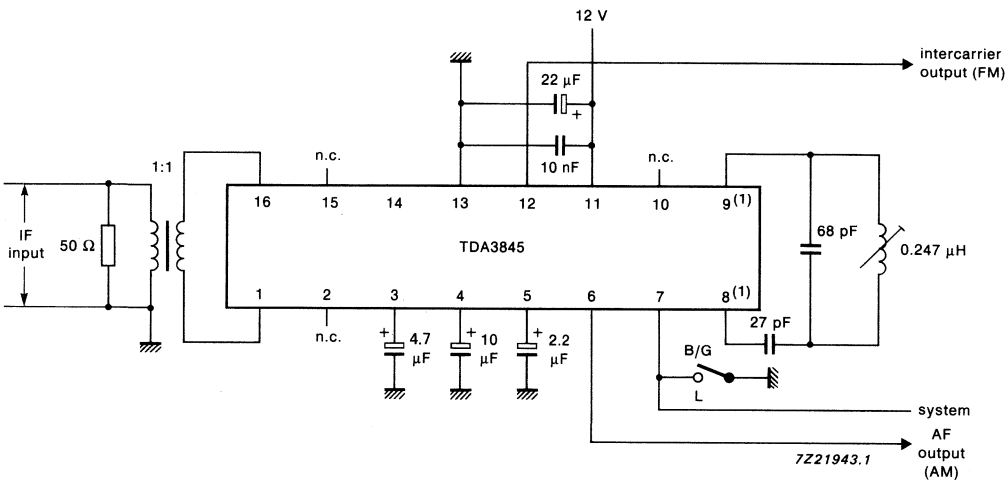
The result is an improved 'intercarrier buzz' in the stereo system B/G, particularly with 250 kHz video modulation (up to 10 dB improvement in sound channel 2), or to suppress 350 kHz video modulated beat in the digitally modulated NICAM subcarrier.
In order to optimize the AF signal performance, fine tuning to the optimal S/W at the sound channel 2 may be achieved by a 250 kHz video modulated squarewave.

6. Residual video AM is defined as:
   m = (A-B)/A
   A = intercarrier level at sync pulse
   B = intercarrier level at 100% white video modulation
7. If higher AC output current is required an external resistor must be connected between the output pin and ground in order to increase the bias current of the emitter follower. The allowable maximum DC output current must not be exceeded.
8. For all S/N measurements the used vision IF modulator must conform to the following:
   Incidental phase modulation for black-to-white jump should be less than 0.5 degrees.
   Intercarrier performance, measured with the television demodulator AMF2 (intercarrier mode weighted S/N ratio) better than 60 dB for 6 kHz sinewave black-to-white video modulation.
   Weighted S/N ratio of the demodulated intercarrier signals in accordance with CCIR 468-2, measured with deemphasis of 50 μs.
   The indicated (S + W)/W ratio X/Y concerns the sound channels 1 and 2 that means demodulated intercarrier signals of 5.5 and 5.74 MHz respectively.
9. Sound carrier frequency = 32.4 MHz modulated with f = 1 kHz and a modulation depth of 80%. IF input signal (sound carrier) $V_{1\text{-}16}$ = 10 mV (RMS value).
10. The capacitor at pin 4 can be omitted, however, the (S + W)/W figure for the AM sound (standard L) will be up to 8 dB worse in the IF voltage range 1 mV to 100 mV.
11. When the supply at V_{P2} = 12 V the performance will be comparable with the performance when V_{P1} = 5 to 8 V.
    The power supply pin that is not in use should be disconnected.
12. The maximum value is given as minimum 120 kHz and typical 700 kHz.



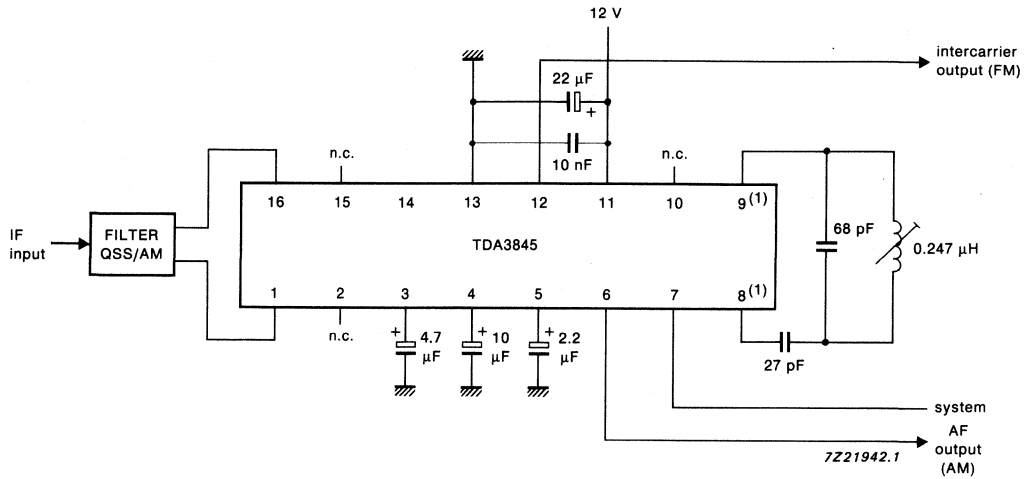
(1) See note 5 to the characteristics.

Fig.2 Test circuit for the +5 V supply.



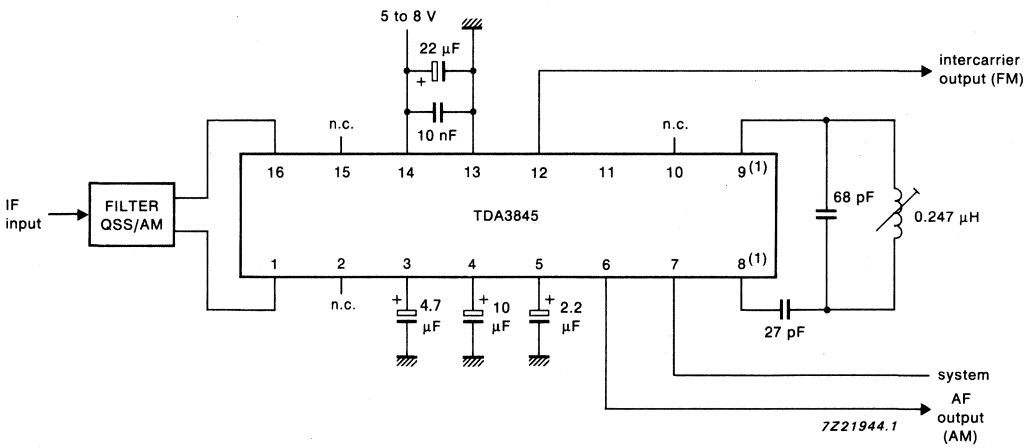
(1) See note 5 to the characteristics.

Fig.3 Test circuit for the +12 V supply.



(1) See note 5 to the characteristics.

Fig.4 Application diagram for the + 12 V supply.



(1) See note 5 to the characteristics.

Fig.5 Application diagram for the + 5 V supply.

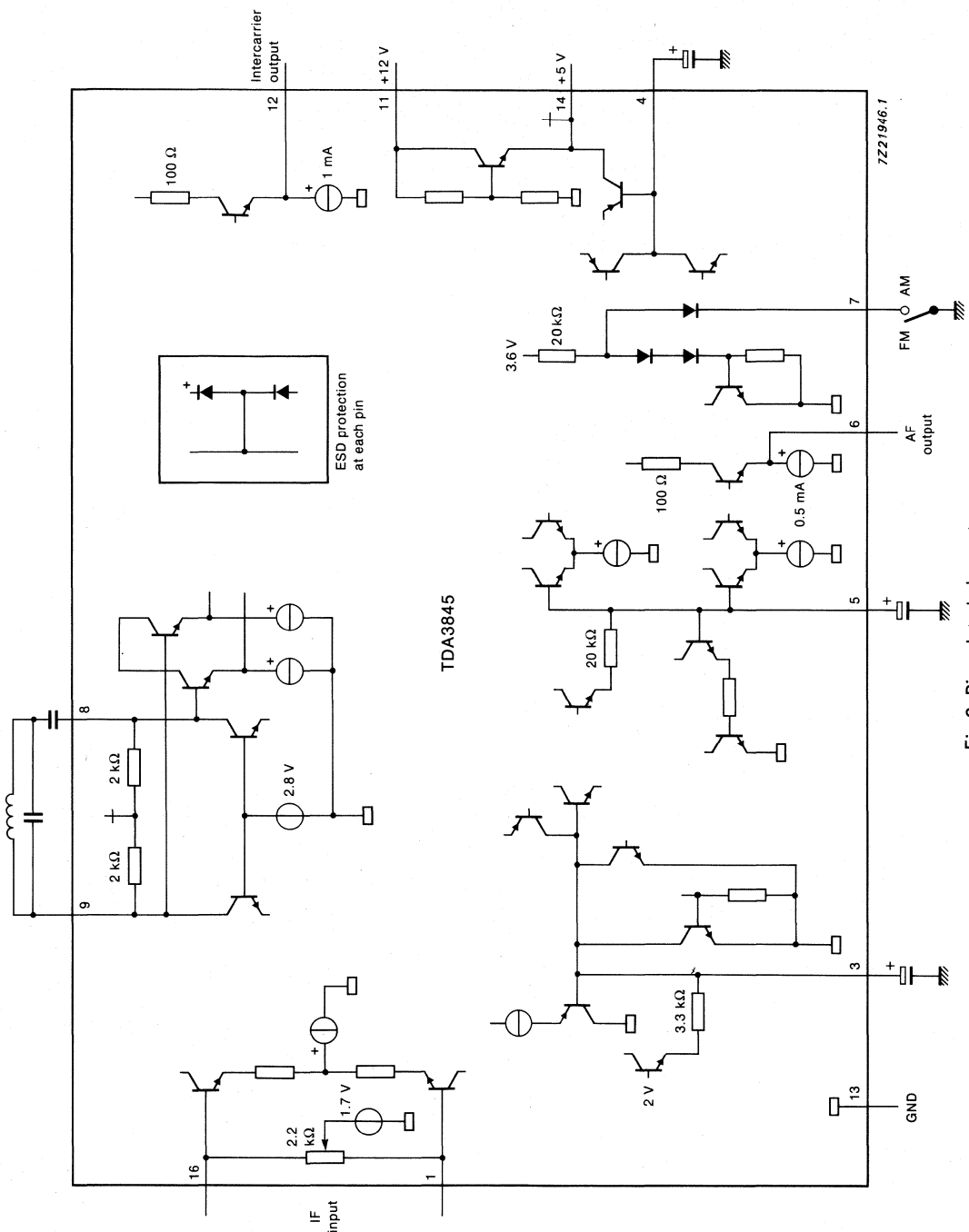
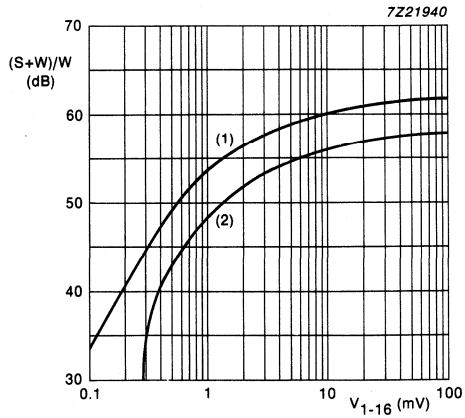


Fig.6 Pin related elements.



Picture modulation; 6 kHz sinewave.
Intercarrier signal; sound channel 1 = 5.5 MHz
sound channel 2 = 5.74 MHz.

Fig.7 Response curve of the signal-to-weighted-noise ratio of the demodulated intercarrier signal.

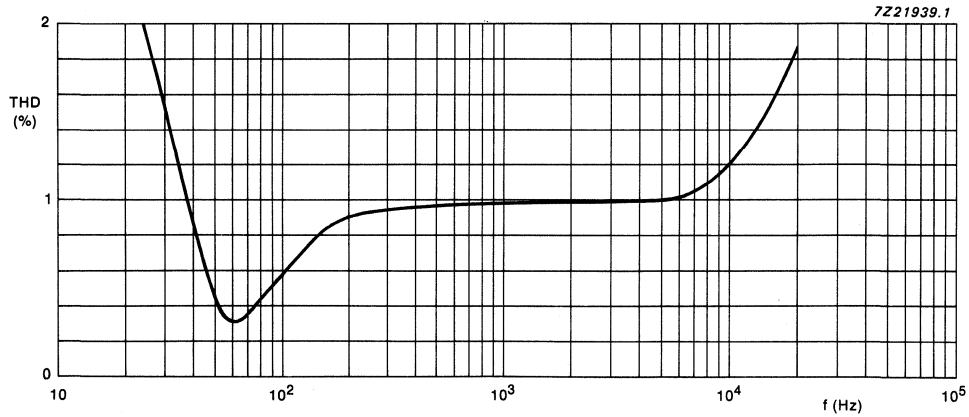


Fig.8 Response curve for the total harmonic distortion of the AM signal.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA3856

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ (rms)}$	audio output signal for FM (B/G)	-	1	-	V
$V_{o\ (rms)}$	audio output signal for AM (L)	-	0.6	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3856	24	shrink DIL	plastic	SOT234

Quasi-split sound processor for all standards

TDA3856

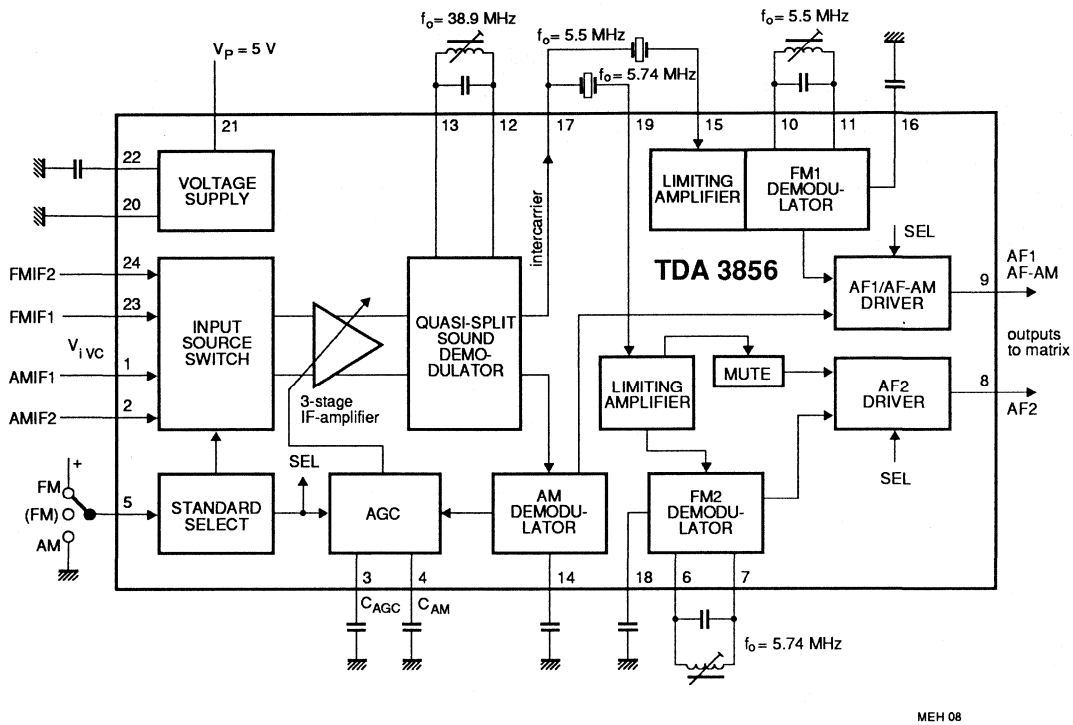


Fig.1 Block diagram (B/G and L).

Quasi-split sound processor for all standards

TDA3856

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5,74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC-decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 ... +8 V supply voltage (pin 28 not connected)
C_{ref}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

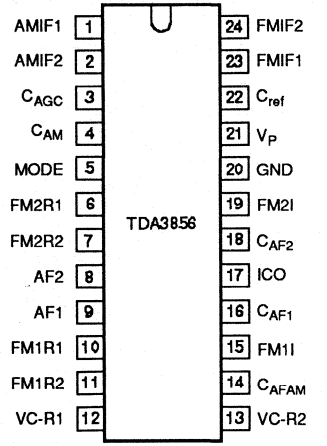


Fig.2 Pin configuration.

Quasi-split sound processor for all standards

TDA3856

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 19 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV on pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise on pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$$C_S = C_P (f_{VC}/f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.
The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltages (pin 21)	-	8.8	V
V_I	voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	650	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1, 2, 23 and 24	±500	-	V
	pins 1, 2, 23 and 24	+400	-	V
	pins 1, 2, 23 and 24	–500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_P	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected	1.3	-	2.3	V
		or alternative measure: 22 kΩ to GND				
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_{P1}$	-	-	100	μA
		V_5 = 0	-	-	–300	μA

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1, 2 or 23, 24)	internally set LOW	-	-	0.1	V
$\alpha_{12\text{-}13}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		-	1.75	-	V
$V_{i\ IF\ (rms)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction at pin 17	-	70	100	µV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction at pin 9	-	70	100	µV
ΔG_V	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)		1.7	-	2.6	V
Resonance amplifier (pins 12-13)						
$V_{o\ (p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{12\text{-}13}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{12,\ 13}$	DC voltage (pins 12 and 13)		-	V_P–1	-	V
Intercarrier mixer output (pin 17)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 17)		-	-	±0.7	mA
I_{17}	allowable DC output current		-	-	–2	mA
V_{17}	DC voltage		-	1.75	-	V

Quasi-split sound processor for all standards

TDA3856

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 15 and 19)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{15, 19}$	input resistance		-	560	-	Ω
$V_{15, 19}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 15 and 19 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 6-7 and 10-11)		-	100	-	mV
V	DC voltage (pins 6, 7, 10, and 11)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 8 and 9)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		-	-	1	dB
$R_{8, 9}$	output resistance		-	100	-	Ω
$V_{8, 9}$	DC voltage		-	2.1	-	V
$I_{8, 9\ (M)}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{8, 9}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	-	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		-	1.7	-	V

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.8; $V_{i\ AM\ (rms)}$ = 10 mV				
$V_{o\ (rms)}$	AF output signal at pin 9 (RMS value)		530	600	675	mV
R_9	output resistance (pin 9)		-	100	-	Ω
$I_{o\ (M)}$	maximum AC output current (peak value)	note 3	-	-	±1.5	mA
I_9	maximum DC output current		-	-	–2	mA
V_9	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{14}	DC voltage (pin 14)		-	2	-	V
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$), unless otherwise specified.						
V_o	signals attenuation of AF source selector					
	AF2 at pin 8	$V_5 = V_P$	70	-	-	dB
	for not required signal AF1 at pin 9	5.5 MHz at pin 15; V_5 = 0; V_i = 10 mV	70	-	-	dB
	or not required signal AF1 at pin 9	signal for L standard $V_5 = V_P$	70	-	-	dB
$dV_{8,9}$	DC level deviation (pins 8 and 9)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 8 and 9)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R=70 Hz $V_{R\ (p-p)}$ = 200 mV	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{12\text{-}13} = 470\ \Omega$ (instead of LC circuit); input signal $V_{i\ (rms)} = 20$ mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\ (rms)} = 20$ mV (pins 12-13). After switching ($V_5 = 0$ V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100% picture modulation.)
3. For larger current: $R_L > 2.2\ k\Omega$ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

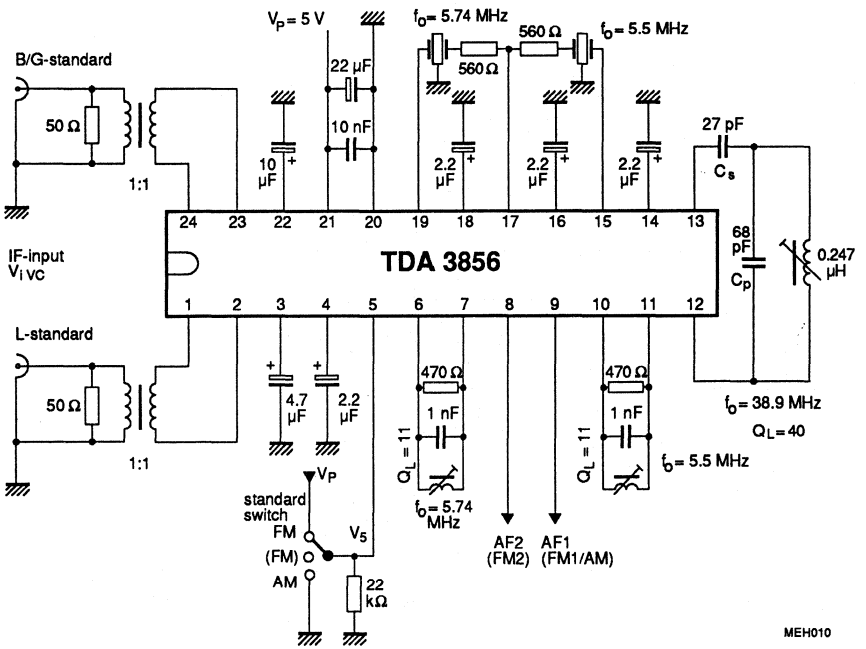


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

CHARACTERISTICS (continued)

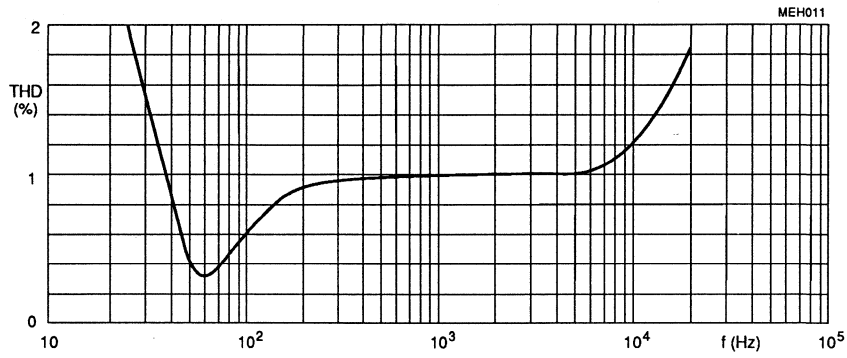
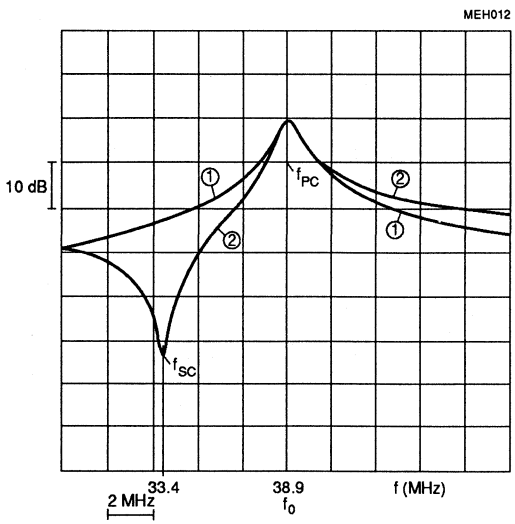


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

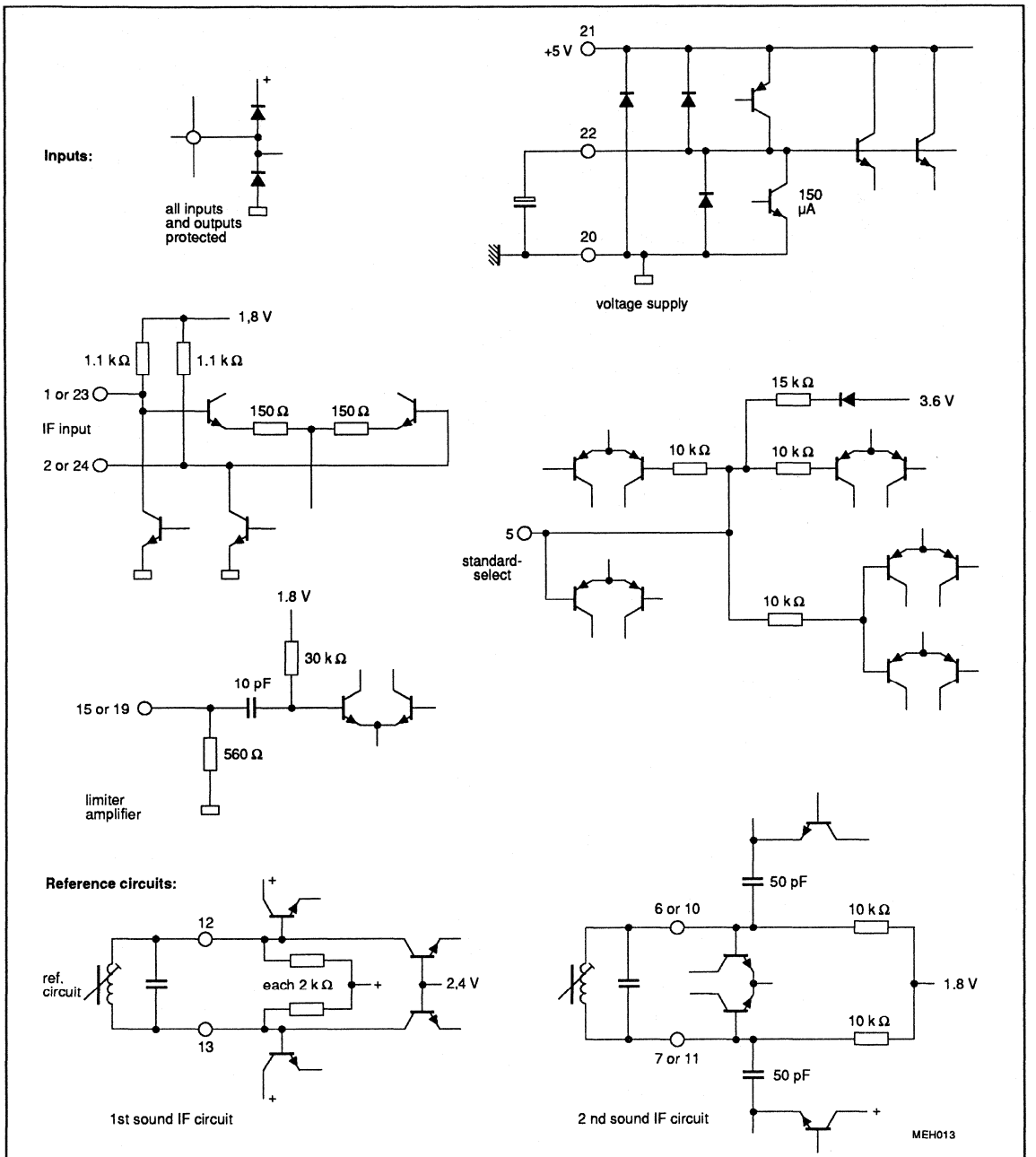


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

APPLICATION INFORMATION (continued)

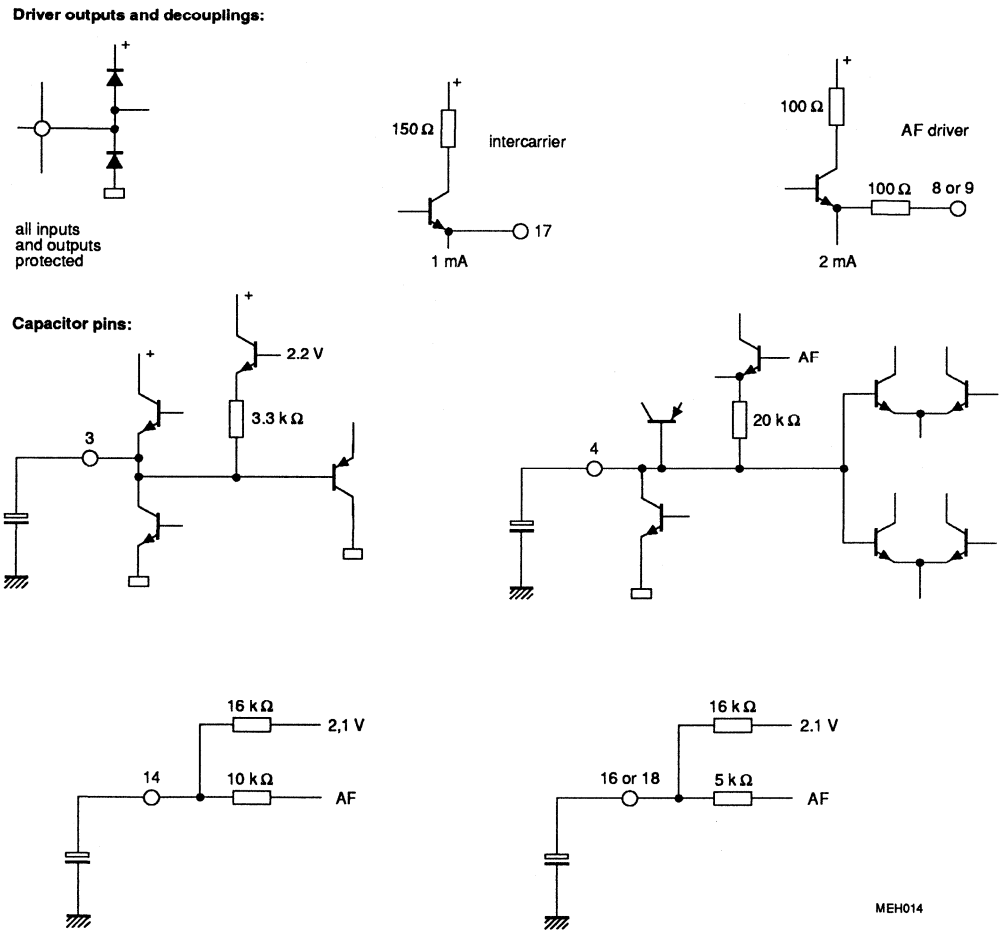


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA3857

Quasi-split sound processor with two FM demodulators

FEATURES

- Quasi-split sound processor for all FM standards e. g. B/G
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- Automatic muting of the AF2 signal (at B/G) by the input level
- Layout-compatible with TDA3856 (24 pins) and TDA3858 (32 pins)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 19)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ AF}$	audio output signal (RMS value)	-	1	-	V
THD	total harmonic distortion	-	0.5	-	%
S/N(W)	weighted signal-to-noise ratio	-	68	-	dB

GENERAL DESCRIPTION

Symmetrical IF inputs.

Gain controlled wideband IF amplifier.

AGC generation due to peak sync

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3857	20	DIL	plastic	SOT146

Quasi-split sound processor with two FM demodulators

TDA3857

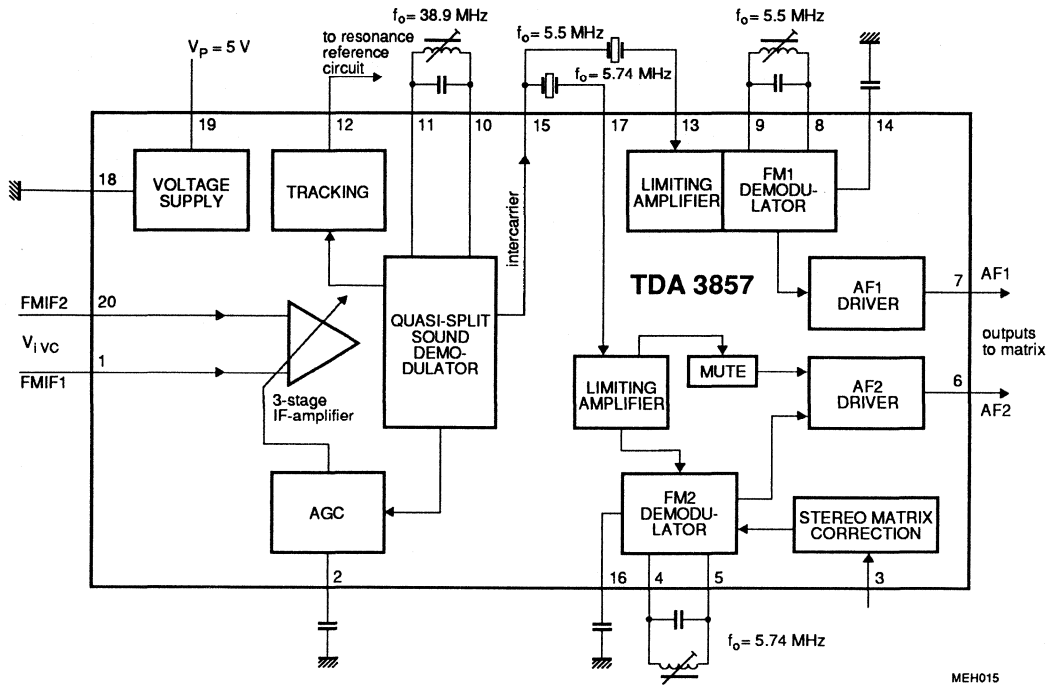


Fig.1 Block diagram (standard B/G).

Quasi-split sound processor with two FM demodulators

TDA3857

PINNING

SYMBOL	PIN	DESCRIPTION
FMIF1	1	IF difference input 1 for B/G standard (38.9 MHz)
C_{AGC}	2	charge capacitor for AM AGC
MATR	3	input for stereo matrix correction
FM2R1	4	reference circuit for FM2 (5.74 MHz)
FM2R2	5	reference circuit for FM2 (5,74 MHz)
AF2	6	AF2 output (AF out of 5.74 MHz)
AF1	7	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	8	reference circuit for FM1 (5.5 MHz)
FM1R2	9	reference circuit for FM1 (5.5 MHz)
VC-R1	10	reference circuit for the vision carrier (38.9 MHz)
VC-R2	11	reference circuit for the vision carrier (38.9 MHz)
TRACK	12	DC output level for tracking
FM1I	13	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	14	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	15	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	16	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	17	intercarrier input for FM2 (5.74 MHz)
GND	18	ground (0 V)
V_P	19	+5 ... +8 V supply voltage (pin 28 not connected)
FMIF2	20	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

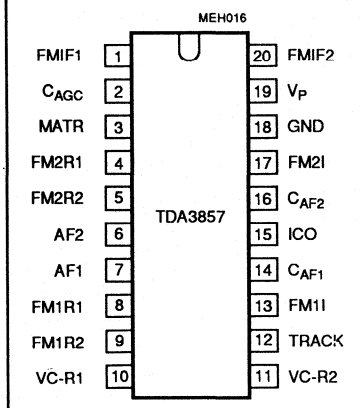


Fig.2 Pin configuration.

Quasi-split sound processor with two FM demodulators

TDA3857

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all FM standards (e. g. B/G).

B/G standard:
AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 17 , AF2 output is muted. The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 17, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 1 and 20 generate noise on pin 17, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 17 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_s in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

Quasi-split sound processor with two FM demodulators

TDA3857

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 19)	-	8.8	V
V_I	voltage (pins 1, 6, 7, 13, 15, 17 and 20)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1 and 20	±500	-	V
	pins 1 and 20	+400	-	V
	pins 1 and 20	–500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 19)		4.5	5	8.8	V
I_P	supply current (pin 19)		48	60	72	mA
IF amplifier (pins 1 and 20)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC input voltage		-	1.75	-	V
$V_{i\ IF\ (rms)}$	max input signal (RMS value, pins 1-20)	V_o = +1 dB	70	100	-	mV
	input signal sensivity (RMS value)	–3 dB intercarrier signal reduction at pin 15	-	70	100	μV
ΔG_v	IF gain control range		60	63	-	dB
V_2	voltage range for gain control (pin 2)		1.7	-	2.6	V
B	IF bandwith	–3 dB	50	70	-	MHz

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resonance amplifier (pins 10-11)						
$V_{o\ (p-p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
R	operating resistance		-	4	-	kΩ
L	inductance	Fig. 3 and 4	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonance circuit	Q_o = 90	-	40	-	
$V_{10, 11}$	DC voltage (pins 10 and 11)		-	V_P–1	-	V
Intercarrier mixer output (pin 15)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{15}	residual video AM on intercarrier	note 1	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{15}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 15)		-	-	±0.7	mA
I_{15}	allowable DC output current		-	-	–2	mA
V_{15}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 13 and 17)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	µV
	maximum input signal (RMS value)		200	-	-	mV
$R_{13, 17}$	input resistance		-	560	-	Ω
$V_{13, 17}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 17)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB

Quasi-split sound processor with two FM demodulators

TDA3857

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM-IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 13 and 17 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 µs. Q_L-factor = 11 for resonant circuits at pins 4-5 and 8-9.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 4-5 and 8-9)		-	100	-	mV
V	DC voltage (pins 4, 5, 8, and 9)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 6 and 7)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 6 and 7)	note 2	-	-	1	dB
$R_{6,7}$	output resistance		-	100	-	Ω
$V_{6,7}$	DC voltage		-	2.1	-	V
$I_{6,7(M)}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{6,7}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 6-7)		60	70	-	dB
V_3	adjusting voltage for AF2 signal (pin 3)	note 4	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_3		–1.5	-	1.0	dB
	typical gain range due to V_3		–2.5	-	1.5	dB
$V_{14,16}$	DC voltage (pins 14 and 16)		-	1.7	-	V
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
$V_{o\ 12}$	tracking output voltage range (pin 12)	note 5	V_P–3.3	-	V_P–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard, unless otherwise specified.						
V_o	signals attenuation of AF source selector	AF2 at pin 6	70	-	-	dB
$dV_{6,7}$	DC level deviation (pins 6 and 7)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 6 and 7)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R=70 Hz $V_{R\ (p-p)}$ = 200 mV	30	40	-	dB

Notes to the characteristics

1. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
2. AF signal can be adjusted by V_3
3. For larger current: R_L > 2.2 kΩ (pin 6 or 7 to GND) in order to increase the bias current of the output emitter follower.
4. If not used, pin 3 should not be connected.
5. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 10 and 11) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.

Quasi-split sound processor with two FM demodulators

TDA3857

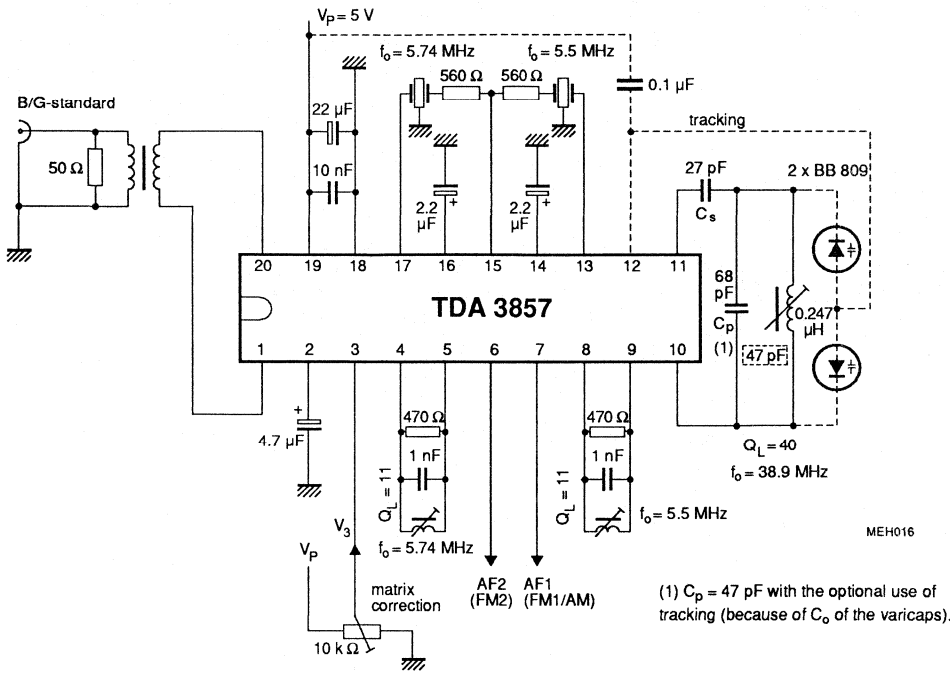
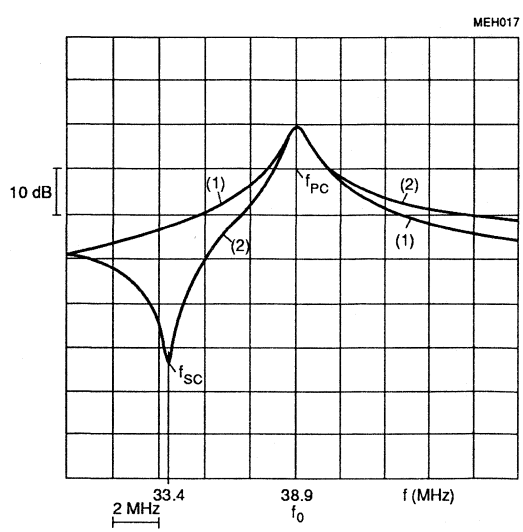


Fig.3 Test and application circuit for standard B/G (for application SAW-filter must be used).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.4 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

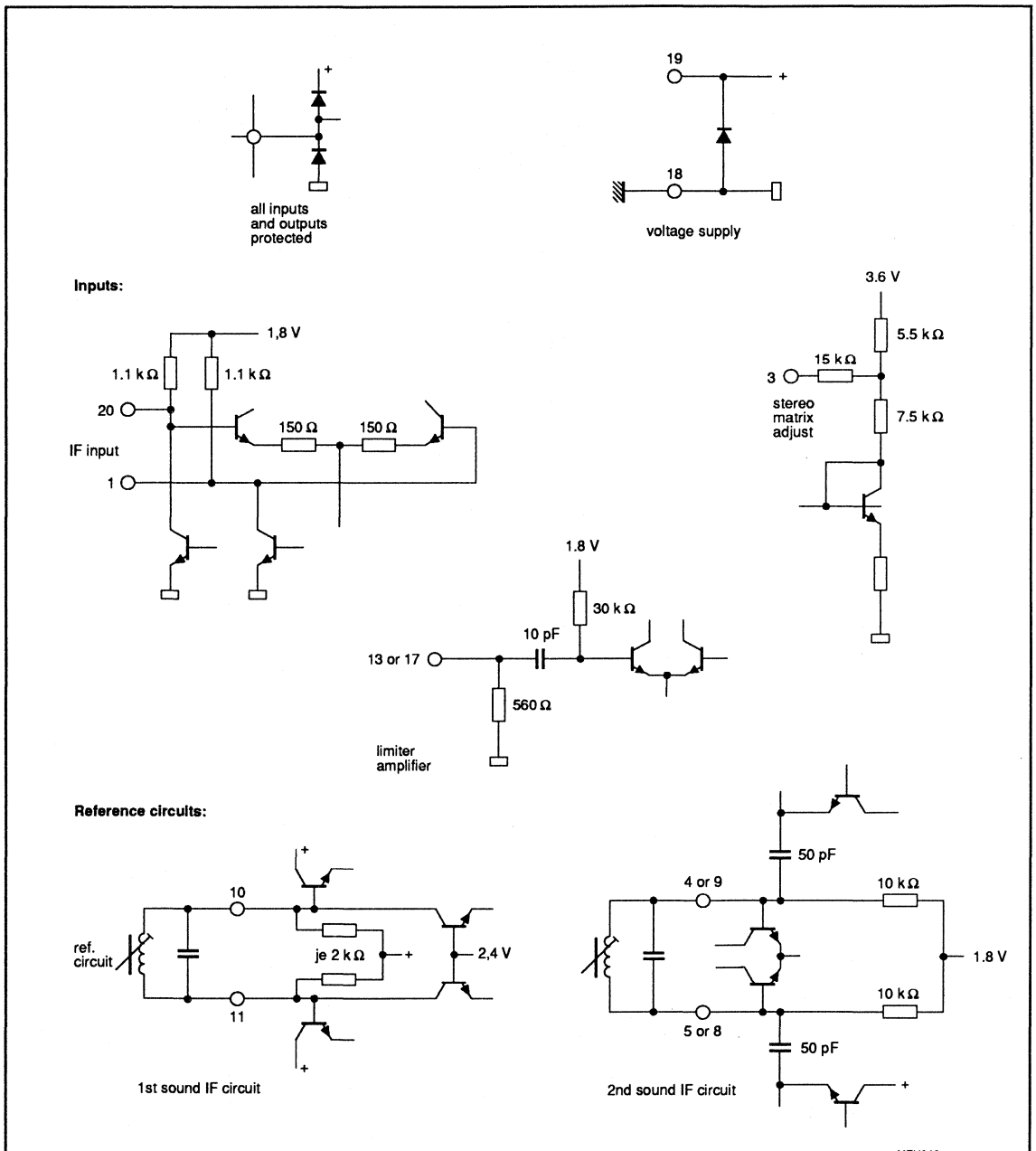


Fig.5(a) Internal circuits; (continued in Fig.5(b)).

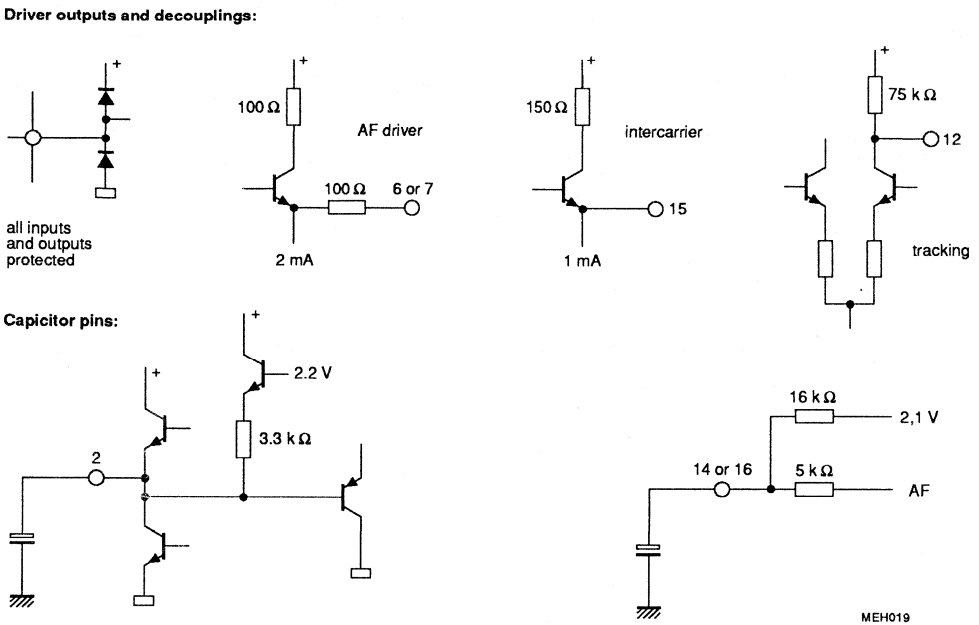


Fig.5(b) Internal circuits; (continued from Fig.5(a)).

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA3858

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3856 (24 pins) and TDA3857 (20 pins)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 27)	4.5	5	8.8	V
V_{P2}	alternative supply voltage (pin 28)	10.8	12	13.2	V
Data at V_{P1} = 5 V					
I_P	supply current (pin 27)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ (rms)}$	audio output signal for FM (B/G)	-	1	-	V
$V_{o\ (rms)}$	audio output signal for AM (L)	-	0.6	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3858	32	shrink DIL	plastic	SOT232

Quasi-split sound processor for all standards

TDA3858

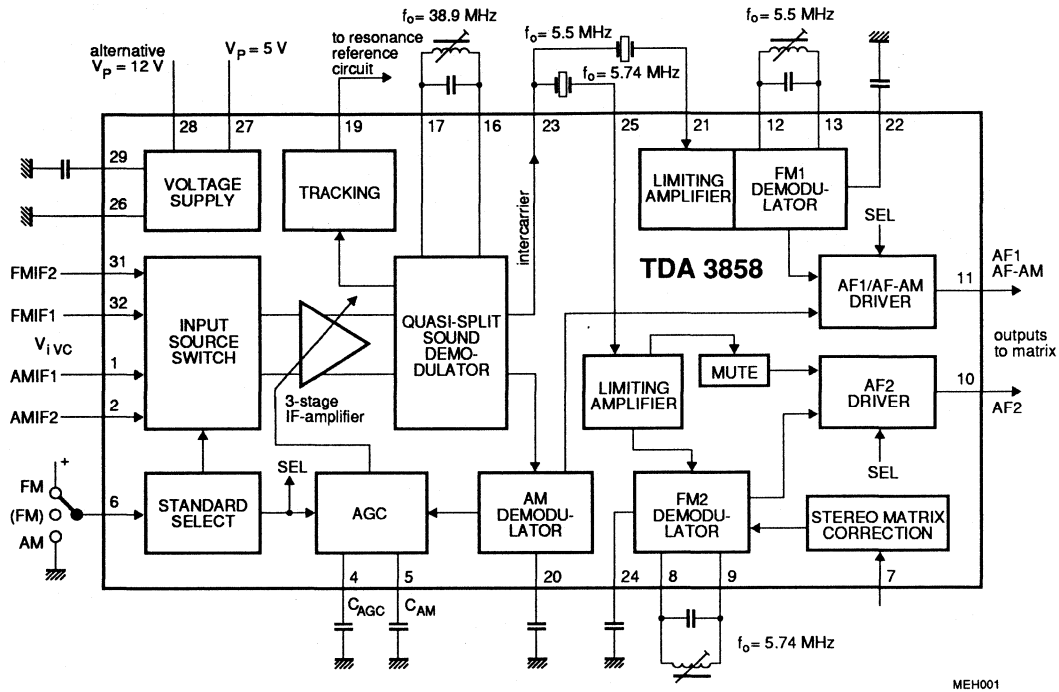


Fig.1 Block diagram (B/G and L standards).

Quasi-split sound processor for all standards

TDA3858

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
n.c.	3	not connected
C_{AGC}	4	charge capacitor for AGC (FM and AM)
C_{AM}	5	charge capacitor for AM AGC
MODE	6	3-state input for standard select
MATR	7	input for stereo matrix correction
FM2R1	8	reference circuit for FM2 (5.74 MHz)
FM2R2	9	reference circuit for FM2 (5,74 MHz)
AF2	10	AF2 output (AF out of 5.74 MHz)
AF1	11	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	12	reference circuit for FM1 (5.5 MHz)
FM1R2	13	reference circuit for FM1 (5.5 MHz)
n.c.	14	not connected
n.c.	15	not connected
VC-R1	16	reference circuit for the vision carrier (38.9 MHz)
VC-R2	17	reference circuit for the vision carrier (38.9 MHz)
n.c.	18	not connected
TRACK	19	DC output level for tracking
C_{AFAM}	20	DC-decoupling capacitor for AM demodulator (AF AM)
FM1I	21	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	22	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	23	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	24	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	25	intercarrier input for FM2 (5.74 MHz)
GND	26	ground (0 V)
V_{P1}	27	+5 to +8 V supply voltage (pin 28 not connected)
V_{P2}	28	+12 V supply voltage (pin 27 not connected)
C_{ref}	29	charge capacitor for reference voltage
n.c.	30	not connected
FMIF1	31	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	32	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

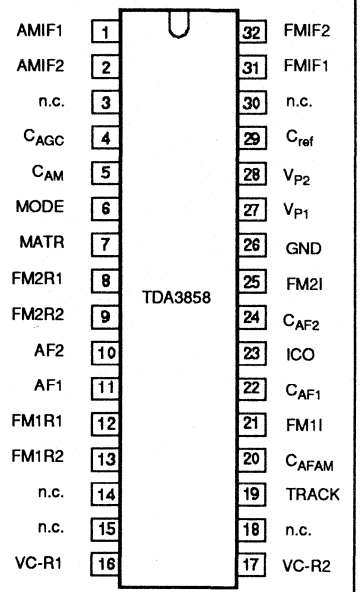


Fig.2 Pin configuration.

Quasi-split sound processor for all standards

TDA3858

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 6 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 31 and 32 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 25 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected). The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 25, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals on pins 31 and 32 generate noise on pin 25, which is present in the intercarrier signal and passes through the 5,74 MHz filter. Noise on pin 25 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level.The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to
$C_S = C_P (f_{VC} / f_{SC})^2 - C_P$.

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

Quasi-split sound processor for all standards

TDA3858

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltages (pin 27)	-	8.8	V
V_{P2}	supply voltages (pin 28)	-	13.2	V
V_I	voltage (pins 1, 2, 6, 10, 11, 21, 23, 25, 31 and 32)	0	V_P	V
$V_{I)}$	voltage at 12 V supply (pin 6)	0	5.5	V
P_{tot}	total power dissipation	0	950	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1, 2, 31 and 32	±500	-	V
	pins 1, 2, 31 and 32	+400	-	V
	pins 1, 2, 31 and 32	–500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_{P1} = 5 V (pin 27) and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage.range (pin 27)	pin 28 not connected	4.5	5	8.8	V
V_{P2}	supply voltage.range (pin 28)	pin 27 not connected	10.8	12	13.2	V
I_{P1}	supply current (pin 27)	V_{P1} = 5 V	48	60	72	mA
IF input not activated (pins 1-2 or 31-32)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1-2 or 31-32)	LOW internal set	-	-	0.1	V
$\alpha_{16\text{-}17}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF source control (pin 6)						
V_6	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 6 connected	2.8	-	V_{P1}	V
		pin 6 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 6 connected	1.3	-	2.3	V
		or alternative measure: 22 kΩ to GND				
	L (AM sound)	pin 6 connected	0	-	0.8	V
I_6	input current	$V_6 = V_{P1}$	-	-	100	μA
		$V_6 = 0$	-	-	−300	μA
$V_{6\ (12\ V)}$	maximum input voltage (pin 6)	supply at pin 28	-	-	5.5	V
IF amplifier (pins 31-32 or 1-2)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC potential, voltage (pins 1, 2, 31, 32)		-	1.75	-	V
$V_{i\ IF\ (rms)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 31-32)	−3 dB intercarrier signal reduction at pin 23	-	70	100	μV
	input signal sensivity L standard (RMS value, pins 1-2)	−3 dB intercarrier signal reduction at pin 11	-	70	100	μV
ΔG_V	IF gain control range		60	63	-	dB
B	IF bandwidth	−3 dB	50	70	-	MHz
V_4	voltage range for gain control (pin 4)		1.7	-	2.6	V
Resonance amplifier (pins 16-17)						
$V_{o\ (p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{16\text{-}17}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{16,\ 17}$	DC voltage (pins 16 and 17)		-	V_P−1	-	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 23)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{23}	residual video AM on intercarrier	note 2	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{23}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 23)		-	-	±0.7	mA
I_{23}	allowable DC output current		-	-	–2	mA
V_{23}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 21 and 25)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{21,\ 25}$	input resistance		-	560	-	Ω
$V_{2i,\ 25}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 25)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 19)	note 3	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

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CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 21 and 25 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 µs and $V_6 = V_{P1}$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 8-9 and 12-13.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 8-9 and 12-13)		-	100	-	mV
V	DC voltage (pins 8, 9, 12, and 13)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 10 and 11)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 10 and 11)	note 4	-	-	1	dB
$R_{10, 11}$	output resistance		-	100	-	Ω
$V_{10, 11}$	DC voltage		-	2.1	-	V
$I_{10, 11(M)}$	allowed AC current of emitter output (peak value)	note 5	-	-	±1.5	mA
$I_{10, 11}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 10-11)		60	70	-	dB
V_7	adjusting voltage for AF2 signal (pin 7)	note 6	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_7		–1.5	-	1.0	dB
ΔG_{AF2}	typical gain range due to V_7		–2.5	-	1.5	dB
$V_{22, 24}$	DC voltage (pins 22 and 24)		-	1.7	-	V
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.8; $V_{i\ AM\ (rms)}$ = 10 mV				
$V_{o\ (rms)}$	AF output signal at pin 11 (RMS value)		530	600	675	mV
R_{11}	output resistance (pin 11)		-	100	-	Ω
$I_{o\ (M)}$	maximum AC output current (peak value)	note 5	-	-	±1.5	mA
I_{11}	maximum DC output current		-	-	–2	mA
V_{11}	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{20}	DC voltage (pin 20)		-	2	-	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard ($V_6 = V_P$), unless otherwise specified.						
V_o	signals attenuation of AF source selector					
	AF2 at pin 10	$V_6 = V_P$	70	-	-	dB
	for not required signal AF1 at pin 11	5.5 MHz at pin 21; $V_6 = 0$; $V_i = 10$ mV	70	-	-	dB
	or not required signal AF1 at pin 11	signal for L standard $V_6 = V_P$	70	-	-	dB
$dV_{10, 11}$	DC level deviation (pins 10 and 11)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 10 and 11)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 µs				
	black picture	$f_i = 5.5$ MHz	59	63	-	dB
	2T/20T pulses with white bar	$f_i = 5.5$ MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	$f_i = 5.5$ MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	$f_i = 5.5$ MHz	50	56	-	dB
	black picture	$f_i = 5.742$ MHz	57	61	-	dB
	2T/20T pulses with white bar	$f_i = 5.742$ MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	$f_i = 5.742$ MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	$f_i = 5.742$ MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R=70 Hz $V_{R\ (p-p)} = 200$ mV	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{16-17} = 470\ \Omega$ (instead of LC circuit); input signal $V_{i\ (rms)} = 20$ mV (pins 31-32). AGC voltage V_4 set to a value to achive $V_{o\ (rms)} = 20$ mV (pins 16-17). After switching ($V_6 = 0$ V) measure attenuation.
   IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
3. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 16 and 17) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.
4. AF signal can be adjusted by V_7
5. For larger current: $R_L > 2.2\ k\Omega$ (pin 10 or 11 to GND) in order to increase the bias current of the output emitter follower.
6. If not used, pin 7 should not be connected.

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CHARACTERISTICS (continued)

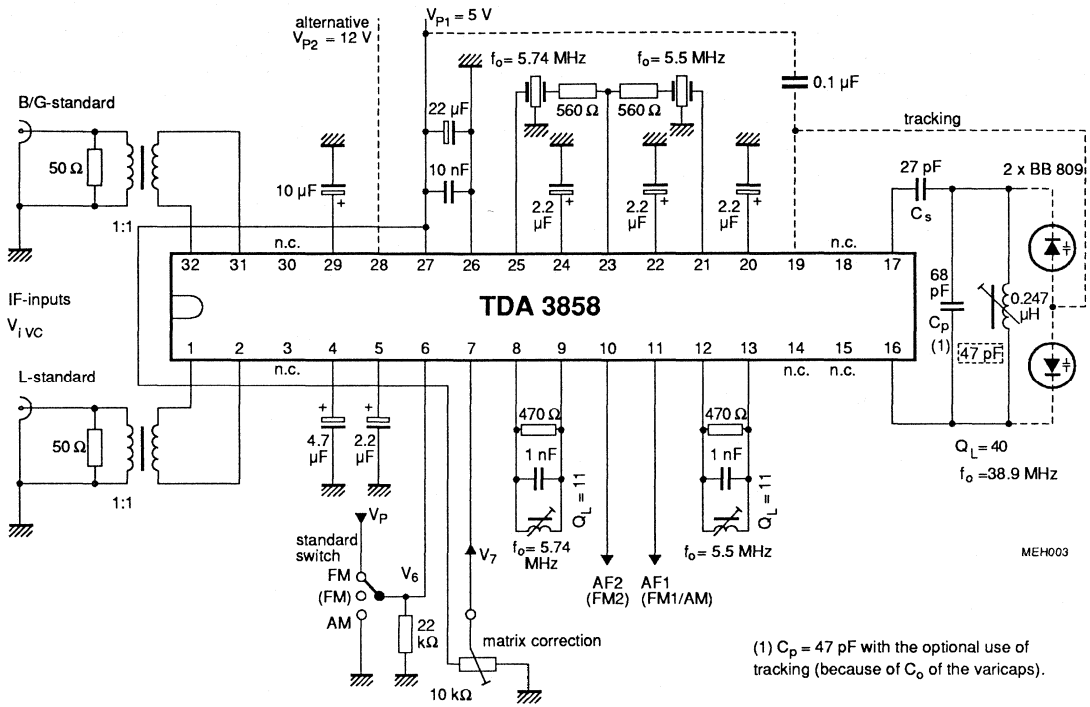


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used). For 12 V supply at pin 28, the capacitors shown at pin 27 must be connected to pin 28.

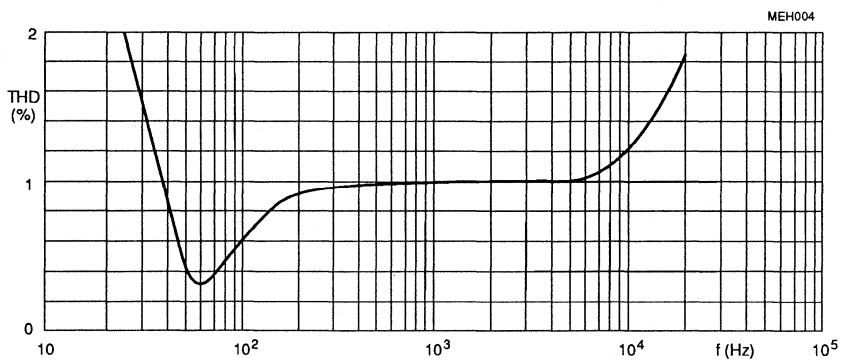
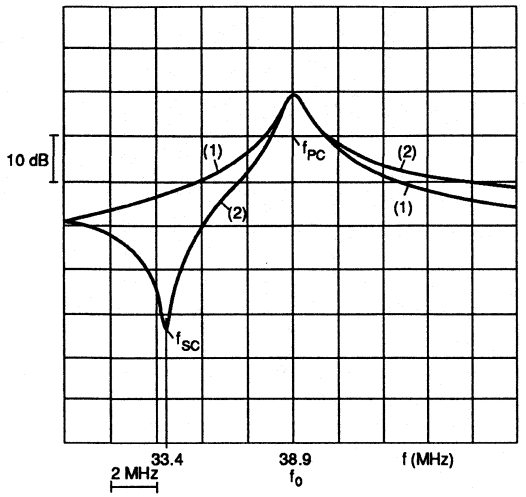


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard (V_6 = 0).

APPLICATION INFORMATION



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION (continued)

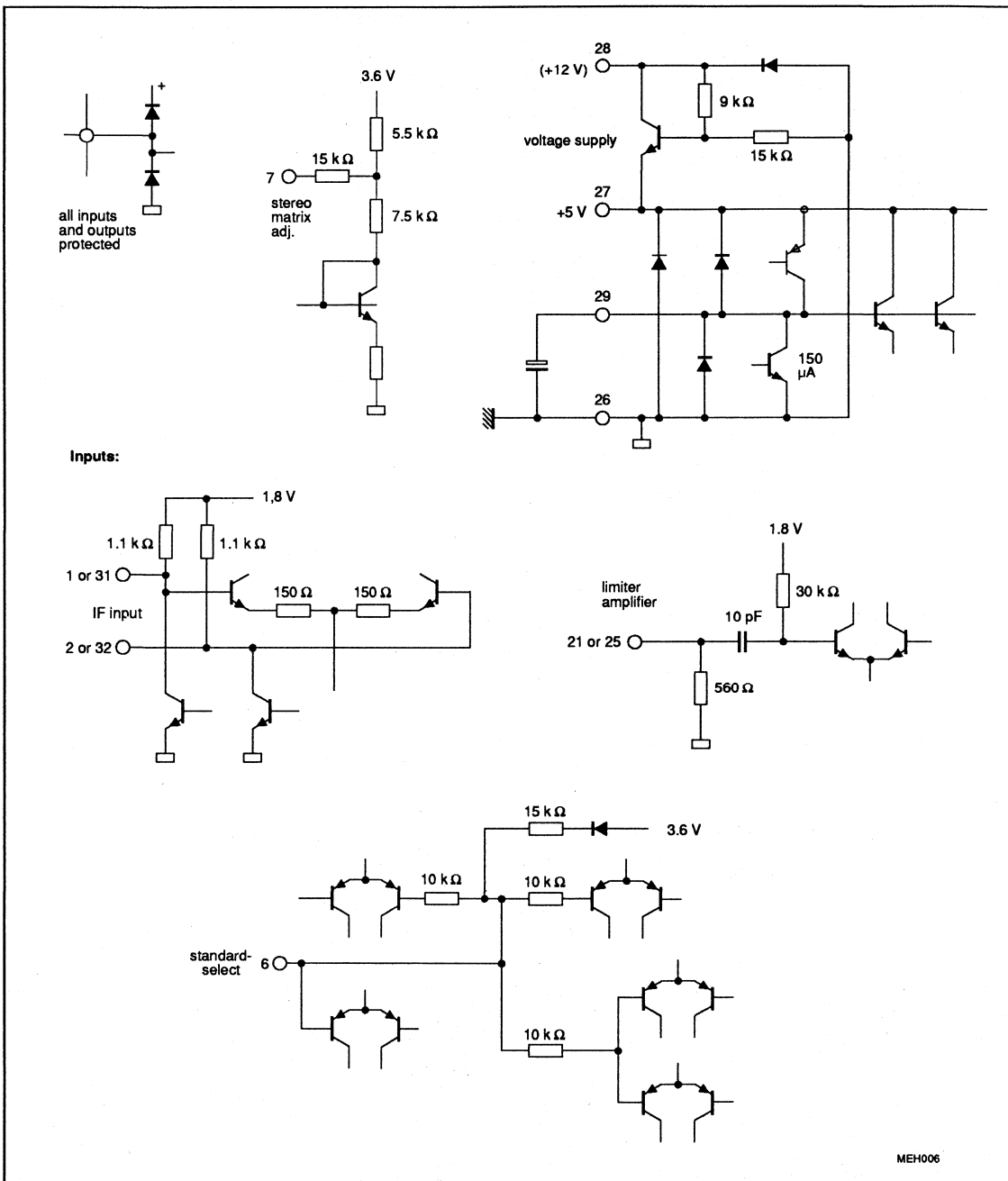


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

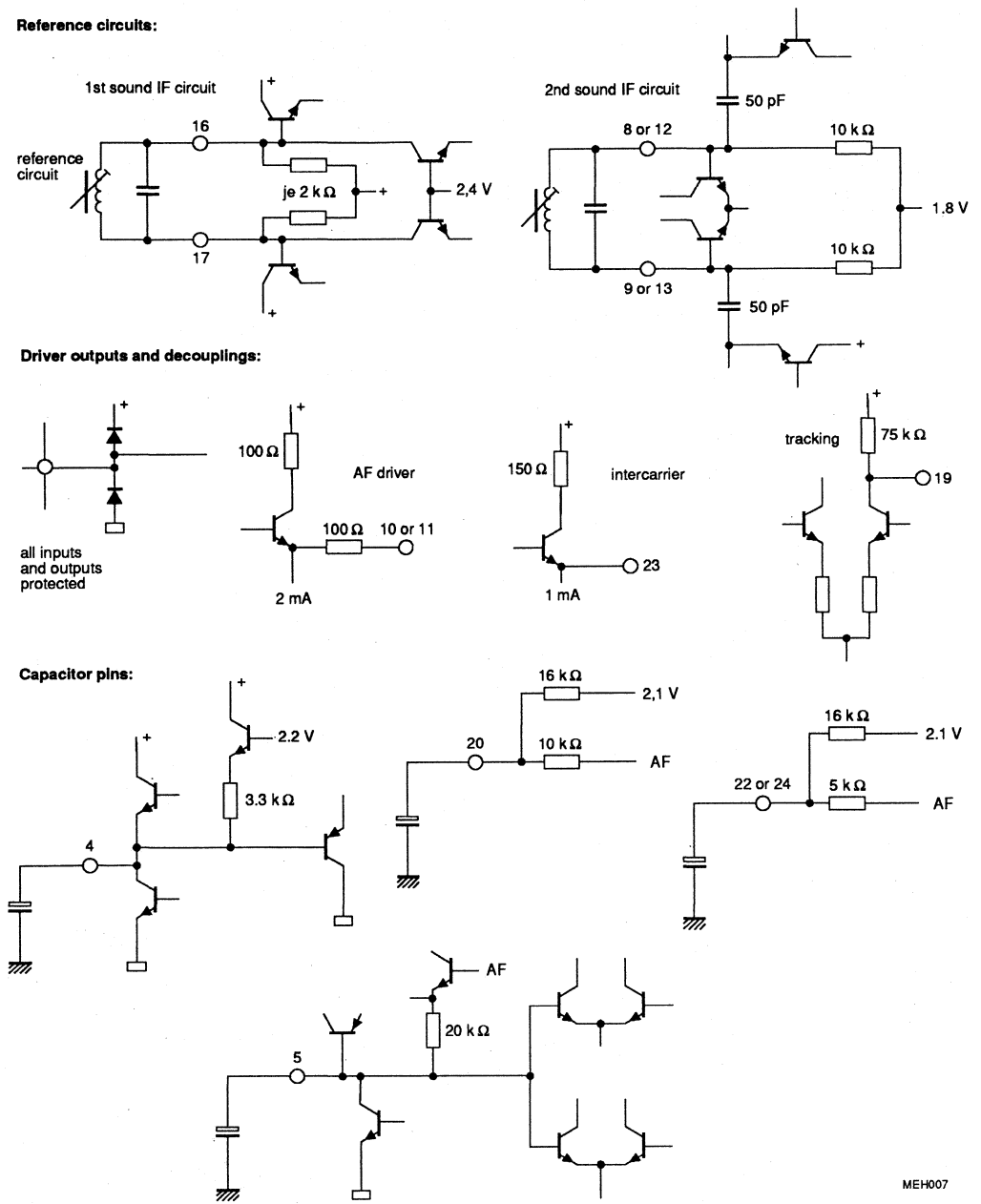


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Philips Components

Data sheet	
status	Preliminary specification
date of issue	February 1991

TDA3866

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins)
- AM output level typically 500 mV at m = 0.5 (+2.5 dB in comparison to TDA 3856)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ (rms)}$	audio output signal for FM (B/G)	-	1	-	V
$V_{o\ (rms)}$	audio output signal for AM (L)	-	0.5	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3866	24	shrink DIL	plastic	SOT234

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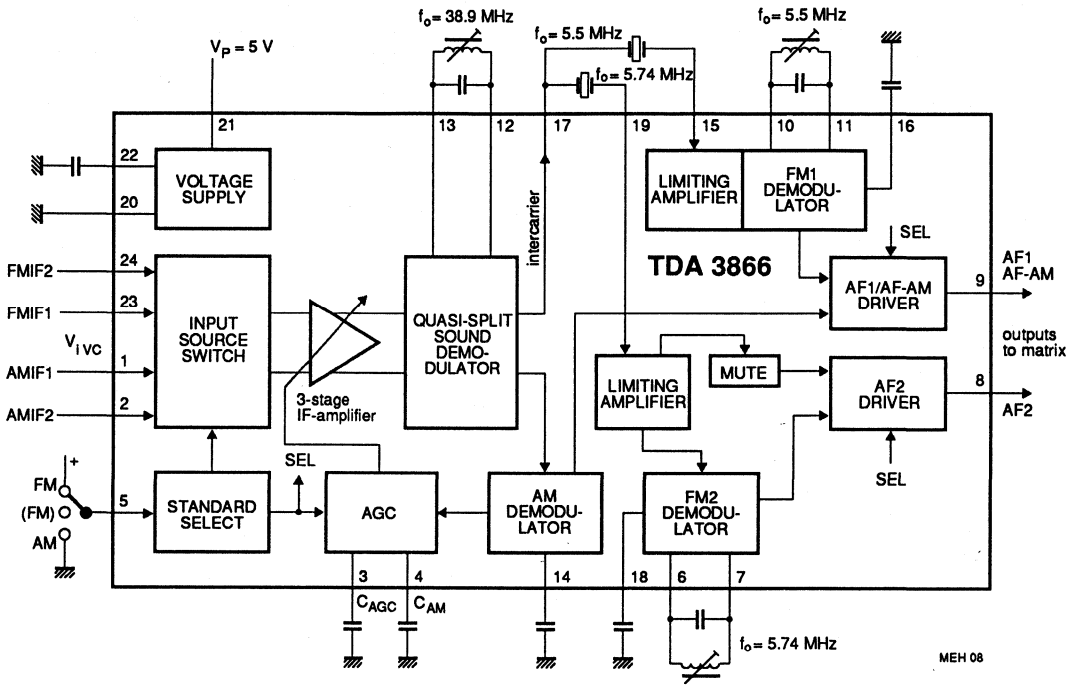

Fig.1 Block diagram (B/G and L).

Quasi-split sound processor for all standards

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PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5,74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC-decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 ... +8 V supply voltage (pin 28 not connected)
C_{ref}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

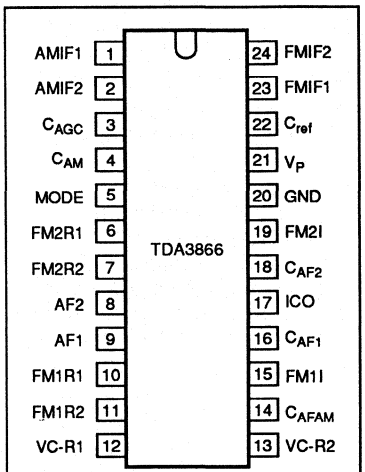

Fig.2 Pin configuration.

Quasi-split sound processor for all standards

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FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 19 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV on pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise on pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$$C_S = C_P (f_{VC}/f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.
The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ± 30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltages (pin 21)	-	8.8	V
V_I	voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	650	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1, 2, 23 and 24	±500	-	V
	pins 1, 2, 23 and 24	+400	-	V
	pins 1, 2, 23 and 24	–500	-	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_P	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected or alternative measure: 22 kΩ to GND	1.3	-	2.3	V
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_{P1}$	-	-	100	μA
		V_5 = 0	-	-	–300	μA

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1, 2 or 23, 24)	internally set LOW	-	-	0.1	V
$\alpha_{12\text{-}13}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction on pin 17	-	70	100	µV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction on pin 9	-	70	100	µV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)		1.7	-	2.6	V
Resonance amplifier (pins 12-13)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{12\text{-}13}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{12,\ 13}$	DC voltage (pins 12 and 13)		-	V_P–1	-	V
Intercarrier mixer output (pin 17)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 17)		-	-	±0.7	mA
I_{17}	allowable DC output current		-	-	–2	mA
V_{17}	DC voltage		-	1.75	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 15 and 19)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{15, 19}$	input resistance		-	560	-	Ω
$V_{15, 19}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 15 and 19 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11.						
V_{IC}	intercarrier signals (RMS values, pins 6-7 and 10-11)		-	100	-	mV
V	DC voltage (pins 6, 7, 10, and 11)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 8 and 9)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		-	-	1	dB
$R_{8, 9}$	output resistance		-	100	-	Ω
$V_{8, 9}$	DC voltage		-	2.1	-	V
$I_{8, 9}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{8, 9}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	-	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		-	1.7	-	V

Quasi-split sound processor for all standards

TDA3866

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.5; $V_{i\ AM\ (rms)}$ = 10 mV				
V_o	AF output signal on pin 9 (RMS value)		440	500	565	mV
R_9	output resistance (pin 9)		-	100	-	Ω
I_o	maximum AC output current (peak value)	note 3	-	-	±1.5	mA
I_9	maximum DC output current		-	-	–2	mA
V_9	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{14}	DC voltage (pin 14)		-	2	-	V
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$), unless otherwise specified.						
V_o	signals attenuation of AF source selector					
	AF2 on pin 8	$V_5 = V_P$	70	-	-	dB
	for not required signal AF1 on pin 9	5.5 MHz on pin 15; V_5 = 0; V_i = 10 mV	70	-	-	dB
	or not required signal AF1 on pin 9	signal for L standard $V_5 = V_P$	70	-	-	dB
$dV_{8,9}$	DC level deviation (pins 8 and 9)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 8 and 9)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 μs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz $V_{R\ (p\text{-}p)}$ = 200 mV	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{12\text{-}13}$ = 470 Ω (instead of LC circuit); input signal $V_{i\ (rms)}$ = 20 mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\ (rms)}$ = 20 mV (pins 12-13). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100% picture modulation.)
3. For larger current: R_L > 2.2 kΩ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

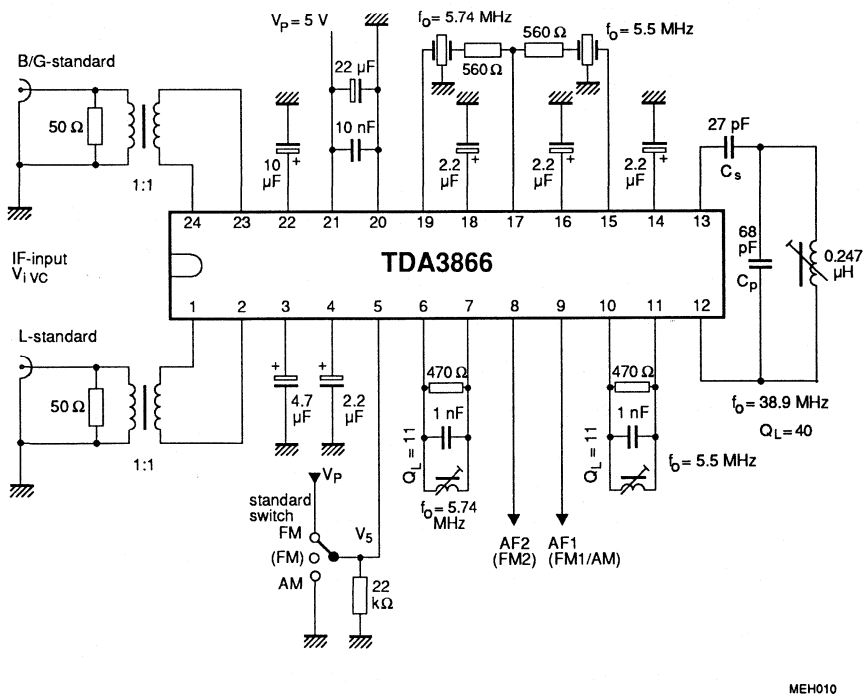


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

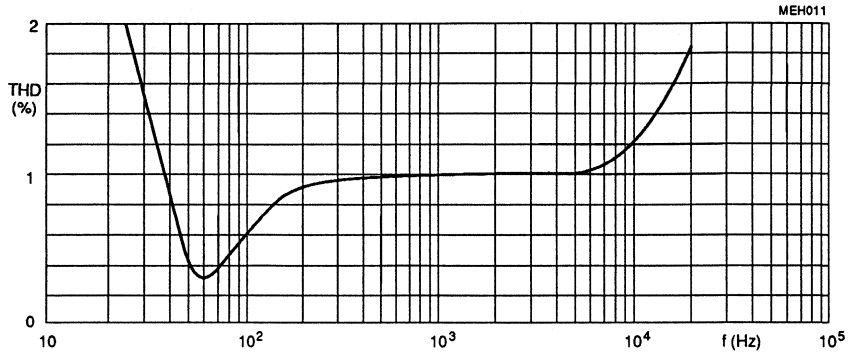
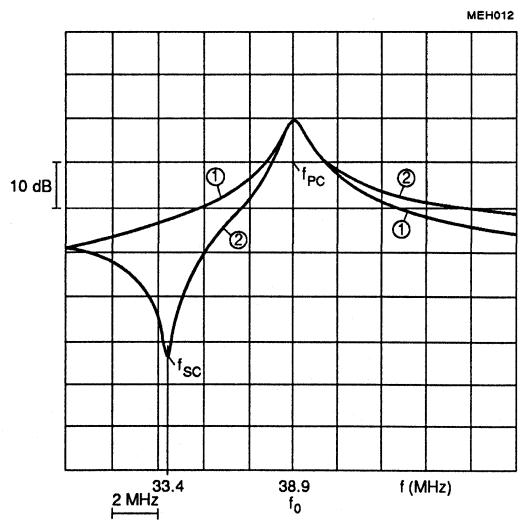


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonant circuit
(2) resonant circuit with $C_P = 68$ pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
$C_S = 27$ pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

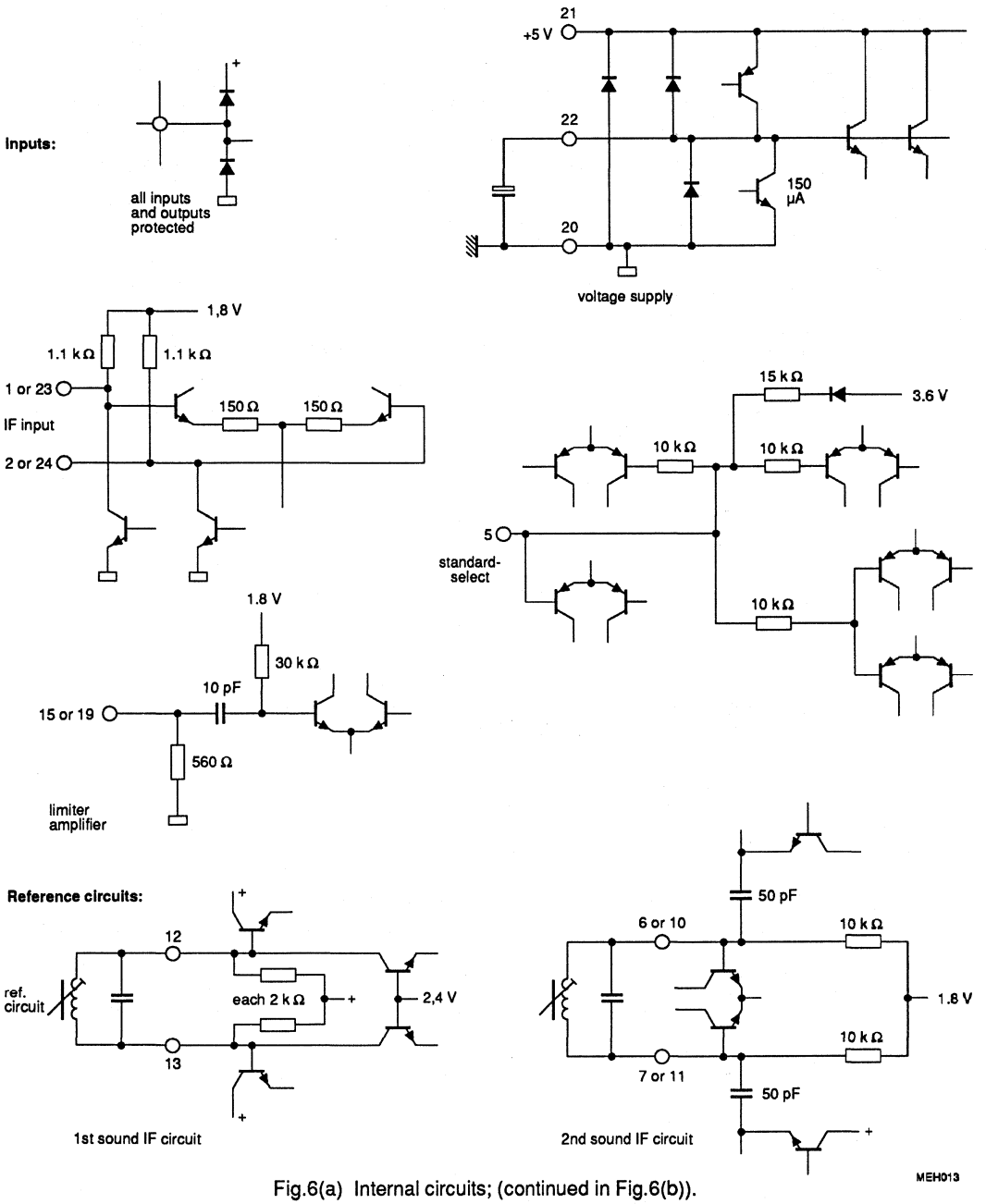


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

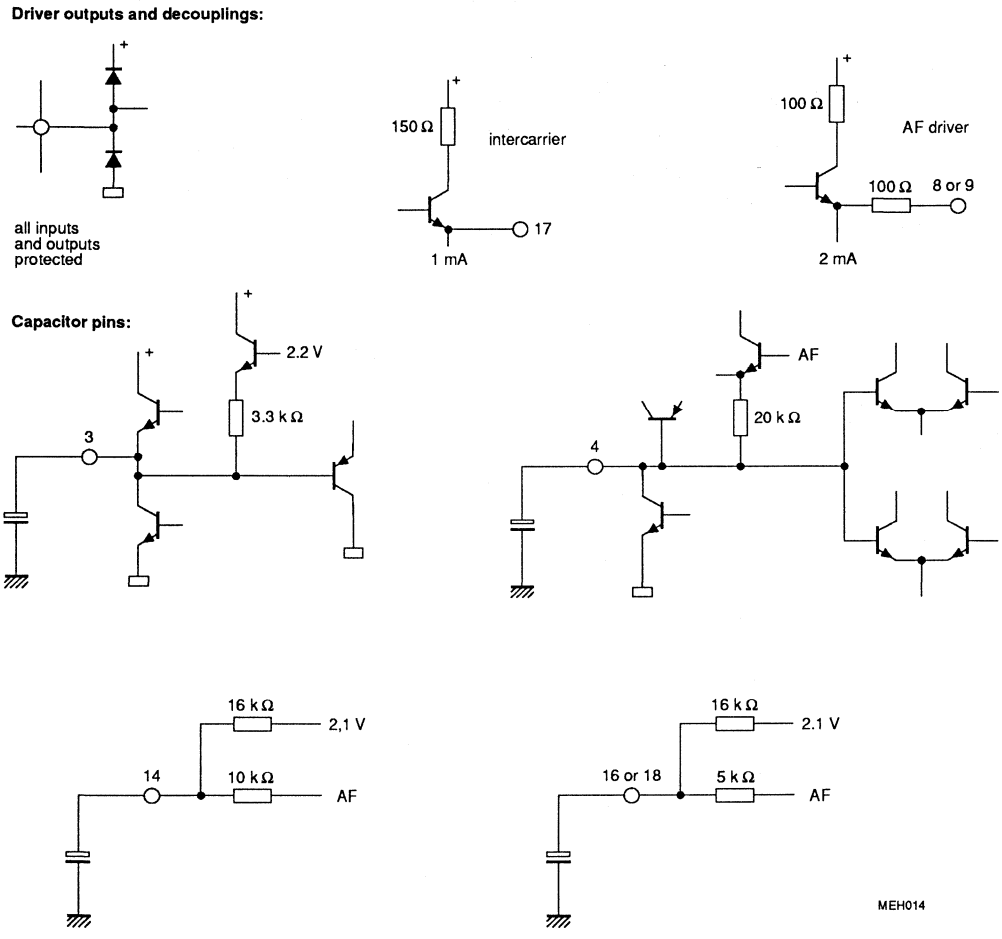


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		V_{13-16}	4.5	5.0	5.5	V
pin 1		V_{1-16}	11.0	11.25	11.5	V
Supply current	V_{13-16} = 5 V	I_{13}	–	14	–	mA
Operating current	V_{1-16} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

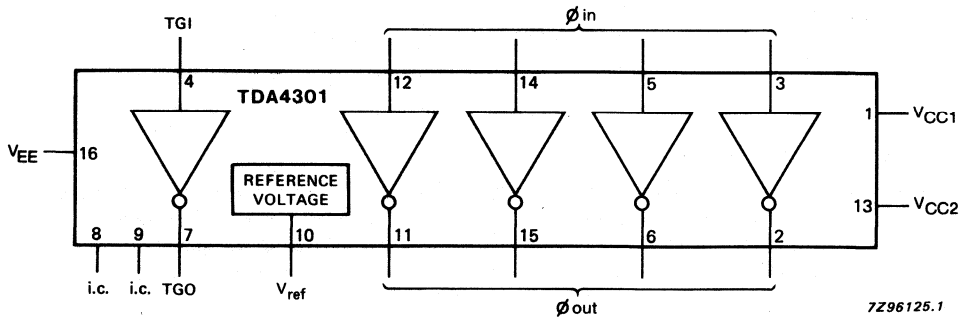


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1\text{-}16} = 11.25$ V; $V_{CC2} = V_{13\text{-}16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

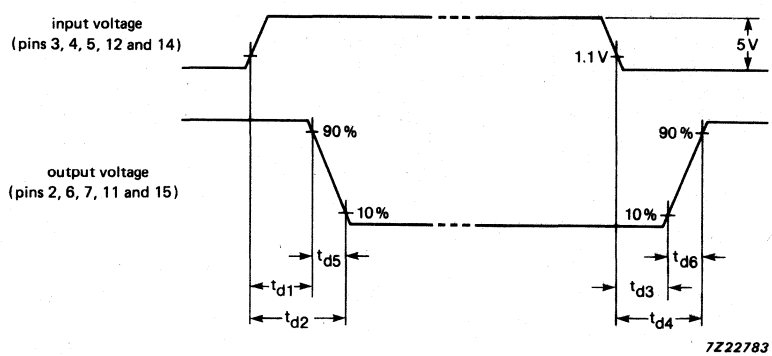


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

APPLICATION INFORMATION

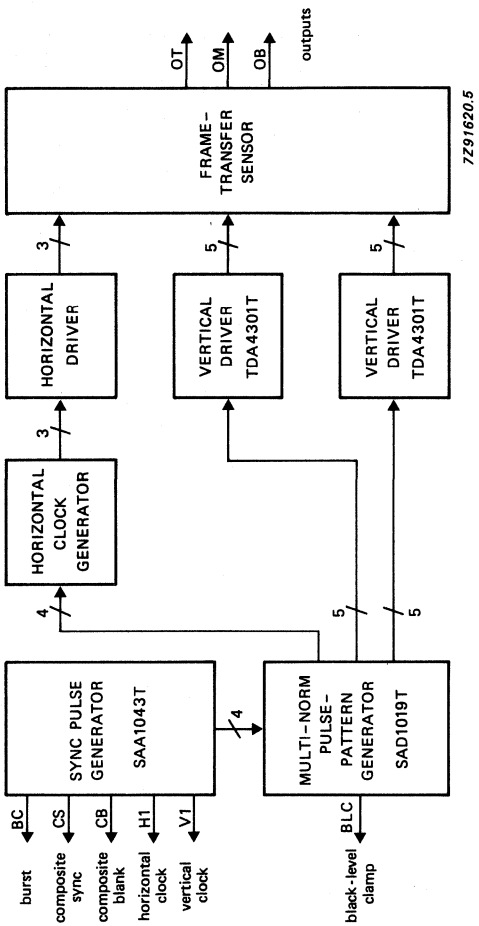


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301T is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 11		V_{11-14}	4.5	5.0	5.5	V
pin 1		V_{1-14}	11.0	11.25	11.5	V
Supply current	V_{11-14} = 5 V	I_{11}	–	14	–	mA
Operating current	V_{1-14} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

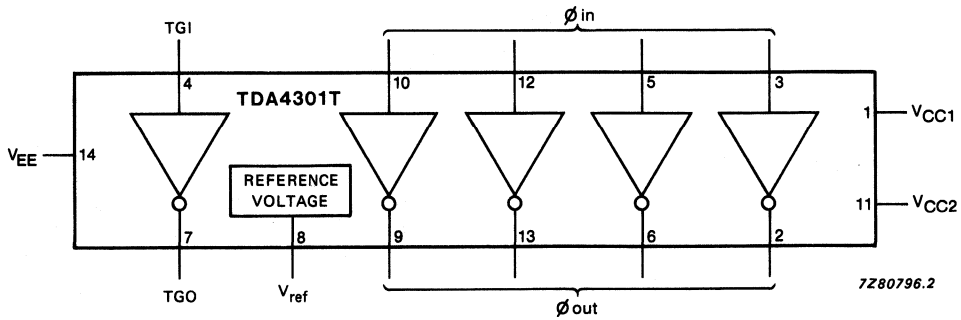


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 11		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 9 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 8)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 11)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1-14} = 11.25$ V; $V_{CC2} = V_{11-14} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 10 and 12)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 9 and 13)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

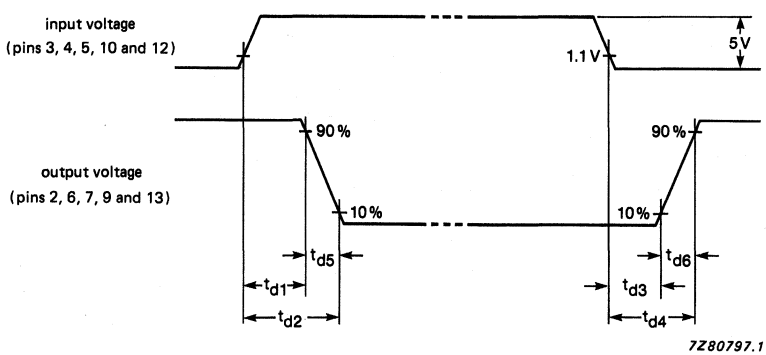


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load switching only one may be done at a time.

APPLICATION INFORMATION

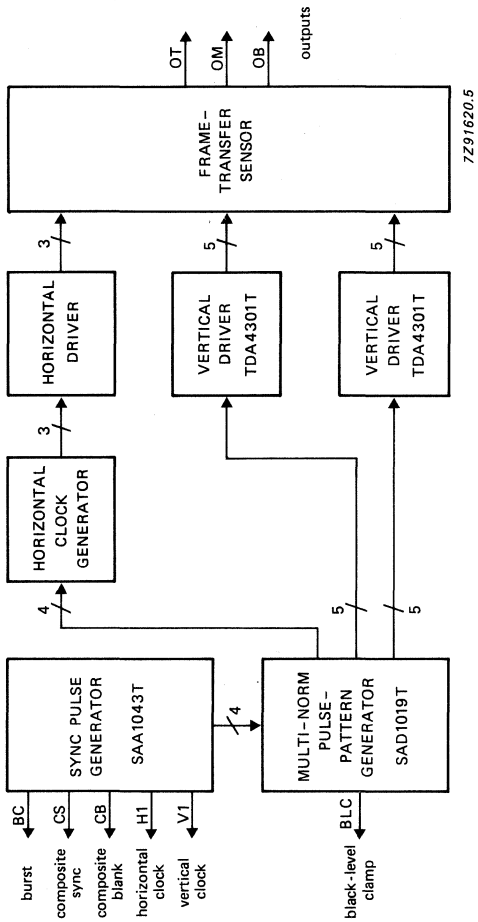


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

MASTER GAIN

GENERAL DESCRIPTION

The TDA4306 is an integrated circuit which controls the amplification of the four output signals (White, Yellow, Green and Cyan) from the frame transfer sensors (NXA1021 to NXA1041). The matching of the four channels is excellent over the whole control and temperature range. An on-chip white clipping circuit protects the white processor (TDA4303) from output signals that are too large. If white clipping occurs, a pulse is available to kill the colour information. Highlights will always be white, not coloured.

Features

- Four variable gain amplifiers
- White clipping circuit
- Blanking switch
- 2.1 V reference voltage

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 20)	$V_P = V_{20\text{-}10}$	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Total power dissipation	P_{tot}	90	140	200	mW
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4306 : 20-lead DIL; plastic (SOT146).
TDA4306T: 20-lead mini-pack; plastic (SO20; SOT163A).

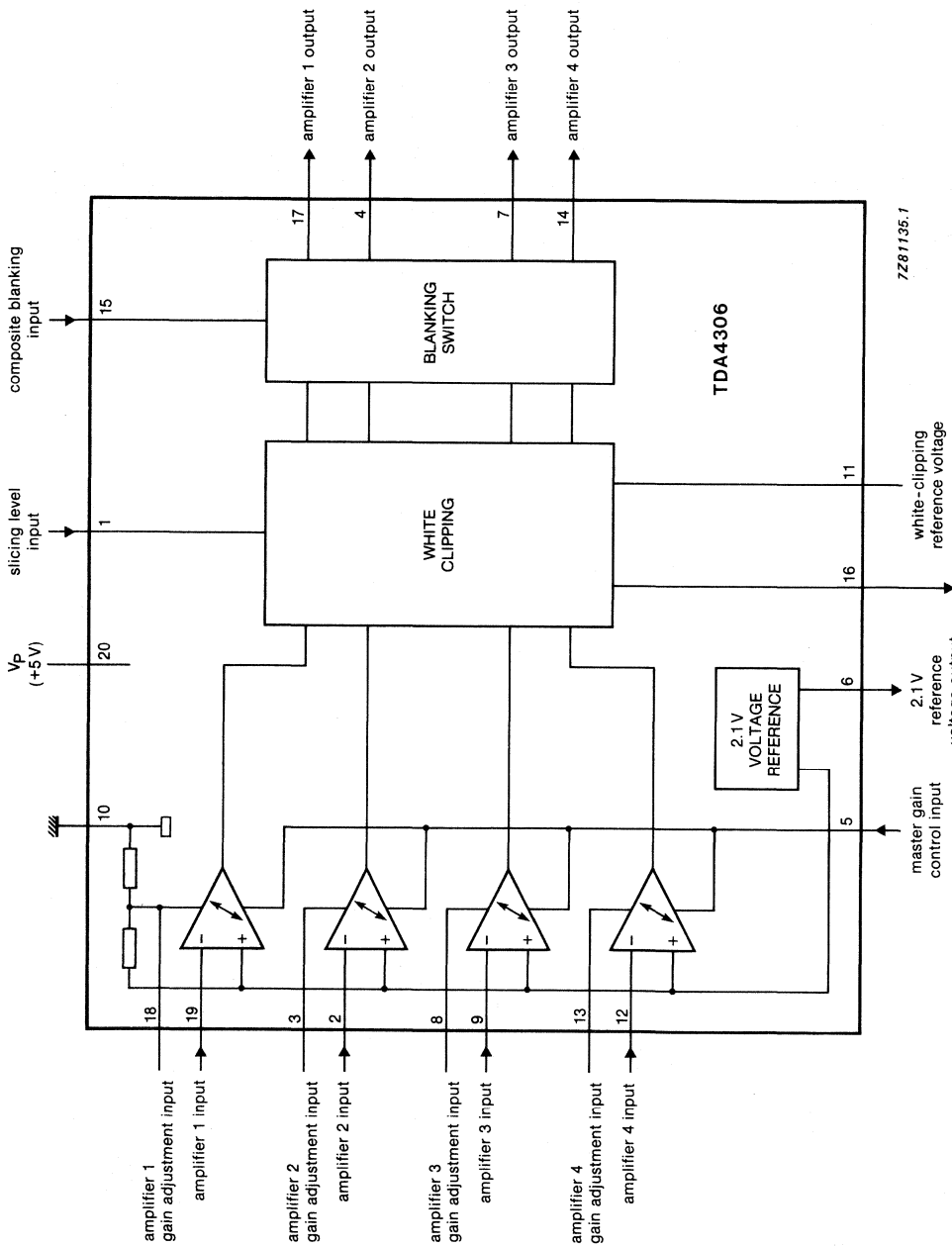


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 20)	V_P	–	12	V
Input voltage (pins 1, 2, 3, 5, 8, 9 12, 13, 15, 18 and 19)	V_I	–	5	V
Output current (pins 17, 4, 7 and 14) $t < 1$ s	I_O	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	370	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

DEVELOPMENT DATA

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{20-10} = 5$ V; $T_{amb} = 25\,^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 20)	V_P	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Temperature drift of V_{ref}	ΔV_{ref}	–	0.18	–	mV/°C
External load current	$I_{L(ext.)}$	–	–	10	mA
Total power dissipation	P_{tot}	90	140	200	mW
Variable gain amplifiers					
Inputs (pins 2, 9, 12 and 19; note 1)					
Input voltage (peak-to-peak value)					
negative video	$V_{n-10(p-p)}$	–	–	−1100	mV
positive video (gain = 1)	$V_{n-10(p-p)}$	–	–	400	mV
Input bias current at $V_I = 2.6$ V	$I_{n(bias)}$	–	2.2	5	μA
Input resistance	$R_{2, 9, 12, 19}$	–	300	–	kΩ
Outputs (pins 17, 4, 7 and 14)					
DC offset voltage of input to output (output = V_{ref})		–	–	−220	mV
DC offset voltage of input to output (output = V_{ref})		–	–	100	mV
Offset voltage between blanked output and V_{ref}		–	–	2	mV
Drift of blanked output voltages	ΔV_O	10	–	–	μV/°C
Output sink current	I_{OS}	–	–	100	μA
Resistive load of output to ground	R_L	1.5	–	–	kΩ
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}−500 mV	–	
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}+ 1200 mV	–	
Output impedance	$\|Z_O\|$	–	100	–	Ω
Power supply rejection ratio (1 kHz)	RR	–	30	–	dB
Bandwidth	B	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Master gain control input (pin 5)					
Gain control range			see Fig. 2		
Input current at V_{5-10} = 0 V	I_5	–	–	30	μA
Matching of gain (note 2) between the 4 channels ($f_{temp.\ range}$ and as $f_{gain\ range\ 2\ to\ x\ 8}$)		–	–	1	%
Gain stability = $f_{temp.range}$ $-20 < t < 60$ °C		–	3	–	%
Differential gain	dG	–	–	1	%
Differential phase	dϕ	–	–	2	deg.
Gain adjustment inputs (pins 18, 3, 8, 13)					
Input voltage range	V_{adj}	0.9	–	1.9	V
Overall gain (MG = 2) at V_{adj} = 0.9 V	G	–	–	2.2	
at V_{adj} = 1.9 V	G	1.5	–	–	
Input current (pins 3, 8 and 13) at V_I = 1,6 V	I_I	–	–	2	μA
Input resistance (pin 18)	R_{18}	–	3.25	–	kΩ
Input voltage (pin 18; open-circuit)	V_I	–	1.2	–	V
White clipping circuit					
Slicing level (pin 1) input voltage range	V_{1-10}	0.5	–	1.8	V
input current at V_{1-10} = 1 V	I_1	–	–	2	μA
White clipping reference voltage (pin 11)	V_{11-10}	–	V_{1-10} x 2.5 V	–	V
Output pulse (pin 16) (peak-to-peak value)	$V_{16-10(p-p)}$	3.0	–	–	V
Output voltage (pin 16) LOW	V_{OL}	–	–	1	V
HIGH	V_{OH}	4	–	–	V
Output sink current (pin 16)	I_{OS}	–	–	0.1	mA
Delay of a variable gain amplifier input to white clipping output	t_d	–	–	100	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Blanking switch (pin 15)					
Composite blanking input voltage					
active HIGH	$V_{15\text{-}10}$	2.4	–	V_P	V
active LOW	$V_{15\text{-}10}$	–	–	1.4	V
Input current at $V_{15\text{-}10}$ = 5 V	I_{15}	–	–	2	μA
Input capacitance	C_I	–	–	5	pF
Delay between blanking input and one of the 4 amplifier outputs	t_d	–	40	100	ns

Notes to the characteristics

1. The maximum input voltage is permitted only if the input voltage minus the DC offset voltage = 2.1 V. If the input voltage minus the DC offset voltage = 1.6 V, the maximum input voltage is 1 V(p-p).
2. Over the range 2 to x 8, after that each channel is adjusted to 0.
   This is possible only if the blanking pulse is switched off and the DC input voltage is equal to V_{ref}.

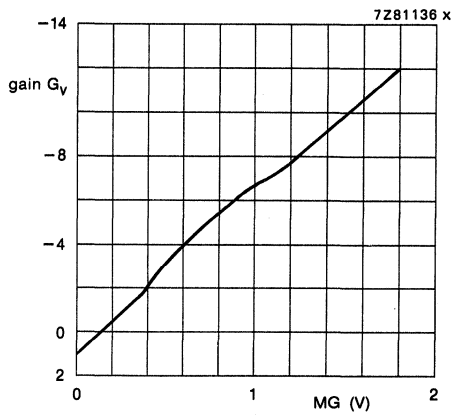


Fig.2 Gain as a function of V_{MG}.

SMALL SIGNAL COMBINATION IC FOR MONOCHROME TV

GENERAL DESCRIPTION

The TDA4500 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4500 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

QUICK REFERENCE DATA

Supply voltage	V_{7-10}, V_{22-10}	typ.	10,5	V
Supply current	I_7	typ.	75	mA
Supply current	I_{22}	typ.	4,5	mA
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	max.	1,7	W

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

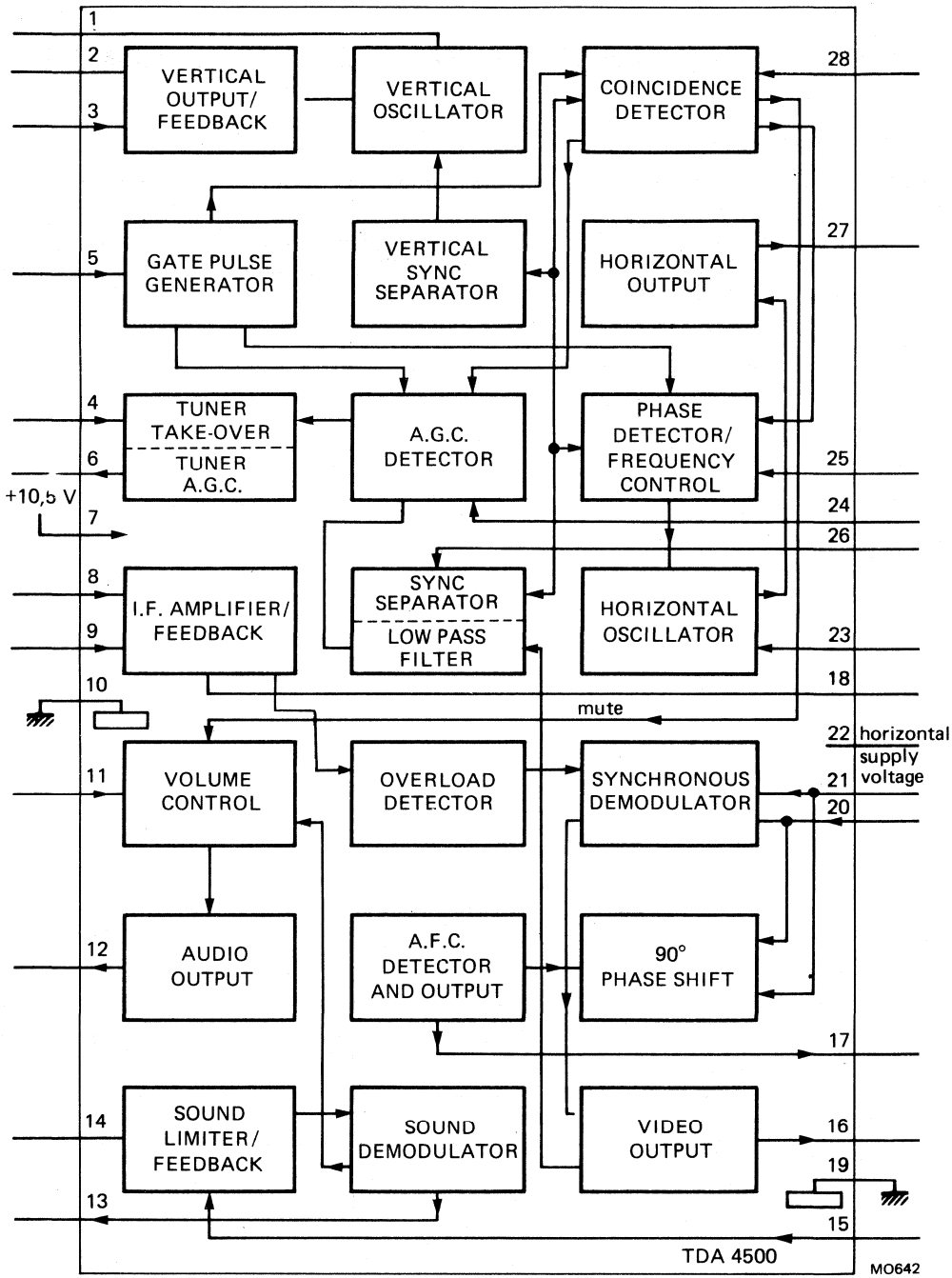


Fig. 1 Block diagram.

PINNING

Pin number	function	Pin number	function
1.	vertical oscillator	15.	sound i.f.
2.	vertical output	16.	video output
3.	vertical feedback	17.	a.f.c. output
4.	top linearity	18.	decoupling capacitor
5.	flyback pulse	19.	ground
6.	tuner a.g.c.	20.	38,5 MHz reference
7.	+10,5 V supply	21.	(38,9 MHz reference)
8.	i.f. input	22.	horizontal supply voltage
9.		23.	horizontal oscillator
10.	ground	24.	top sync detector
11.	volume control	25.	phase detector
12.	sound output	26.	sync separator
13.	6 MHz tuning (5,5 MHz tuning)	27.	horizontal output
14.	decoupling	28.	mute/coincidence detector

FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4500 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 μV for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90° phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 (V_{7-10} = 10,5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3,5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1,5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a Δf of 7,5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3,5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4500 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{7-10}, V_{22-10}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_{7-10} = 10,5 V, V_{22-10} = 10,5 V and T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{7-10}	9,5	10,5	13,2	V
Supply current	I_7	–	75	–	mA
Supply voltage (horizontal oscillator)	V_{22-10}	9,5	10,5	13,2	V
Supply current (horizontal oscillator, note 1)	I_{22}	–	4,5	–	mA
Power dissipation	P_{tot}	–	850	–	mW
Vision i.f. amplifier (pin 8)					
Input sensitivity (onset of a.g.c.) at 39,5 MHz (note 2)	$V_{i(rms)}$	–	70	–	μV
Differential input resistance (note 3)	R_i	–	800	–	Ω
Differential input capacitance (note 3)	C_i	–	6	–	pF
Gain control range	ΔG	–	56	–	dB
Output signal expansion for 50 dB input signal variation (note 4)	ΔV_o	–	1	–	dB
Maximum input signal	$V_{i\ max}$	–	50	–	mV
Video amplifier (note 5)					
Zero signal output level (note 6)	V_{16-10}	–	5	–	V
Top sync output level (note 7)	V_{16-10}	1,2	1,4	1,6	V
Video output signal amplitude (peak-to-peak value)	$V_{16-10(p-p)}$	2,75	3,0	3,25	V
Internal bias current of n-p-n emitter follower output transistor	I_B	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	5	6	–	MHz
Video non-linearity (note 8)		–	–	10	%

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuner a.g.c.					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner)	V_{4-10}	–	3,5	–	V
Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner)	V_{4-10}	–	8	–	V
Maximum tuner a.g.c. output swing	$I_{6\ max}$	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6-10(sat)}$	–	–	300	mV
Leakage current	I_6	–	–	1	μA
A.F.C. circuit (note 9)					
A.F.C. output voltage swing	V_{17-19}	9	–	10	V
Available output current	$\pm I_{17}$	–	1	–	mA
Output voltage at nominal tuning of the reference tuned circuit	V_{17-19}	–	5,25	–	V
Sound circuit					
Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10)	$V_{14\ lim}$	–	400	–	μV
Input resistance at pin 15 (note 11)	R_i	–	3	–	kΩ
A.F. output signal at pin 12 (note 12) (r.m.s. value)	$V_{12-10(rms)}$	170	–	240	mV
Volume control (pin 11) (Fig. 3)					
Voltage with pin 11 disconnected	V_{11-10}	–	6,5	–	V
Current pin 11 short-circuited to ground	I_{11}	–	1	–	mA
Volume control characteristic (note 13)			See Fig. 3		
Value of external control resistor	R_{11-10}	–	5	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization circuit					
Slicing level sync separator (note 14)		–	30	–	%
Holding range PLL		–	±1000	–	Hz
Catching range PLL		–	±600	–	Hz
Control sensitivity video to flyback (note 15)		–	2	–	kHz/μs
Horizontal oscillator					
Free running frequency	f_{osc}	–	15625	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Frequency variations due to supply voltage changes (note 16)	$\Delta f_{osc}/\Delta V$	–	0	–	%
Frequency variation with temperature	$\Delta f_{osc}/\Delta T$	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{osc}	–	–	10	%
Maximum frequency deviation between starting point output and nominal condition	Δf_{osc}	–	–	10	%
Horizontal (push-pull) output					
Output current	I_{27}	10	–	–	mA
Output impedance	R_{27-10}	–	200	–	Ω
Voltage when I_{27} = 10 mA	V_{27-10}	–	2	–	V
	V_{27-22}	–	3	–	V
Duty cycle of output pulse (note 17)	δ	0,35	0,40	0,45	
Flyback input (note 18)					
Minimum required input amplitude (peak-to-peak value)	$V_{5-10(p-p)}$	–	4	–	V
Phase detector switching voltage		–	0	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Coincidence detector (mute) (note 19)					
Voltage in synchronized condition	V_{28-19}	–	9,5	–	V
Voltage in non-synchronized condition (no-signal)	V_{28-19}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{28-19}	4,5	5,0	5,5	V
Switching level to activate the 'mute' function (transmitter identification)	V_{28-19}	2,25	2,5	2,75	V
Output current; in-sync (peak-to-peak value)	$I_{28(p-p)}$	–	1	–	mA
Vertical oscillator					
Free running frequency	f_{osc}	–	47,5	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	1×10^{-4}	–	K^{-1}
Frequency shift due to a supply voltage change from 9,5 to 12 V	$\Delta f_{osc}/\Delta V$	–	5	–	%
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_{2-10}	–	2	–	kΩ
Feedback input (pin 3)					
D.C. input voltage	V_{3-10}	4,75	5	5,25	V
A.C. input voltage (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	10	μA
Non-linearity of deflection current at V_P = 10,5 V		–	–	2,5	%

Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) – value at top sync level at which the video amplitude has dropped 0,5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal (V_{8-9}) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. Q_L of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5,5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

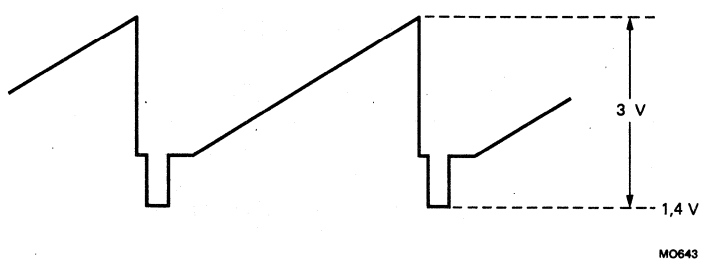


Fig. 2 Video output signal.

Notes to characteristics (continued)

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4,5 V so that the time constant is fast and the sound is still available.

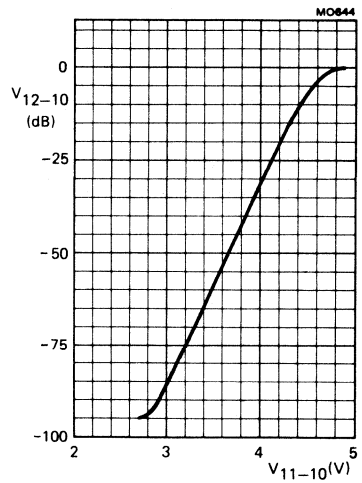


Fig. 3 Volume control characteristic at f = 1 kHz.

APPLICATION INFORMATION

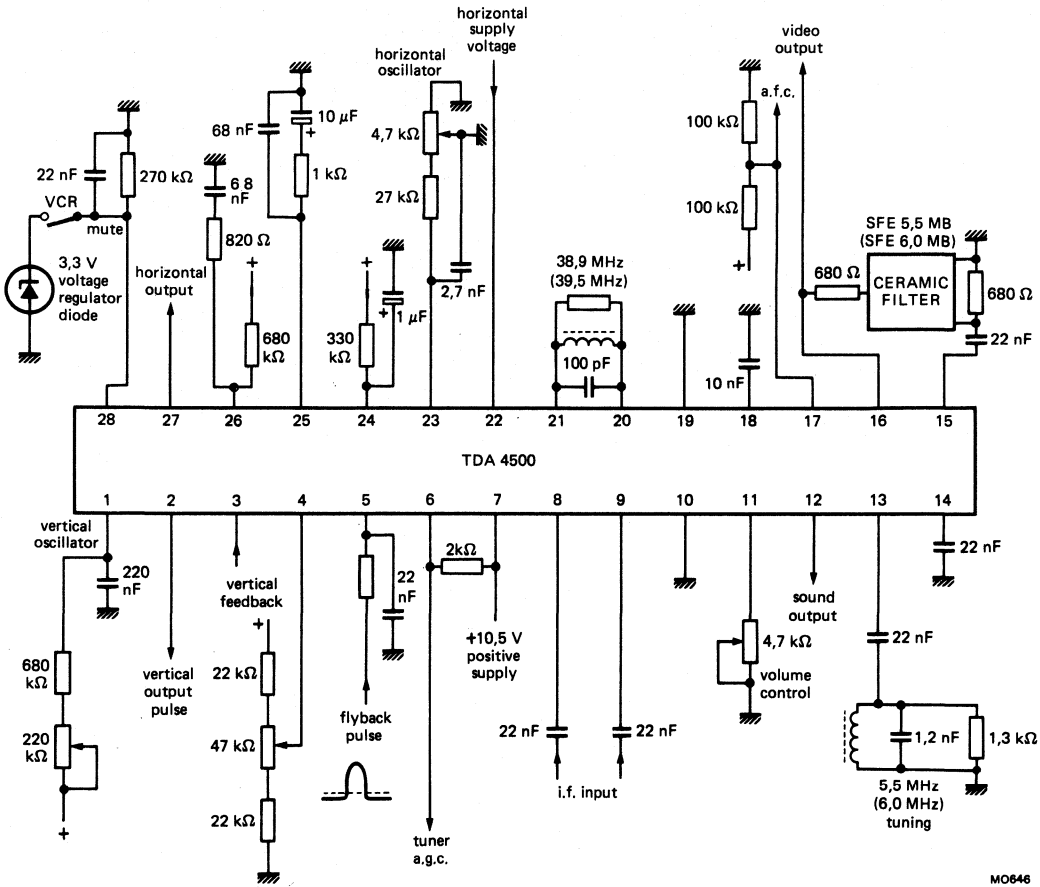


Fig. 4 Typical application circuit.

SMALL-SIGNAL COMBINATION IC FOR BLACK-AND-WHITE TV

GENERAL DESCRIPTION

This IC contains all small-signal functions required for black-and-white tv reception. The only additional circuits needed to complete the receiver are a tuner and the deflection output stages.

The IC includes a vision i.f. amplifier with synchronous demodulator and a.f.c. circuit, an a.g.c. detector with tuner output and fully synchronized vertical and horizontal drive outputs.

Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and internal muting.

The TDA4503 may also be adapted for simple colour tv reception by the use of an external, three-level sandcastle pulse generator.

Features

- Vision i.f. amplifier with synchronous demodulator
- A.G.C. detector and amplifier with a.g.c. output to tuner
- A.F.C. circuit
- Video preamplifier
- Audio preamplifier
- Sound i.f. amplifier and demodulator
- D.C. volume control
- Horizontal synchronization circuit
- Transmitter identification and mute circuit
- Vertical synchronization circuit and sawtooth generator

QUICK REFERENCE DATA

Supply voltage (pin 7)	$V_{7\text{-}10}$	typ.	10,5 V
Supply current (pin 7)	I_7	typ.	82 mA
Supply voltage (pin 22)	$V_{22\text{-}10}$	typ.	10,5 V
Supply current (pin 22)	I_{22}	typ.	5 mA
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to +150 °C
Power dissipation	P_{tot}	typ.	920 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

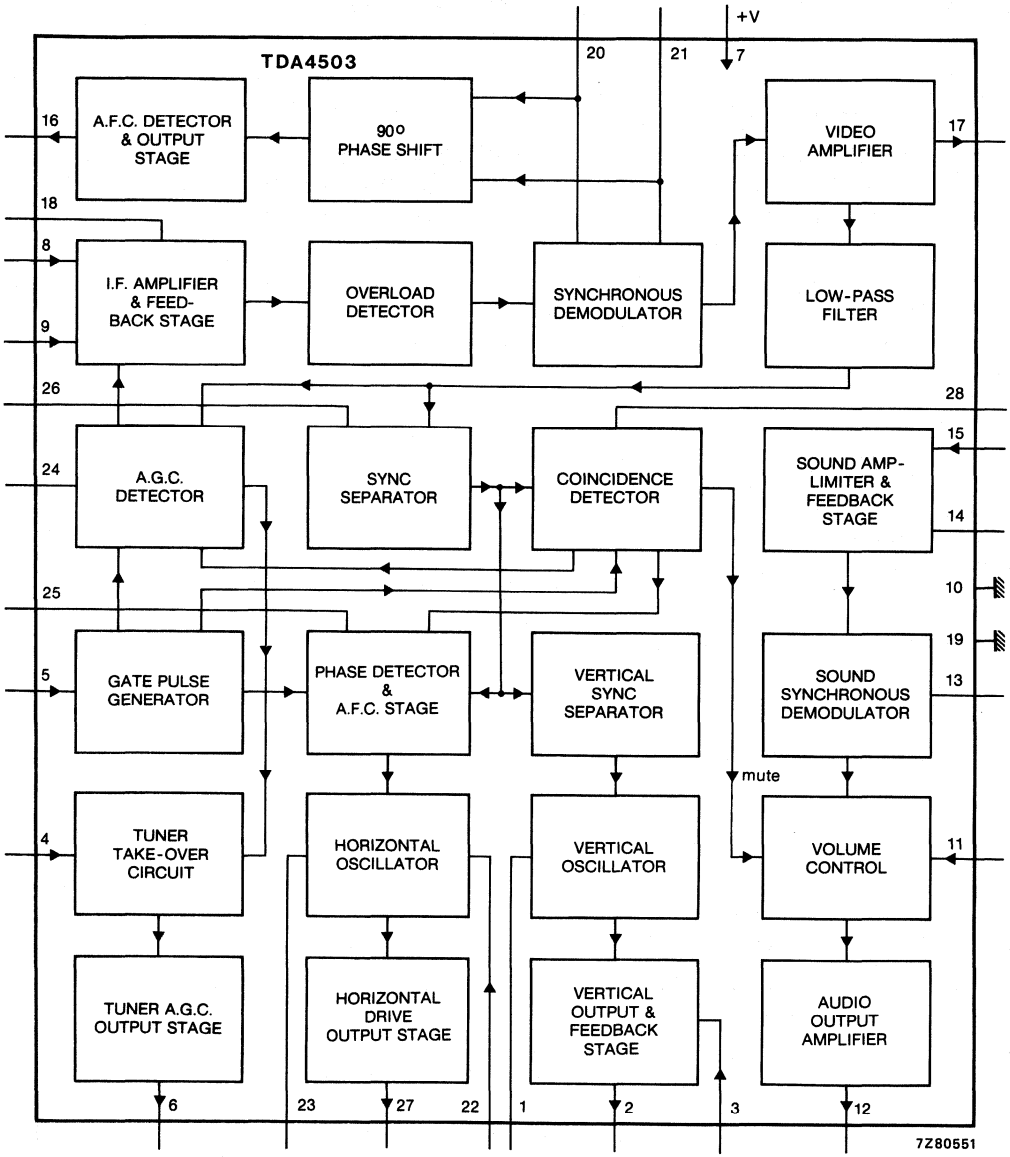


Fig. 1 Block diagram.

PINNING

1. Vertical oscillator input
2. Vertical drive output
3. Vertical drive feedback
4. Tuner take-over input
5. Flyback pulse input
6. A.G.C. output to tuner
7. Power supply input
8. I.F. input
9. I.F. input
10. Power supply return (ground)
11. Volume control
12. Audio output
13. Sound demodulator reference input
14. Sound i.f. decoupling
15. Sound i.f. input
16. A.F.C. output
17. Video output
18. I.F. amplifier decoupling
19. Ground (for critical circuits)
20. Synchronous demodulator
21. Synchronous demodulator
22. Horizontal oscillator start input
23. Horizontal oscillator
24. A.G.C. time constant
25. Horizontal phase detector filter
26. Sync separator slicing level
27. Horizontal drive output
28. Coincidence detector time constant

FUNCTIONAL DESCRIPTION

I.F. amplifier, demodulator and A.F.C.

The i.f. amplifier operates with symmetrical inputs at pins 8 and 9 and has an input impedance suitable for SAW filter application. The amplifier sensitivity gives a peak-to-peak output voltage of 3 V for an r.m.s. input of 70 μV. The demodulator and the a.f.c. circuit share an external reference tuned circuit (pins 20 and 21) and an internal RC-network provides the phase-shifting necessary for a.f.c. operation. The a.f.c. circuit provides a control voltage output with a (typical) swing of 9 V from pin 16 (V_P = 10,5 V).

A.G.C. circuit

Gating of the a.g.c. detector is performed to reduce sensitivity of the i.f. amplifier to external electrical noise. The a.g.c. time constant is provided by an RC-network connected to pin 24. The typical gain control range of the i.f. amplifier is 60 dB. Tuner a.g.c. voltage is supplied from pin 6 and is suitable for tuners with pnp or npn RF stages. The sense of the AGC (to incease in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at pin 4 (V_4 = 3,5 V (typ) for positive a.g.c.; V_4 = 8 V (typ) for negative a.g.c.).

Video amplifier

The video signal output from pin 17 has a peak-to-peak value of 3 V (top sync level = 1,5 V) and carries negative-going sync. In order to retain sound information at pin 17, the video signal is not blanked during flyback periods.

Sound circuit

The sound i.f. signal present at the video output (pin 17) is coupled to the sound circuit by a band-pass filter to pin 15. The sound circuit has an amplifier-limiter stage, a synchronous demodulator with reference tuned circuit at pin 13, a volume control stage and an output amplifier. The volume control has a range of approximately 80 dB and the audio output signal at maximum volume and with Δf = 7,5 kHz is 320 mV (r.m.s. value). The sound output signal is suppressed when no input signal is detected.

Synchronization circuits

The sync separator slicing level is determined by an external resistor network at pin 26. The slicing level is referred to the top sync level and the recommended value for slicing is 30%. Internal protection from electrical noise is included.

A gated phase detector compares the phase of the separated sync pulses with a sawtooth waveform obtained from the flyback pulse at pin 5. In-sync and out-of-sync conditions are detected by the coincidence detector at pin 28 (this circuit also gives transmitter identification). During the out-of-sync condition, gating of the phase detector is switched off and the output current from the phase detector increases to give the detector a short time-constant and thus a fast response. This condition can be imposed by clamping the voltage at pin 28 to 3,5 V for the reception of VCR signals.

The horizontal oscillator frequency is controlled by the output voltage of the phase detector circuit. The horizontal drive output from pin 27 has a duty factor of 40%.

Vertical sync pulses are separated by an internal integrating network and are used to trigger the vertical oscillator. A comparator circuit compares the vertical sawtooth waveform, generated by the vertical oscillator, with feedback from the deflection coils and supplies the drive voltage for the output stage at pin 2.

Power supplies

The main supply is to pin 7 (positive supply) and pin 10 (ground). The horizontal oscillator is supplied from pin 22 to facilitate starting of the oscillator from a high-voltage rail. A special ground connection at pin 19 is used by critical voltage dividers in the feedback loops of the vision and sound i.f. circuits.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-10}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to +150 °C

CHARACTERISTICS

V_{7-10} = 10,5 V; V_{22-10} = 10,5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 7)	V_{7-10}	9,5	10,5	13,2	V
Supply current (pin 7)	I_7	–	82	100	mA
Supply voltage (pin 22)	V_{22-10}	9,5	10,5	13,2	V
Supply current (pin 22) (note 1)	I_{22}	–	5	6,5	mA
Total power dissipation	P_{tot}	–	920	1150	mW
Vision i.f. amplifier (pins 8 and 9)					
Input sensitivity at 38,9 MHz (note 2)	V_{8-9}	40	80	120	μV
Input sensitivity at 45,75 MHz (note 2)	V_{8-9}	–	90	–	μV
Differential input resistance (pin 8 to 9)	R_{8-9}	–	1,3	–	kΩ
Differential input capacitance (pin 8 to 9)	C_{8-9}	–	5	–	pF
A.G.C. range		–	59	–	dB
Maximum input signal	V_{8-9}	50	70	–	mV
Expansion of output signal (pin 17) for 50 dB variation of input signal (pins 8 and 9) (note 3)	ΔV_{17-10}	–	0,5	1,0	dB
Video amplifier (note 4)					
Output level for zero signal input (zero point of switched demodulator)	V_{17-10}	4,2	4,5	4,8	V
Output signal top sync level (note 5)	V_{17-10}	1,25	1,45	1,65	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Amplitude of video output signal (peak-to-peak value)	$V_{17\text{-}10(p\text{-}p)}$	2,4	2,7	3,0	V
Internal bias current of output transistor (npn emitter follower)	$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	–	5	–	MHz
Differential gain (Fig. 4 and note 6)	G_{17}	–	6	–	%
Differential phase (Fig. 4 and note 6)		–	4	–	%
Video non-linearity over total video amplitude (peak white to black)		–	–	10	%
Intermodulation (Figs 5 and 6) at gain control = 45 dB					
f = 1,1 MHz; blue;		55	60	–	dB
f = 1,1 MHz; yellow;		50	54	–	dB
f = 3,3 MHz; blue;		60	66	–	dB
f = 3,3 MHz; yellow;		55	59	–	dB
Signal-to-noise ratio (note 7)					
at V_i = 10 mV	S/N	50	54	–	dB
at end of a.g.c. range	S/N	50	56	–	dB
as a function of input signal		see Fig. 7			
Residual A.M. of intercarrier output signal (note 8)		–	5	10	%
Residual carrier signal		–	7	30	mV
Residual 2nd harmonic of carrier signal		–	3	30	mV
Tuner a.g.c. (note 9)					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (NPN tuner)	$V_{4\text{-}10}$	–	3,5	–	V
Starting point take-over at $V_{4\text{-}10}$ = 5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,4	2,0	mV
Starting point take-over at $V_{4\text{-}10}$ = 1,2 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Take-over voltage (pin 1) for negative-going tuner a.g.c. (PNP tuner)	$V_{4\text{-}10}$	–	8	–	V
Starting point take over at $V_{4\text{-}10}$ = 9,5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,3	2,0	mV
Starting point take over at $V_{4\text{-}10}$ = 5,6 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Maximum tuner a.g.c. output swing	I_{6max}	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6\text{-}10(sat)}$	–	–	300	mV
Leakage current at pin 6	I_6	–	–	1	μA
Input signal variation required for complete tuner control	$\Delta V_{8\text{-}9}$	0,5	2	4	dB

parameter	symbol	min.	typ.	max.	unit
A.F.C. circuit (pin 16; note 10)					
A.F.C. output voltage swing (peak-to-peak value)	$V_{16\text{-}10(p\text{-}p)}$	9	–	10	V
Available output current	$\pm I_{16}$	–	1	–	mA
Control steepness at					
100% picture carrier		20	40	80	mV/kHz
10% picture carrier		–	15	–	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit	$V_{16\text{-}10}$	–	5,25	–	V
Output voltage without input signal	$V_{16\text{-}10}$	2,7	6,0	8,5	V
Sound circuit					
Input limiting voltage (note 11) (r.m.s. value) at $V_o = V_{o\ max}$ - 3 dB	$V_{15\ lim}$	–	2	–	mV
Input resistance at $V_{i(rms)}$ = 1 mV	$R_{15\text{-}10}$	–	2,6	–	kΩ
input capacitance at $V_{i(rms)}$ = 1 mV	$C_{15\text{-}10}$	–	6	–	pF
A.M. rejection (Figs 8 and 9) at					
V_i = 10 mV	AMR	–	35	–	dB
V_i = 50 mV	AMR	–	43	–	dB
A.F. output signal (note 12) (r.m.s. value)	$V_{12\text{-}6(rms)}$	220	320	–	mV
A.F. output impedance	$Z_{12\text{-}10}$	–	150	–	Ω
Total harmonic distortion (note 12)	THD	–	1	–	%
Ripple rejection at					
f_k = 100 Hz, volume control 20 dB	RR	–	22	–	dB
when muted	RR	–	26	–	dB
Output voltage in mute condition	$V_{12\text{-}10}$	–	2,6	–	V
Signal-to-noise ratio; weighted noise (CCIR 468)	S/N	–	47	–	dB
Volume control					
Voltage (pin 11 disconnected)	$V_{11\text{-}10}$	–	6,9	–	V
Current (pin 11 connected to ground)	I_{11}	–	1	–	mA
External control resistor (note 13)	$R_{11\text{-}10}$	–	5	–	kΩ
Suppression of output signal during mute condition		–	66	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization					
Slicing level sync separator (note 14)		–	30	–	%
Phase-lock loop holding range		±800	±1100	±1500	Hz
Phase-lock loop catching range		±600	1000	–	Hz
Control sensitivity video to flyback (note 15)		–	2,3	–	kHz/μs
Delay between leading edge of sync pulse and zero cross-over of sawtooth (pin 5)		–	3	–	μs
Horizontal oscillator (pin 23)					
Free-running frequency R = 35 kΩ; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		–	–	4	%
Frequency variation due to change of supply voltage from 8 to 12 V	Δf_{fr}	–	0	0,5	%
Temperature coefficient	TC	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{fr}	–	–	10	%
Maximum frequency deviation(V_{7-10} = 8 V)	Δf_{fr}	–	–	10	%
Horizontal output (pin 27)					
Output current	I_{27}	5	–	–	mA
Output impedance	R_{27}	–	200	–	Ω
Output voltage at I_{27} = 5 mA	V_{27-10}	–	1,4	–	V
	V_{27-22}	–	2,5	–	V
Duty factor of horizontal output signal (note 16)	α	0,35	0,40	0,45	%
Rise and fall times of output pulse	t_r, t_f	–	400	–	ns
Flyback input (pin 5)					
Amplitude of input pulse	V_5	2	4	6	V
Voltage at which gate pulse generator changes state (note 17)	V_5	–	0	–	V

parameter	symbol	min.	typ.	max.	unit
Coincidence detector mute output (pin 28) (note 18)					
Voltage for in-sync condition	V_{28-10}	–	9,5	–	V
Voltage for no-sync condition (no input signal)	V_{28-10}	–	1,0	1,5	V
Voltage level for phase detector to switch from slow to fast	V_{28-10}	3,7	4,1	4,5	V
Fast-to-slow hysteresis		–	1	–	V
Voltage level to activate mute function (transmitter identification)	V_{28-10}	2,25	2,5	2,75	V
Output current for in-sync condition (peak-to-peak value)	$I_{22(p-p)}$	0,7	1,0	–	mA
Vertical oscillator (pin 1)					
Free-running frequency at C = 220 nF; R = 560 kΩ	f_{fr}	–	47,5	–	Hz
Spread with fixed external components		–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	–	$2x10^{-4}$	K^{-1}
Frequency variation due to change of supply voltage from 9,5 to 12 V	Δf_{fr}	–	3	5	%
Leakage current at pin 1	I_1	–	–	1,6	μA
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_2	–	2	–	kΩ
Feedback input (pin 3)					
Input voltage					
d.c. component	V_{3-10}	4,0	5,0	5,5	V
a.c. component (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	12	μA
Non-linearity of deflection current at V_{7-10} = 10,5 V	ΔI_3	–	–	2,5	%
Delay between leading edge of vertical sync and start of vertical oscillator flyback		6	–	10	μs

Notes to the characteristics

1. The horizontal oscillator can be started by supplying a current of 6 mA to pin 22. Taking this current from the mains rectifier allows the positive supply voltage to pin 7 to be derived from the horizontal output stage (the load current of pin 27 is additional to the 6 mA quoted).
2. At start of a.g.c.
3. Measured with 0 dB = 200 μV.
4. Measured at 10 mV (rms) top sync output signal.
5. Signal with negative-going sync; top white = 10% of the top sync amplitude.
6. Measured with test line as shown in Fig. 4. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest values relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angles.
7. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20\log \frac{V_o \text{ black-to-white}}{V_{i(rms)} \text{ at } B = 5 \text{ MHz}}.$$

8. Measured with a sawtooth-modulated input signal: m = 90%; $V_{i(rms)}$ = 10 mV;

$$\text{Amplitude modulation} = \frac{V_o \text{ SC at top sync} - V_o \text{ SC at white}}{V_o \text{ SC at top sync} + V_o \text{ SC at white}} \times 100\%.$$

(SC = sound carrier)

9. Starting point of tuner take-over for an npn tuner is when I_6 = 1,8 mA, and for a pnp tuner is when I_6 = 0,2 mA.
10. Measured at $V_{8\text{-}9(rms)}$ = 10 mV and pin 16 loaded with 2 x 100 kΩ between V_7 and ground. Reference tuned circuit Q-factor = 36.
11. Reference tuned circuit Q-factor = 16; audio frequency = 1 kHz; carrier frequency = 5,5 MHz.
12. The demodulator tuned circuit must be tuned for minimum distortion; output signal is measured at Δf = 7,5 kHz; other measurements are at Δf = 27,5 kHz.
13. Volume control can be realized by a variable resistor (5 kΩ) connected between pin 11 and ground, or by a variable voltage direct to pin 11 (the low value of input impedance to pin 11 must be taken into account).
14. The sync separator is noise-gated; the slicing level is referred to the top sync level and is independent of the video signal. The value stated is a percentage of the sync pulse amplitude, the level being dependent on external resistors connected to pin 26.
15. The phase detector current is increased by a factor of 7 during catching and when the phase detector is switched to 'fast' via pin 28, thus ensuring a wide catching range and a high dynamic loop gain.
16. The negative-going edge initiates switching-off of the line output transistor (simultaneous driver).
17. The circuit requires an integrated flyback pulse. Gate pulses for a.g.c. and coincidence detectors are obtained from the sawtooth waveform.
18. The functions of in-sync, out-of-sync and transmitter identification are combined on pin 28. For the reception of VCR signals, V_{28} must be fixed between 3 V and 4,5 V so that the time constant is fast and sound information is preserved.

APPLICATION INFORMATION

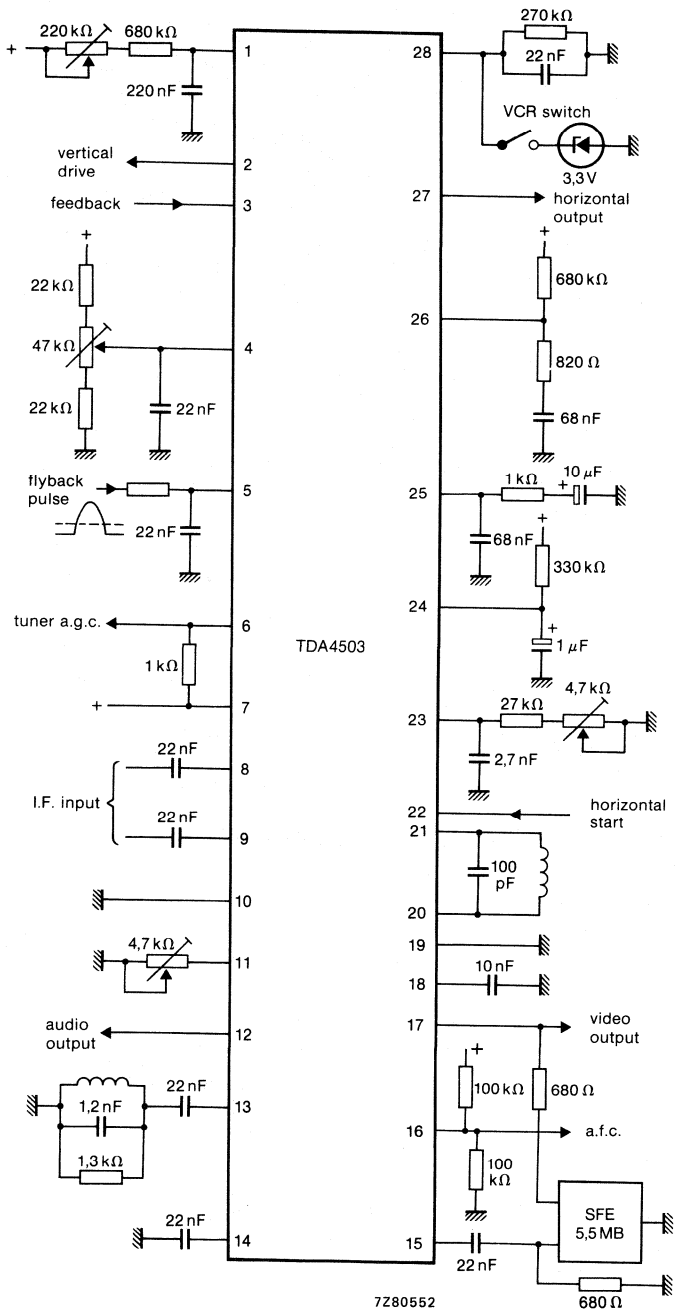


Fig. 2 Application circuit diagram.

APPLICATION INFORMATION (continued)

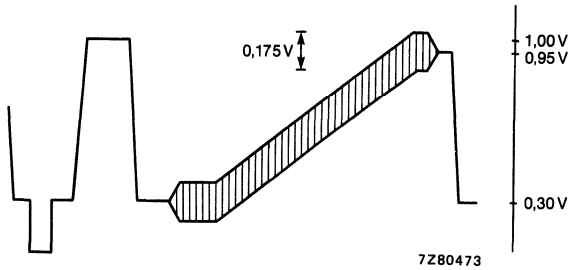


Fig. 3 Video output signal.

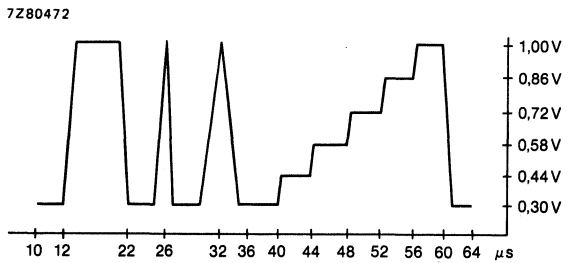


Fig. 4 E.B.U. test signal - line 330.

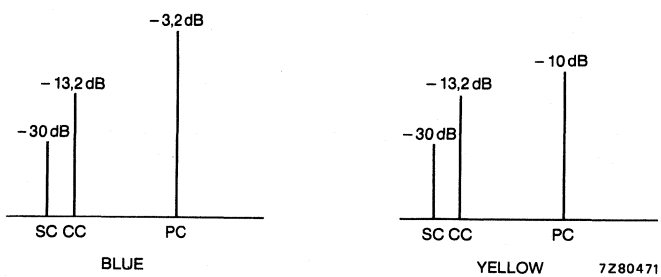


Fig. 5 Input signal conditions for intermodulation test: SC = sound carrier; CC = chrominance carrier; PC = picture carrier; all values are with respect to the top sync level.

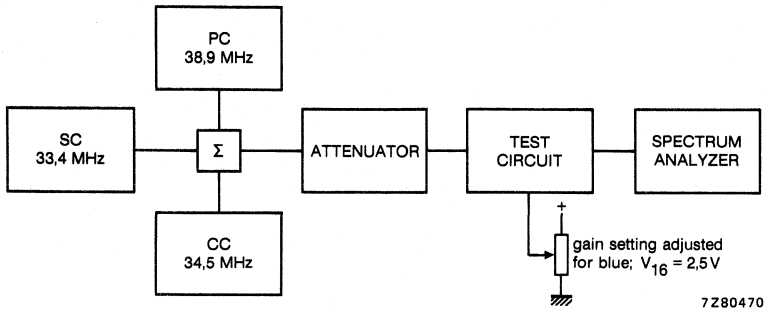


Fig. 6 Circuit for intermodulation test:

$$\text{value at 1,1 MHz} = 20\log \frac{V_o \text{ at 4,4 MHz}}{V_o \text{ at 1,1 MHz}} + 3{,}6 \text{ dB};$$

$$\text{value at 3,3 MHz} = 20\log \frac{V_o \text{ at 4,4 MHz}}{V_o \text{ at 3,3 MHz}}.$$

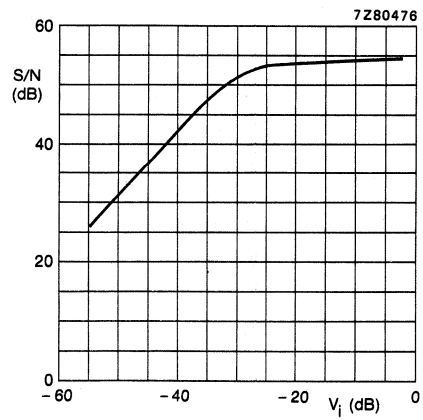


Fig. 7 Signal-to-noise ratio as a function of input voltage.

APPLICATION INFORMATION (continued)

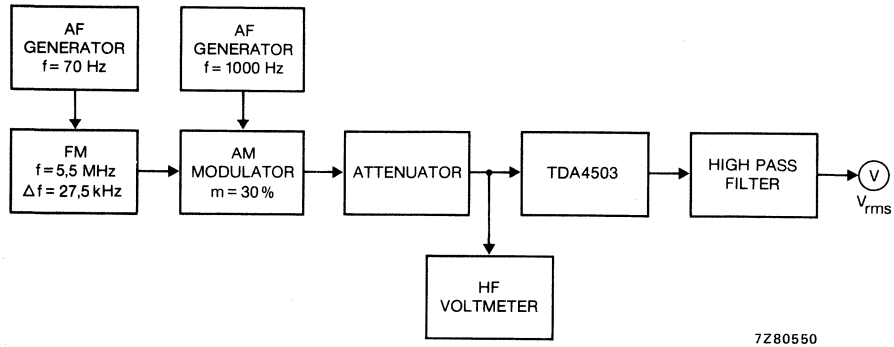


Fig. 8 Circuit for amplitude modulation rejection test.

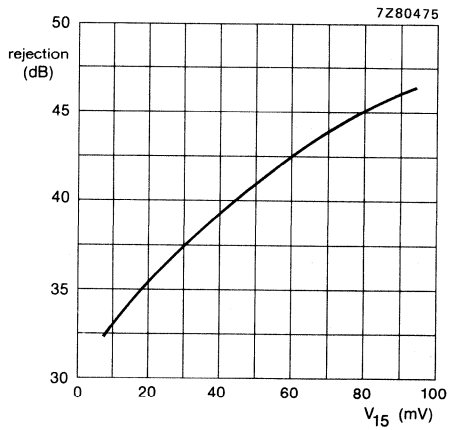


Fig. 9 Typical amplitude modulation rejection curve.

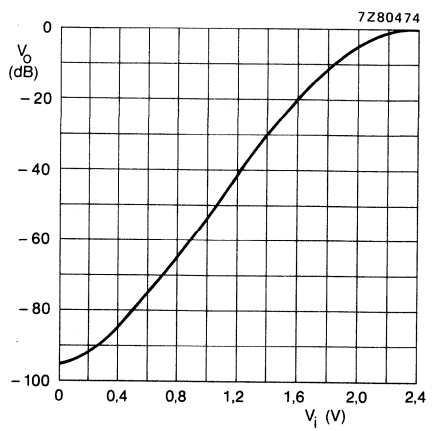


Fig. 10 Volume control characteristic.

PAL DECODER

The TDA4510 is a colour decoder for the PAL standard, which is pin sequent compatible with multi-standard decoder TDA4555 and also pin compatible with NTSC decoder TDA4570. It incorporates the following functions:

Chrominance part

- Gain controlled chrominance amplifier with operating point control stage
- Chrominance output stage for driving the 64 μs delay line
- Blanking circuit for the colour burst signal
- Automatic chrominance control (ACC) with sampled rectifier during burst-key

Oscillator and control voltage part

- Reference oscillator for double subcarrier frequency
- Gated phase comparison
- Identification demodulator and automatic colour killer
- Sandcastle pulse detector
- Service switch

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Colour switching stages
- Separate colour switching output
- (B-Y) and (R-Y) signal output stages
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7-3}$	typ.	12 V
Supply current	$I_P = I_7$	typ.	50 mA
Chrominance input signal (peak-to-peak)	$V_{9-3(p-p)}$		10 to 400 mV
Chrominance output signal (peak-to-peak)	$V_{6-3(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
–(R-Y) signal	$V_{1-3(p-p)}$	typ.	1,05 V ± 2 dB
–(B-Y) signal	$V_{2-3(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse, required amplitude for			
burst gating level	V_{15-3}	typ.	7,7 V
horizontal pulse separation	V_{15-3}	typ.	4,5 V
vertical and horizontal pulse separation	V_{15-3}	typ.	2,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

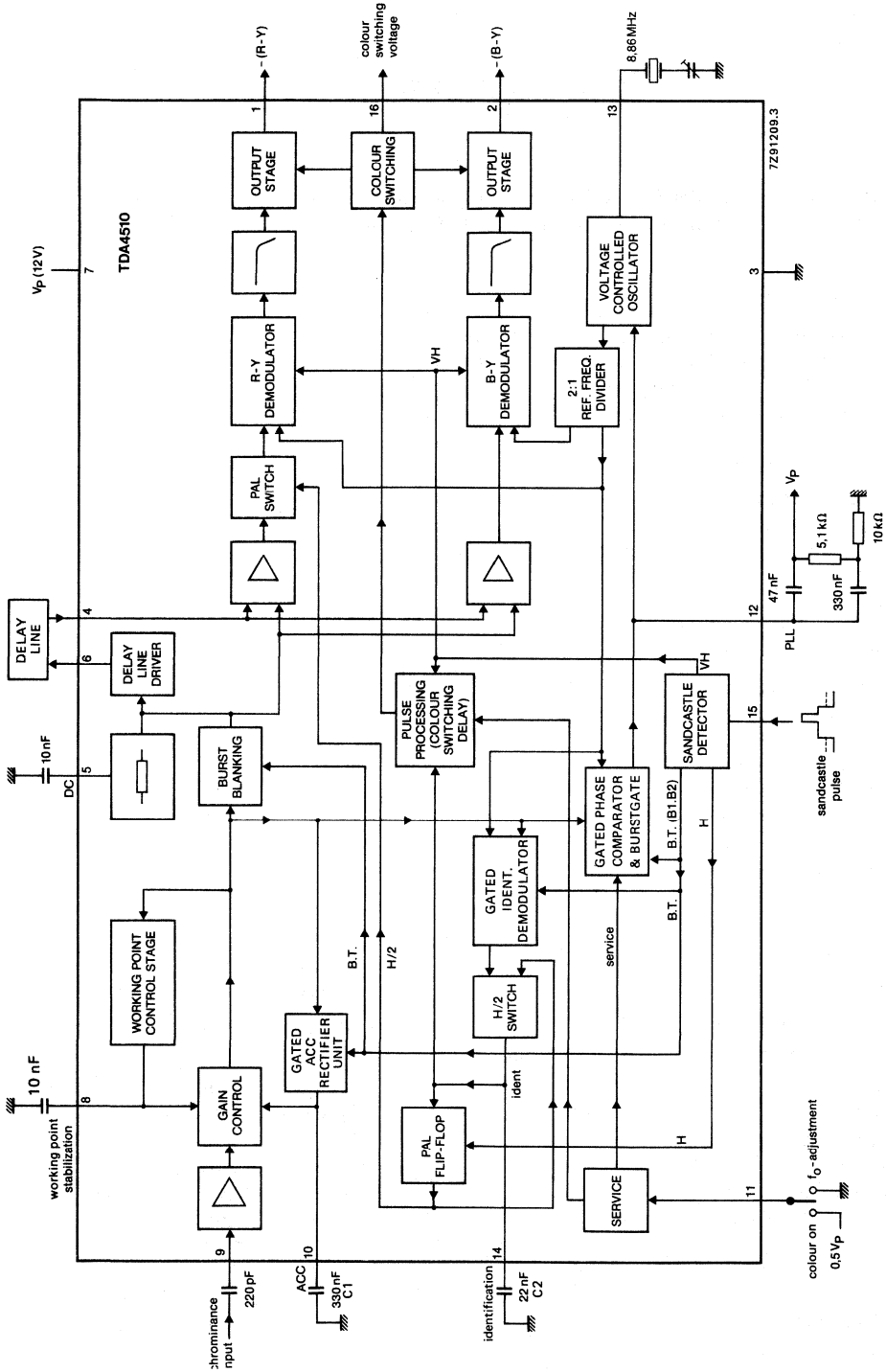


Fig. 1 Block diagram.

External capacitors in Fig. 1

C1 filter capacitor for control voltage (pin 10)
C2 filter capacitor for identification signal (pin 14)

FUNCTIONAL DESCRIPTION

DIVIDER STAGES

The divider stages provide −(R-Y) and −(B-Y) reference signals with the correct 90 degrees relation for the demodulators.

PHASE COMPARATOR

The phase comparator compares the −(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator.

IDENTIFICATION DEMODULATOR

The identification demodulator delivers a positive going identification signal for PAL-signals at pin 14, also used for the automatic colour-killer.

SERVICE SWITCH

The service switch has two functions. The first position ($V_{14-3} < 1$ V) allows the adjustment of the reference oscillator. Therefore the colour is switched on and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5$ V) switches the colour on and the output signals can be observed.

DEVELOPMENT DATA

SANDCASTLE PULSE DETECTOR

Sandcastle pulse detector for burst-gate, line and blanking (horizontal and vertical) pulse detection. The vertical part of the sandcastle pulse is needed for the internal colour-on and colour-off delay.

PULSE PROCESSING PART

Pulse processing part which shall prevent a premature switching on of the colour. The colour-on delay, two or three field periods after identification of the PAL signal, is achieved by a counter. The colour is switched off immediately or at the latest one field period after disappearance of the identification voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents				
at pins 1 and 2	$-I_{1,2}$	max.	5	mA
at pin 6	$-I_6$	max.	15	mA
at pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}	−25 to + 150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	I_7	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9\text{-}3(p\text{-}p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value)					
with 75% colour bar signal	$V_{9\text{-}3(p\text{-}p)}$	–	100	–	mV
Input impedance	$Z_{9\text{-}3}$	–	3,3	–	kΩ
Input capacitance	$C_{9\text{-}3}$	–	4	–	pF
Colour ON					
Chrominance output voltage (peak-to-peak)					
with 75% colour bar signal	$V_{6\text{-}3(p\text{-}p)}$	–	1,6	–	V
d.c. voltage at chrominance output	$V_{6\text{-}3}$	–	8,2	–	V
Oscillator and control voltage part					
Oscillator frequency	f_o	–	8,8	–	MHz
Input resistance	$R_{13\text{-}3}$	–	350	–	Ω
Catching range					
(depending on RC-network at pin 12)	f	± 400	–	–	Hz
Control voltage					
without burst signal	$V_{14\text{-}3}$	–	6,0	–	V
colour on switching threshold	$V_{14\text{-}3}$	–	6,6	–	V
hysteresis of colour switching	$V_{14\text{-}3}$	–	150	–	mV
flip-flop correction (FFC) voltage	$V_{14\text{-}3}$	–	5,5	–	V
hysteresis of FFC	$V_{14\text{-}3}$	–	170	–	mV
Colour-on delay		2	–	3	f.p.*
Colour-off delay		0	–	1	f.p.*
First service position (PLL is inactive					
for oscillator adjustment, colour on)	$V_{11\text{-}3}$	0	–	1	V
second service position (colour on)	$V_{11\text{-}3}$	5	–	–	V
Colour switching output (open npn emitter)					
output current	$-I_{16}$	–	–	5	mA
colour-on voltage	$V_{16\text{-}3}$	–	6	–	V
colour-off voltage	$V_{16\text{-}3}$	–	0	–	V
Demodulator part					
Delayed chrominance input signal					
(peak-to-peak value)					
with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	–	200	–	mV
Colour difference output signals					
(peak-to-peak value)					
–(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	1,06	1,33	1,67	V

parameter	symbol	min.	typ.	max.	unit
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1\text{-}3}/V_{2\text{-}3}$	0,71	0,79	0,87	V
D.C. voltage at colour difference outputs	$V_{1;\,2\text{-}3}$	–	7,7	–	V
Residual carrier voltage at colour difference outputs					
1 x subcarrier frequency (4,4 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
2 x subcarrier frequency (8,8 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
Sandcastle pulse detector					
Thresholds:					
Field- and line-pulse separation pulse ON	$V_{15\text{-}3}$	1,3	1,6	1,9	V
Required pulse amplitude	$V_{15\text{-}3}$	2,0	2,5	3,0	V
Line pulse separation; pulse ON	$V_{15\text{-}3}$	3,3	3,6	3,9	V
Required pulse amplitude	$V_{15\text{-}3}$	4,1	4,5	4,9	V
Burst pulse separation; pulse ON	$V_{15\text{-}3}$	6,6	7,1	7,6	V
Required pulse amplitude	$V_{15\text{-}3}$	7,7	–	–	V
Input voltage during horizontal scanning	$V_{15\text{-}3}$	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

DEVELOPMENT DATA

* f.p. is shortening for field periods in this case.

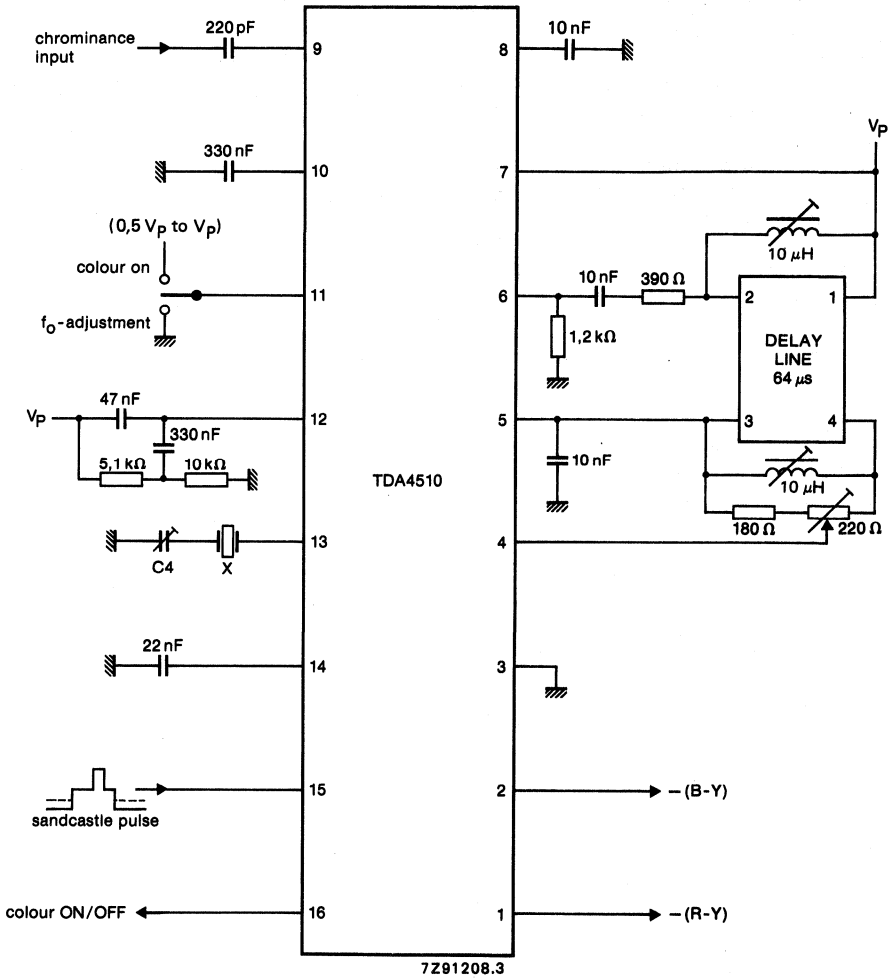


Fig. 2 Application information and test circuit.

C4 = 5 to 27 pF, X = 8,8 MHz; nominal frequency 8,867 238 MHz; resonance resistance 60 Ω, load capacitance 20 pF, dynamic capacitance 22 fF and static capacitance 5,5 pF.

SECAM DECODER

GENERAL DESCRIPTION

The TDA4532 is a monolithic integrated colour decoder for SECAM television receivers. It is pin compatible with the multi-standard decoder TDA4555.

Features

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with rectifier which is disabled during horizontal and vertical flyback
- Chrominance output stage for driving the 64 μs glass delay line
- Limiter stages for direct and delayed chrominance signal
- SECAM permutator

Identification part

- Identification demodulator which is active during the horizontal identification signal and/or during part of the vertical flyback
- Identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Service switch for forced colour on
- Sandcastle pulse for detection of burst gating pulse, horizontal blanking pulse, combined horizontal and vertical blanking pulse. The vertical part of the sandcastle pulse is required for the internal colour ON and colour OFF delay
- Pulse processor part which prevents premature switch-on of the colour. A counter provides colour ON delay of 2 or 3 vertical periods after identification of the SECAM signal. Colour is switched off immediately the identification voltage disappears, or 1 vertical period later

Demodulator part

- Two quadrature demodulators with external reference tuned circuits
- Internal filtering of residual carrier in the demodulated colour difference signals
- De-emphasis circuit and colour switching stages in front of the output stages. The colour switching stages are controlled by the pulse processing part
- (B-Y) and (R-Y) colour difference output stages are low resistance n-p-n emitter followers

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	60 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 400 mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
—(R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V
—(B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	min.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

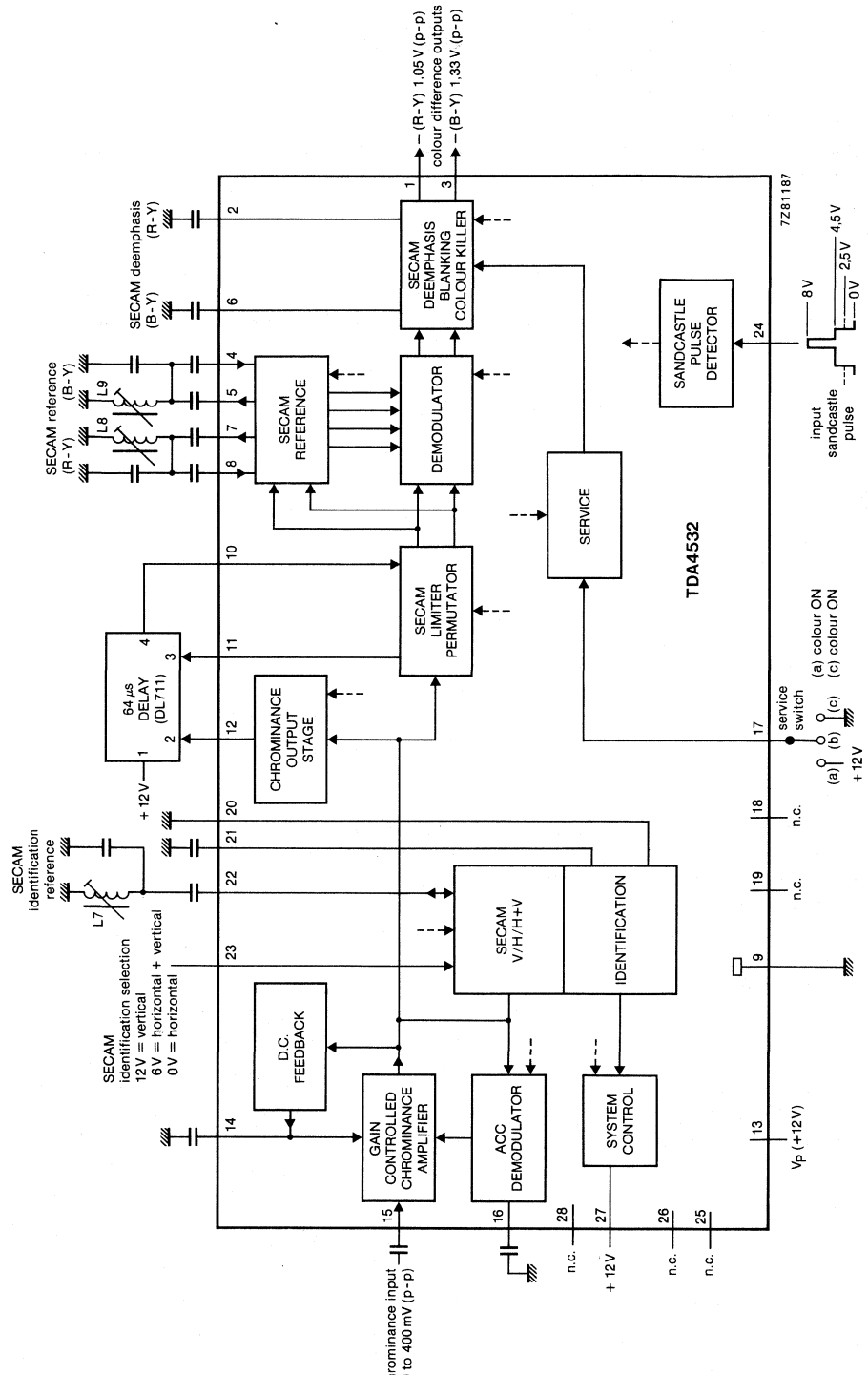


Fig. 1 Block diagram.

n.c. = not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 27 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	60	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	400	mV
input impedance	$\lvert Z_{15-9}\rvert$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12-9}\rvert$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part					
Colour difference output signals (note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
–(R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05*	–	V
–(B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33*	–	V
Ratio of colour difference output signals –(R-Y)/–(B-Y)	$V_{1/3-9}$	0,71*	0,79*	0,87*	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,\ 3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,\ 3-9(p-p)}$	–	20	30	mV
H/2 ripple at –(R-Y) –(B-Y) outputs (peak-to-peak value) with f_o signals	$V_{1,\ 3-9(p-p)}$	–	–	30	mV
D.C. output voltage	$V_{1,\ 3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only) with temperature	$\Delta V/\Delta T$	–	0,5*	0,6*	mV/K
with supply voltage	$\Delta V/\Delta V_P$	–	8,0*	15*	mV/K

* Value measured without influence of external circuitry.

parameter	symbol	min.	typ.	max.	unit
Identification mode switch (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6**	–	V
Colour killer delay time					
colour ON	t_{dC1}	–	–	3	field periods
colour OFF	t_{dC2}	–	–	1	field periods
Service switch					
Switching voltage (pin 17) (for forced colour ON)					
connected to ground	V_{17-9}	–	–	0,5	V
connected to supply voltage	V_{17-9}	6	–	–	V
Sandcastle pulse detector (note 2)					
Input voltage pulse levels (pin 24)					
to separate vertical and horizontal blanking pulses	V_{24-9}	1,3	1,6	1,9	V
required pulse amplitude	V_{24-9}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{24-9}	3,3	3,6	3,9	V
required pulse amplitude	V_{24-9}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{24-9}	6,6	7,1	7,6	V
required pulse amplitude	V_{24-9}	7,7	–	–	V
Input voltage during horizontal scanning	V_{24-9}	–	–	1,1	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference output signals −(R-Y) and −(B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

** Or not connected.

DEVELOPMENT DATA

APPLICATION INFORMATION

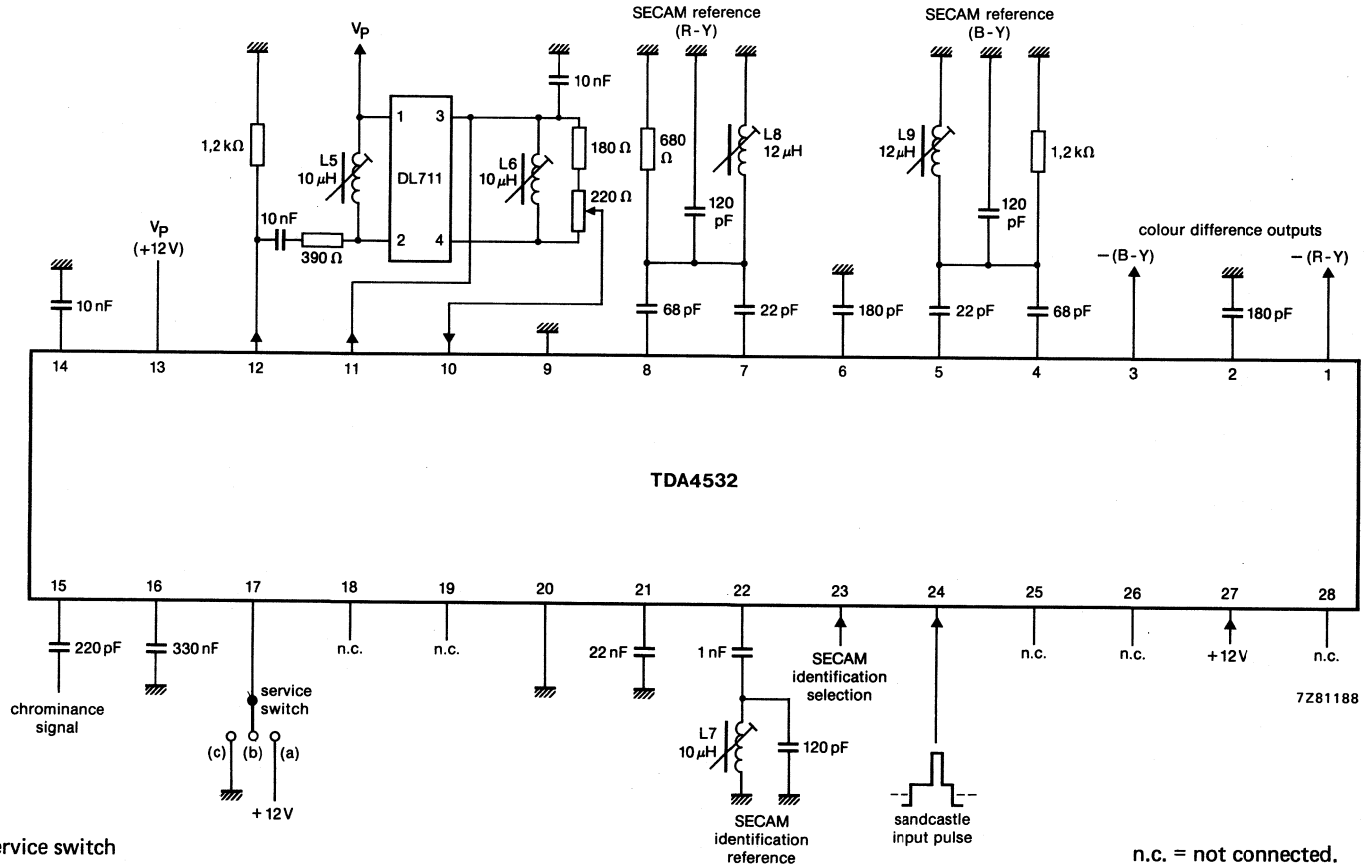


Fig. 2 Application diagram.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4555 and TDA4556 are monolithic integrated multistandard colour decoders for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the colour difference output signals (B-Y) and (R-Y).

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12	V
Supply current (pin 13)	$I_P = I_{13}$	typ.	65	mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 200	mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6	V
Colour difference output signals (peak-to-peak values)				
TDA4555: –(R-Y); **TDA4556:** + (R-Y)	$V_{1-9(p-p)}$	typ.	1,05	V ± 2 dB
TDA4555: –(B-Y); **TDA4556:** + (B-Y)	$V_{3-9(p-p)}$	typ.	1,33	V ± 2 dB
Sandcastle pulse; required amplitude for				
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5	V
horizontal pulse separation	V_{24-9}	typ.	4,5	V
burst gating	V_{24-9}	typ.	7,7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

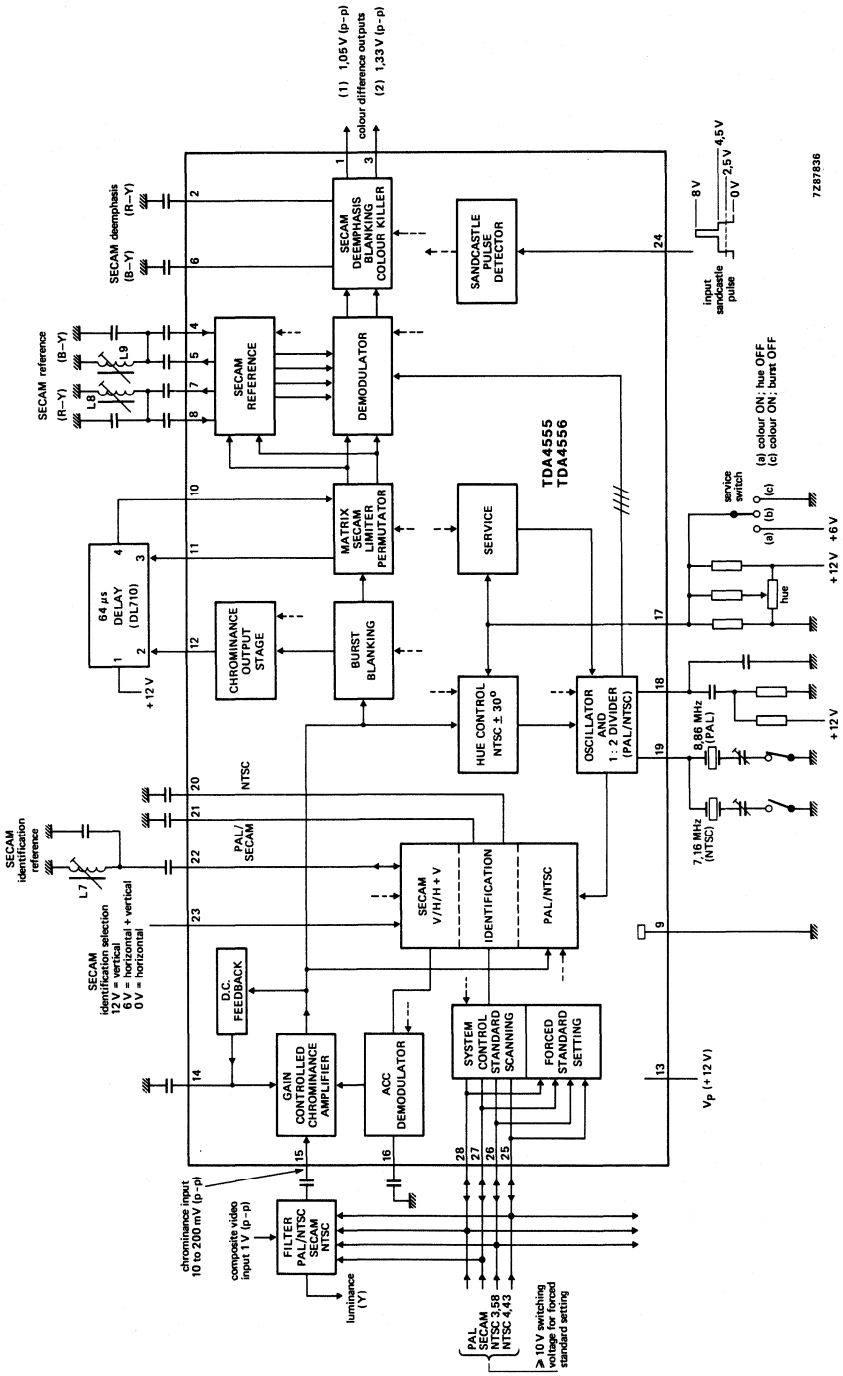


Fig. 1 Block diagram.

(1) TDA4555: −(R-Y); TDA4556: + (R-Y)
(2) TDA4555: −(B-Y); TDA4556: + (B-Y)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	8	mA
Peak value	I_{12M}	max.	15	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	65	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	200	mV
input impedance	$\|Z_{15-9}\|$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
TDA4555					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1-9(p-p)}$	–	–	10	mV
D.C. output voltage n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3-9}$	–	7,7	–	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555					
–(R-Y) signal (pin 1	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T$(R-Y)	–	–0,55	–	mV/K
	$\Delta V/\Delta T$(B-Y)	–	+0,25	–	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	–	30**	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	–	30**	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

** Relative to phase at V_{17-9} = 3 V.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3,58 MHz) at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0,5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28-9}$	–	2,45	–	V
colour ON	$V_{25,26,27,28-9}$	–	5,8	–	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	V_{28-9}	9	–	–	V
SECAM	V_{27-9}	9	–	–	V
NTSC 3,58 MHz	V_{26-9}	9	–	–	V
NTSC 4,43 MHz	V_{25-9}	9	–	–	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1,2	–	2,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3,2	–	4,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	4,0	–	5,0	V
to separate burst gating pulse	$V_{24\text{-}9}$	6,5	–	7,7	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

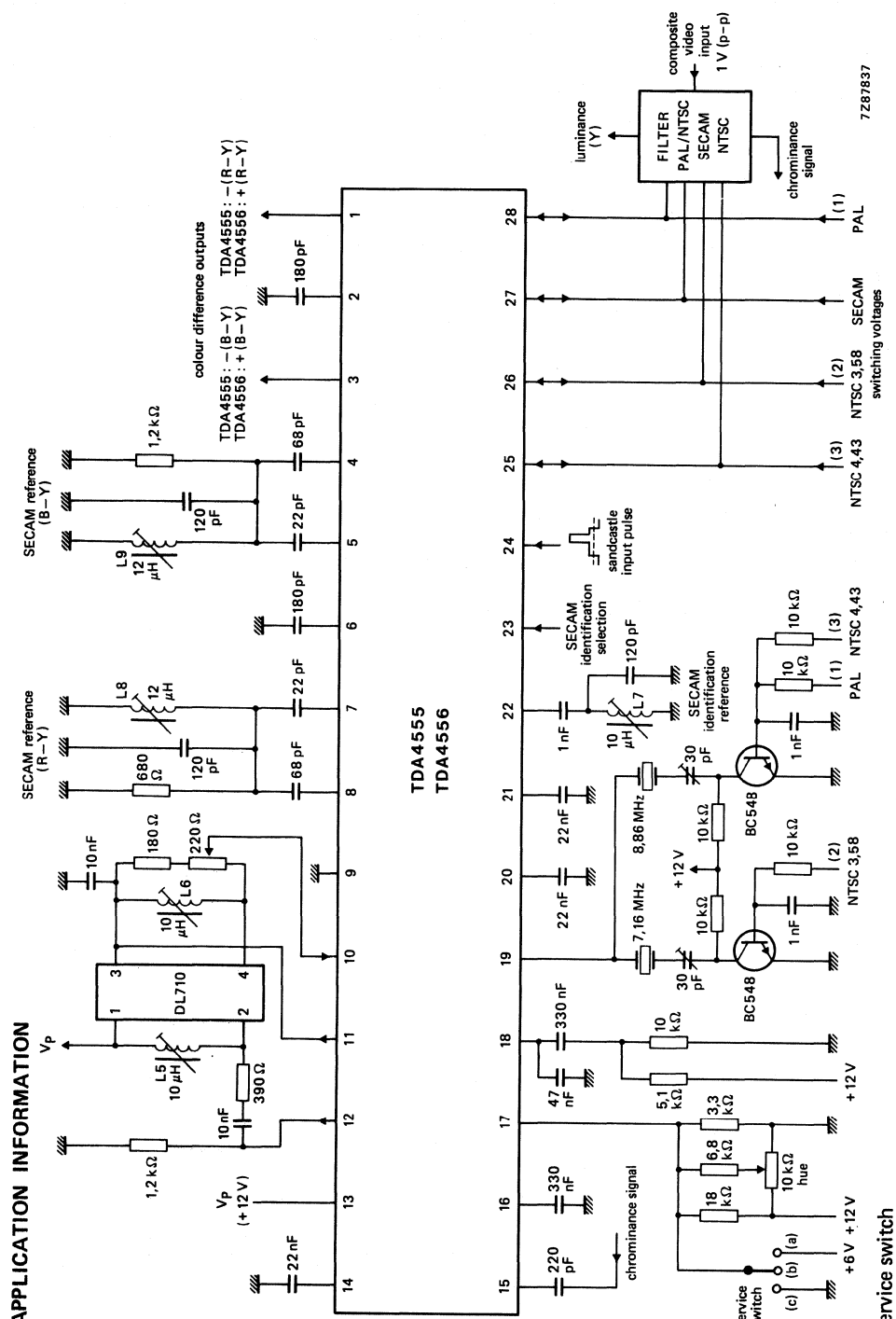


Fig. 2 Application diagram.

Service switch

(a) colour ON; hue OFF
(c) colour ON; burst OFF

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4557 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz standards.

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the demodulators (PAL, NTSC, SECAM)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit and 50/60 Hz recognition
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	10.8	12.0	13.2	V
Supply current (pin 13)	I_P	–	65	–	mA
Chrominance input voltage (peak-to-peak value)	$V_{15(p\text{-}p)}$	20	100	400	mV
Chrominance output voltage (peak-to-peak value)	$V_{12(p\text{-}p)}$	–	1.6	–	V
Colour difference output voltages (peak-to-peak values)					
–(R-Y)	$V_{1(p\text{-}p)}$	–	1.05 V ± 2 dB	–	V
–(B-Y)	$V_{3(p\text{-}p)}$	–	1.33 V ± 2 dB	–	V
Sandcastle pulse (pin 24)					
Required amplitude to separate					
vertical and horizontal pulse	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
horizontal pulse	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
burst gating pulse	$V_{24(p\text{-}p)}$	7.7	–	V_P	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

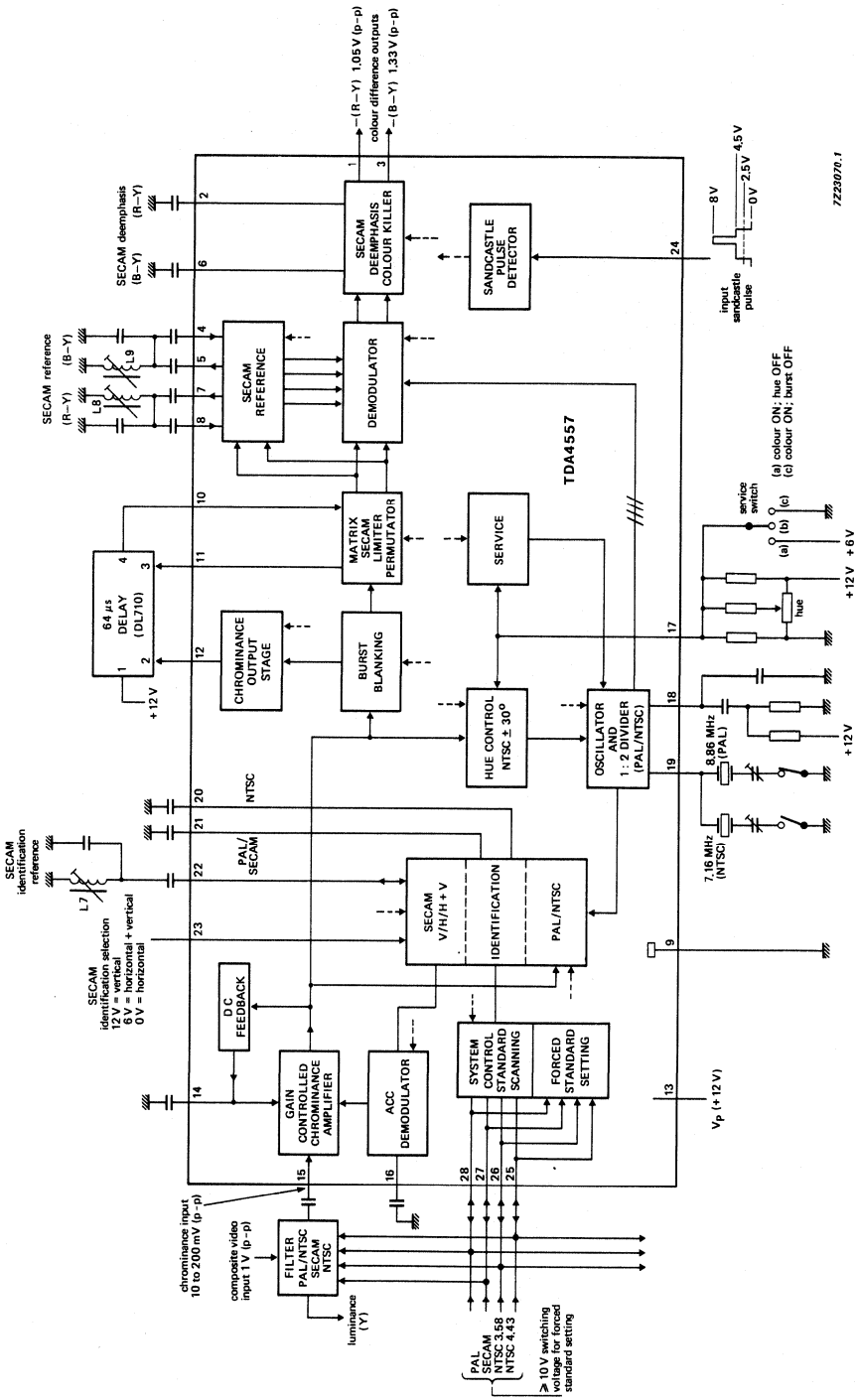


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	V_P	–	13.2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}	0	V_P	V
Current at pin 12	I_{12}	–	8	mA
Peak value	I_{12M}	–	15	mA
Total power dissipation	P_{tot}	–	1.4	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	V_P	10.8	12	13.2	V
Supply current	I_P	50	65	80	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
input impedance	$\|Z_{15-9}\|$	7	10	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12(p-p)}$	1.1	1.6	1.75	V
output impedance (npn emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
DC output voltage	V_{12-9}	7.3	8.2	9.0	V
Input for delayed signal (pin 10)					
DC input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1(p-p)}$	–	–	10	mV
DC output voltage					
npn emitter follower with internal current source of 0.3 mA	$V_{1,3-9}$	7.0	7.7	8.4	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
−(R-Y) signal (pin 1	$V_{1(p-p)}$	−	1.05	−	V
− (B-Y) signal (pin 3)	$V_{3(p-p)}$	−	1.33	−	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	−	0.79* ± 10%	−	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	−	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	−	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3(p-p)}$	−	−	30	mV
DC output voltage	$V_{1,3-9}$	7.0	7.7	8.4	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$	−	0.5	0.6	mV/K
	$\Delta V/\Delta V_P$	−	8	−	mV/V
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	30	40	−	deg
at V_{17-9} = 3 V	ϕ	−	0	−	deg
at V_{17-9} = 4 V	$+\phi$	30	40	−	deg
Input resistance	R_{17-9}	−	5	−	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	0	−	0.5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	−	V_P	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	−	350	−	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	−	−	Hz

* Value measured without influence of external circuitry.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3.58 MHz) at pin 25 (NTSC 4.43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0.5	V
Control voltage ON state during scanning; colour OFF	$V_{25,26,27,28-9}$	2.1	2.45	2.7	V
colour ON	$V_{25,26,27,28-9}$	5.5	5.8	6.2	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON PAL	V_{28-9}	9	–	V_P	V
SECAM	V_{27-9}	9	–	V_P	V
NTSC 3.58 MHz	V_{26-9}	9	–	V_P	V
NTSC 4.43 MHz	V_{25-9}	9	–	V_P	V
Delay time for restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for horizontal identification (H)	V_{23-9}	0	–	2	V
vertical identification (V)	V_{23-9}	10	–	V_P	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3.58 MHz-NTSC 4.43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	V_{24-9}	1.3	1.6	1.9	V
required pulse amplitude	$V_{24(p-p)}$	2.0	2.5	3.0	V
to separate horizontal blanking pulse	V_{24-9}	3.3	3.6	3.9	V
required pulse amplitude	$V_{24(p-p)}$	4.1	4.5	4.9	V
to separate burst gating pulse	V_{24-9}	6.6	7.1	7.6	V
required pulse amplitude	$V_{24(p-p)}$	7.7	–	V_P	V
Input voltage during horizontal scanning	V_{24-9}	–	–	1.0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION

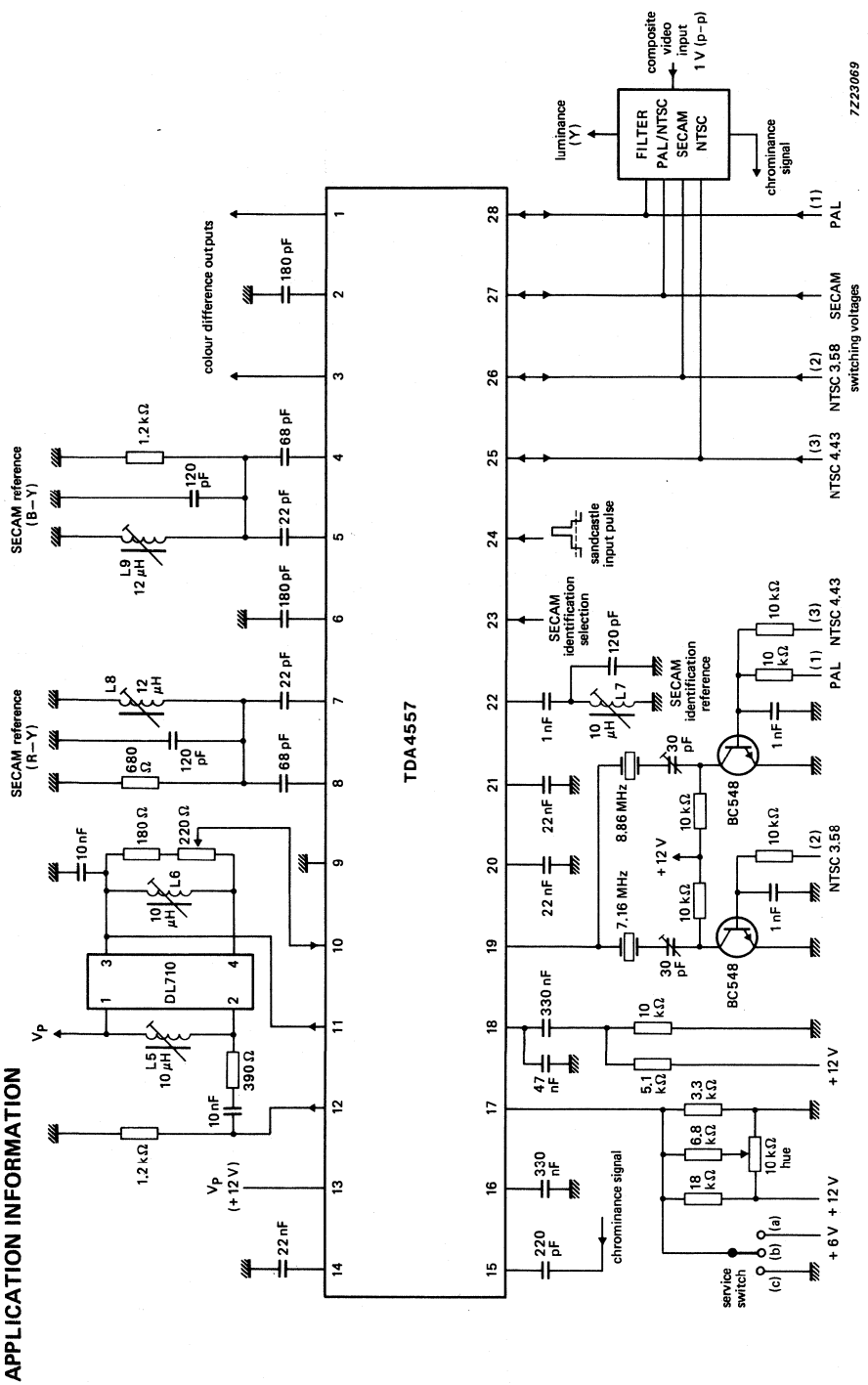


Fig. 2 Application diagram.

Service switch
(a) colour ON; hue OFF
(c) colour ON; burst OFF

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12 V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35 mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0 dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150 ns
Adjustable Y-delay time	t_d		720 to 1035 ns
Y-attenuation	α_y	typ.	7 dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

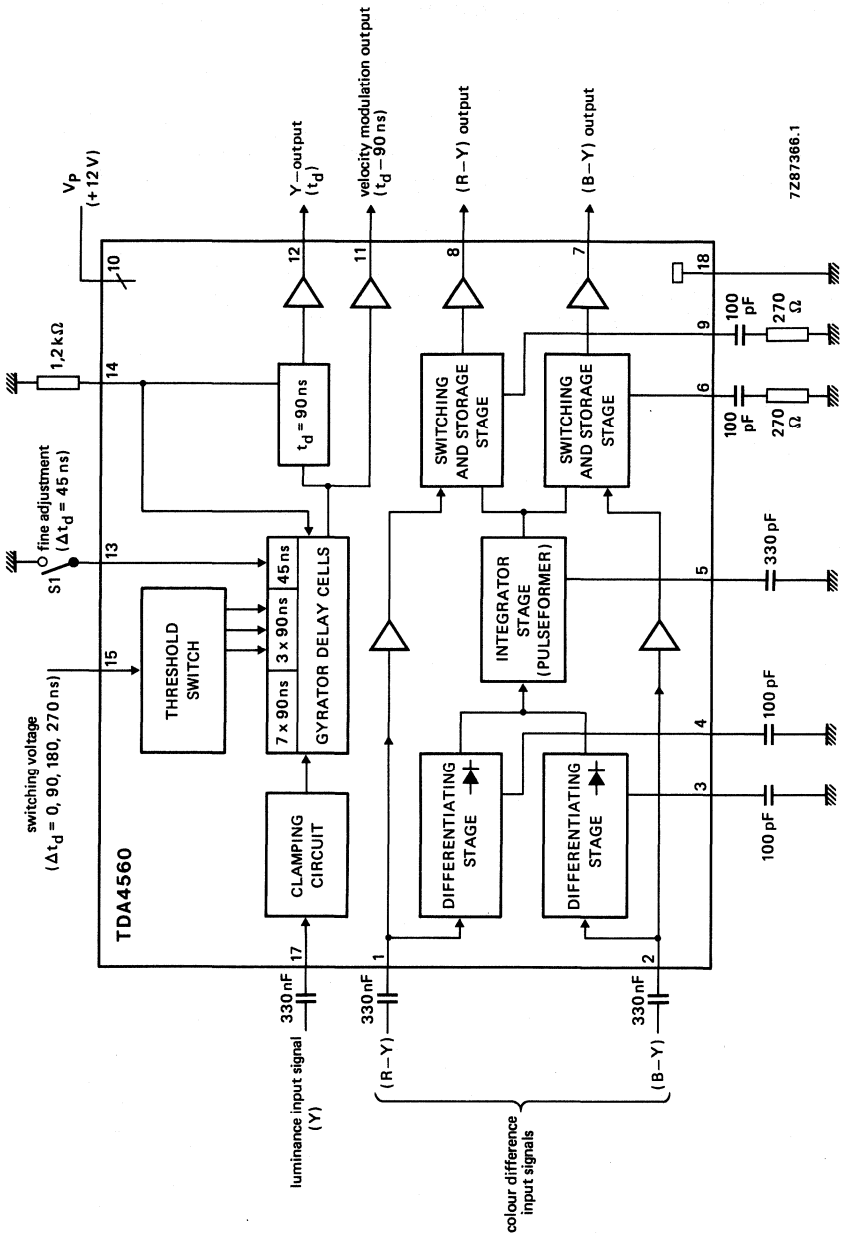


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC)

Supply voltage (pin 10)	$V_P = V_{10-18}$	max. 13,2	V
Voltage ranges to pin 18 (ground)			
at pins 1,2,12,15	V_{n-18}	0 to V_P	V
at pin 11	V_{11-18}	0 to (V_P–3V)	V
at pin 17	V_{17-18}	0 to 7	V
Voltage ranges			
at pin 7 to pin 6	V_{7-6}	0 to 5	V
at pin 8 to pin 9	V_{8-9}	0 to 5	V
Currents			
at pins 6,9	$\pm I_{6,9}$	max. 15	mA
at I_7, I_8, I_{11}, I_{12}		internally limited	
Total power dissipation	P_{tot}	max. 1,1	W
Storage temperature range	T_{stg}	–25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	50	mA
Colour difference channels (pins 1 and 2);					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1,33	–	V
Input resistance	$R_{1,\,2-18}$	–	12	–	kΩ
Internal bias (input)	$V_{1,\,2-18}$	–	4,3	–	V
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output voltage (d.c.)	$V_{7,\,8-18}$	–	4,4	–	V
Output current (emitter follower with constant current source 0,65 mA)	$-I_{7,8}$	–	1,2	–	mA
(R-Y) and B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Internal bias voltage (during clamping)	V_{17-18}	–	1,5	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}$	α_Y	–	8	–	dB
Y-signal attenuation $\frac{V_{12}}{V_{17}}$	α_Y	–	7	–	dB
Output voltage (d.c.)	V_{11-18}	–	2,3	–	V
Output voltage (d.c.)	V_{12-18}	–	10,3	–	V
Output current (emitter follower with constant current source 0,45 mA)	$-I_{11,12}$	–	1,2	–	mA
Frequency response (note 1) $R_{14-18} = 1{,}2$ kΩ; $V_{15-18} = 12$ V	f_{12-17}	–	5	–	MHz

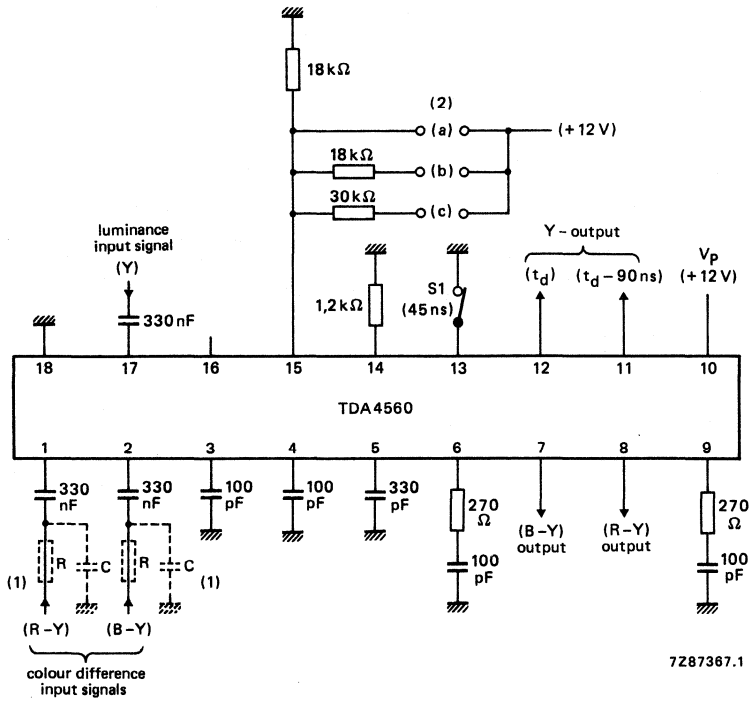
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17)					
Adjustable delay (note 2) (switch open)					
at $V_{15\text{-}18}$ = 0 to 2,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3,5 to 5,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	810	–	ns
at $V_{15\text{-}18}$ = 6,5 to 8,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	900	–	ns
at $V_{15\text{-}18}$ = 9,5 to 12 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at $V_{13\text{-}18}$ = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	–	–	70	K/W

NOTES TO THE CHARACTERISTICS

1. $R_{14\text{-}18}$ influences the bandwidth.
2. Delay time is proportional to resistor $R_{14\text{-}18}$.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
O	O	O	0 to 2,5 V	720
O	O	X	3,5 to 5,5 V	810
O	X	X	6,5 to 8,5 V	900
X	X	X	9,5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4565 is a monolithic integrated circuit for coulour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 730 ns to 1000 ns in steps of 90 ns and additional fine adjustment of 50 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	760	820	880	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	850	910	970	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	940	1000	1060	ns
Y-signal attenuation	0.5 MHz	α_Y	0	6.5	8.0	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

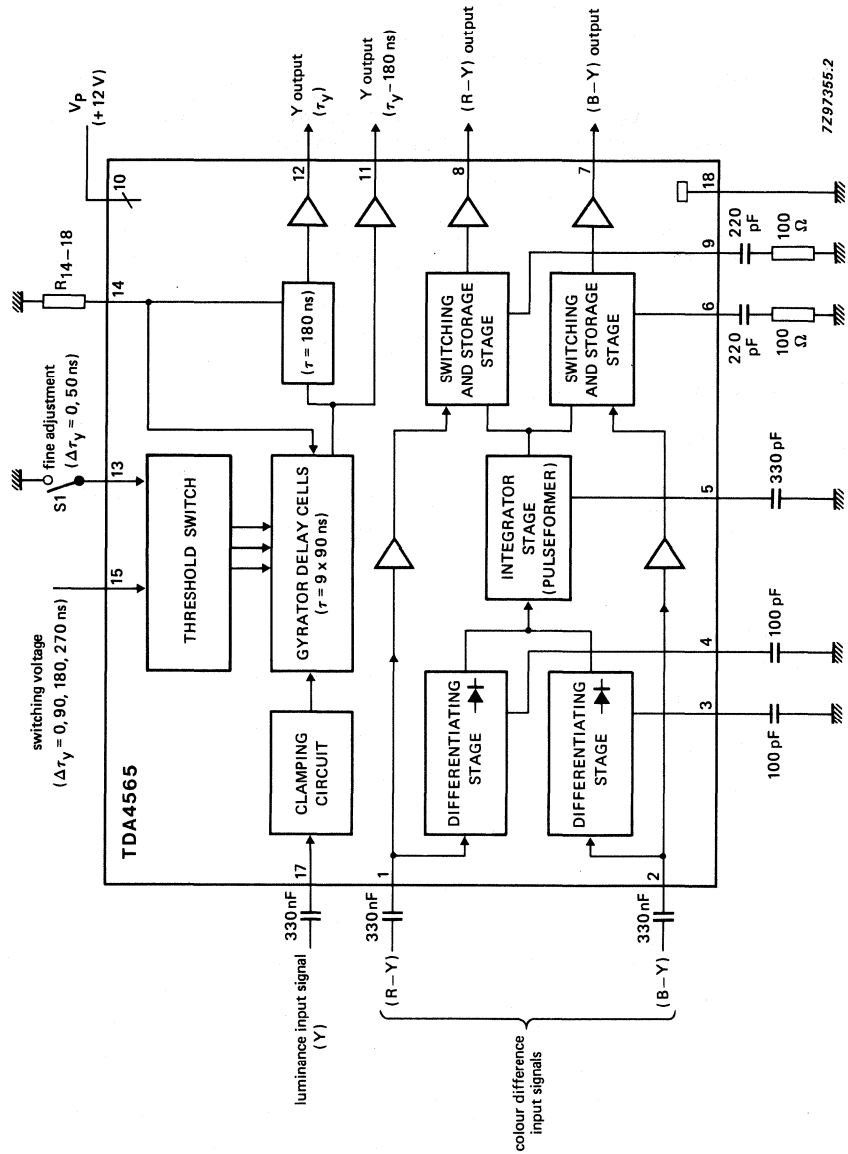


Fig.1 Block diagram.

DEVELOPMENT DATA

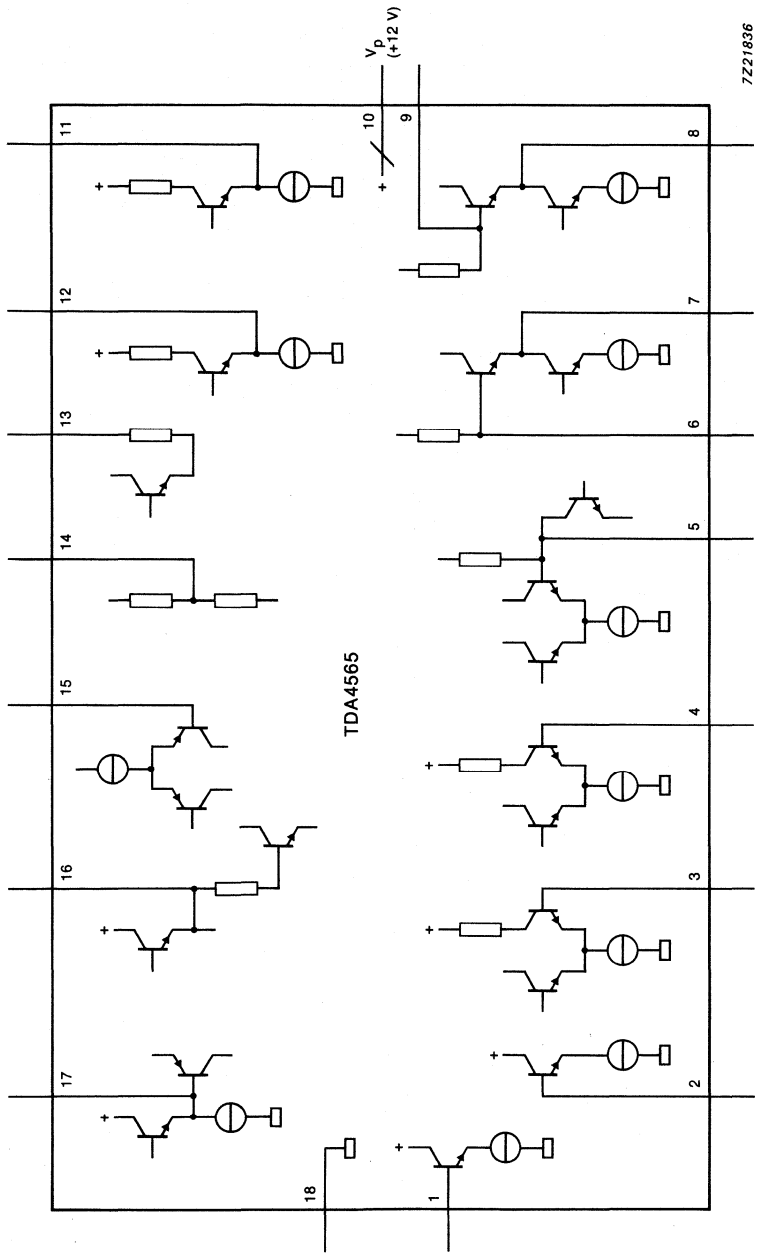


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	V_{n-18}	0	V_p	V
at pin 11	V_{11-18}	0	$(V_p - 3\ V)$	V
at pin 17	V_{17-18}	0	7	V
Voltage ranges				
at pin 7 to pin 6	V_{7-6}	0	5	V
at pin 8 to pin 9	V_{8-9}	0	5	V
Currents				
at pins 6, 9	$I_{6, 9}$	−10	+10	mA
at pins 7, 8, 11 and 12	$I_{7, 8, 11, 12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	−	1.1	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	1.05	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	1.33	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+1	dB
(B-Y)		V_7/V_2	−1	0	+1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	1	1.4	V
Internal bias voltage	during clamping	V_{17-18}	1.3	1.5	1.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4)					
at V_{15-18} = 0 to 2.5 V		t_{17-18}	670	730	790	ns
at V_{15-18} = 3.5 to 5.5 V		t_{17-18}	760	820	880	ns
at V_{15-18} = 6.5 to 8.5 V		t_{17-18}	850	910	970	ns
at V_{15-18} = 9.5 to 12 V		t_{17-18}	940	1000	1060	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	30	50	70	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12}.\Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12}.\Delta V_p}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	5.0	6.5	8.0	dB
pin 12 from pin 17		V_{12}/V_{17}	5.0	6.5	8.0	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	–3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz}{V_{12}\ (0.5\ MHz)}$	–3.0	–	2.0	dB

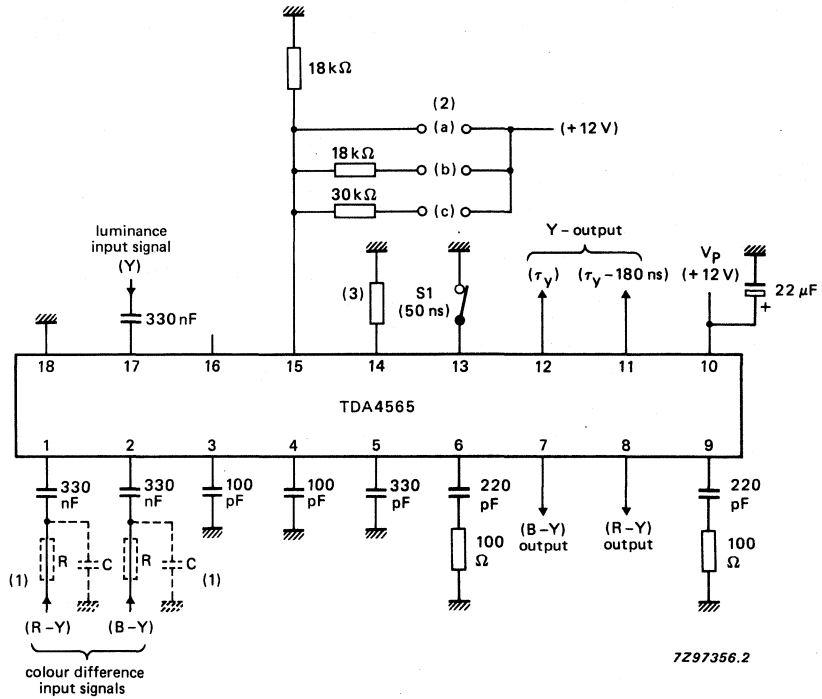
parameter	conditions	symbol	min.	typ.	max.	unit
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\,12}$	–	–	0.4	mA
sink		$-I_{11,\,12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4565
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4565A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	730
0	0	X	3.5 to 5.5 V	820
0	X	X	6.5 to 8.5 V	910
X	X	X	9.5 to 12 V	1000

Where: X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 50 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+ 1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

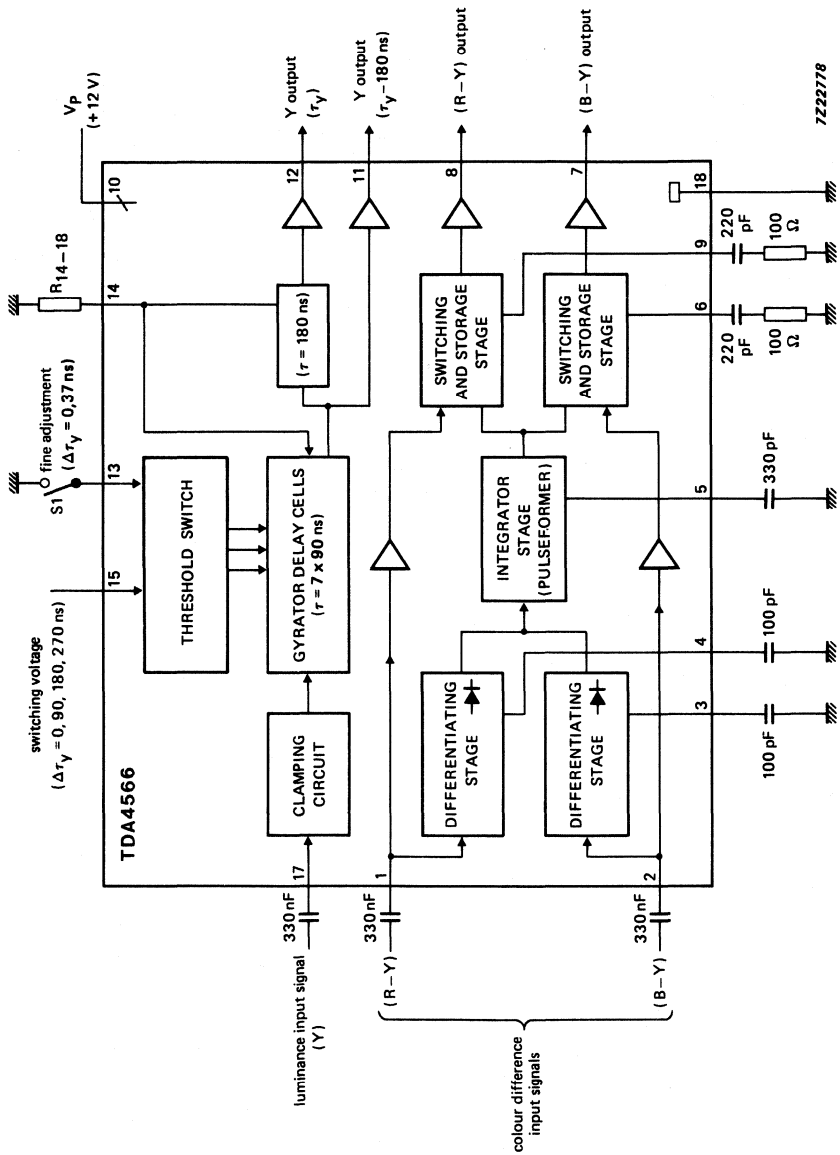


Fig.1 Block diagram.

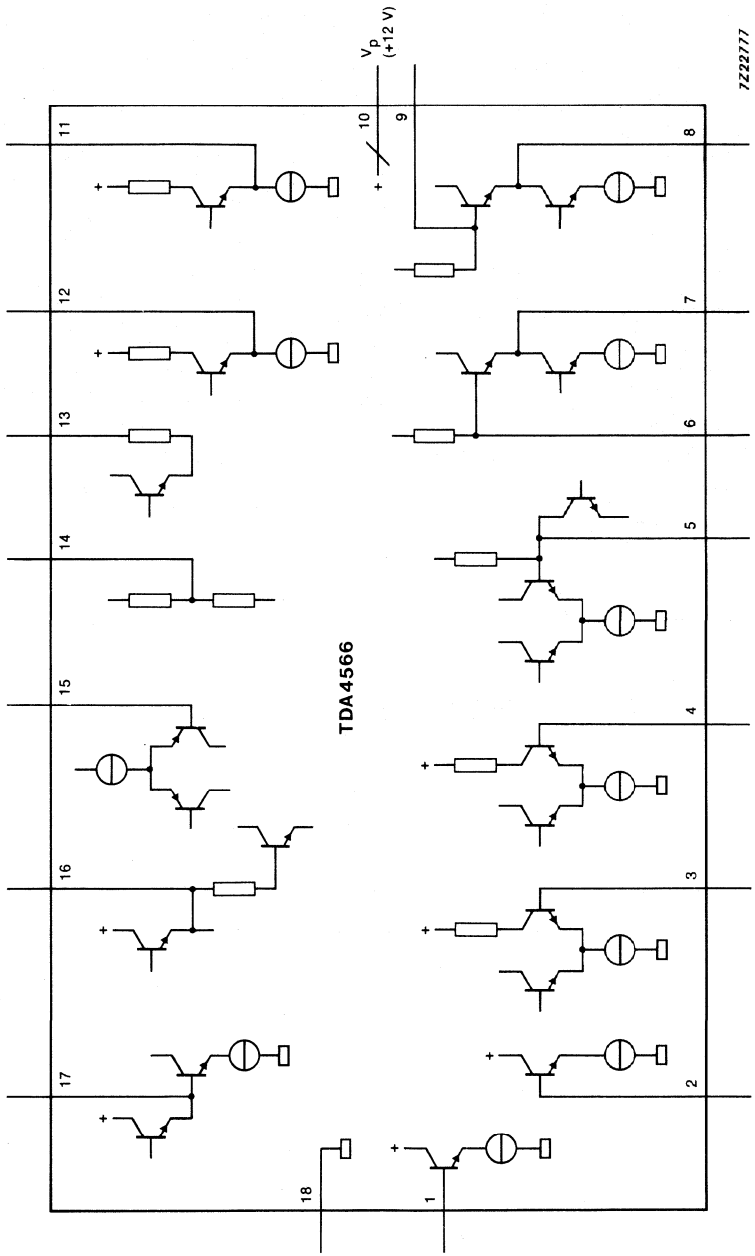


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	V_{n-18}	0	V_P	V
at pin 11	V_{11-18}	0	(V_P–3 V)	V
at pin 17	V_{17-18}	0	7	V
Voltage ranges				
at pin 7 to pin 6	V_{7-6}	0	5	V
at pin 8 to pin 9	V_{8-9}	0	5	V
Currents				
at pins 6, 9	$I_{6,9}$	–10	+ 10	mA
at pins 7, 8, 11 and 12	$I_{7,8,11,12}$		internally limited	
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	0.63	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+ 1	dB
(B-Y)		V_7/V_2	−1	0	+ 1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

CHARACTERISTICS (continued)

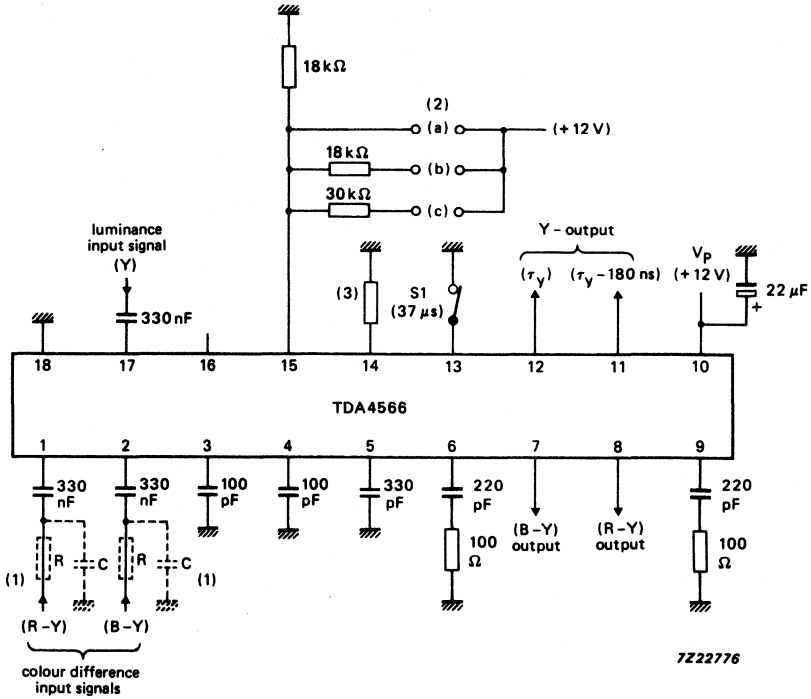
parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p\text{-}p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	$V_{17\text{-}18}$	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4					
at $V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}18}$	490	550	610	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}18}$	580	640	700	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}18}$	670	730	790	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}18}$	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	$t_{17\text{-}12}$	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	$t_{11\text{-}12}$	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4566.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4566A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

LUMINANCE SIGNAL DELAY CIRCUIT

GENERAL DESCRIPTION

The TDA4568 is an integrated circuit that provides the luminance signal delay in colour television receivers.

Features

- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	22	–	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

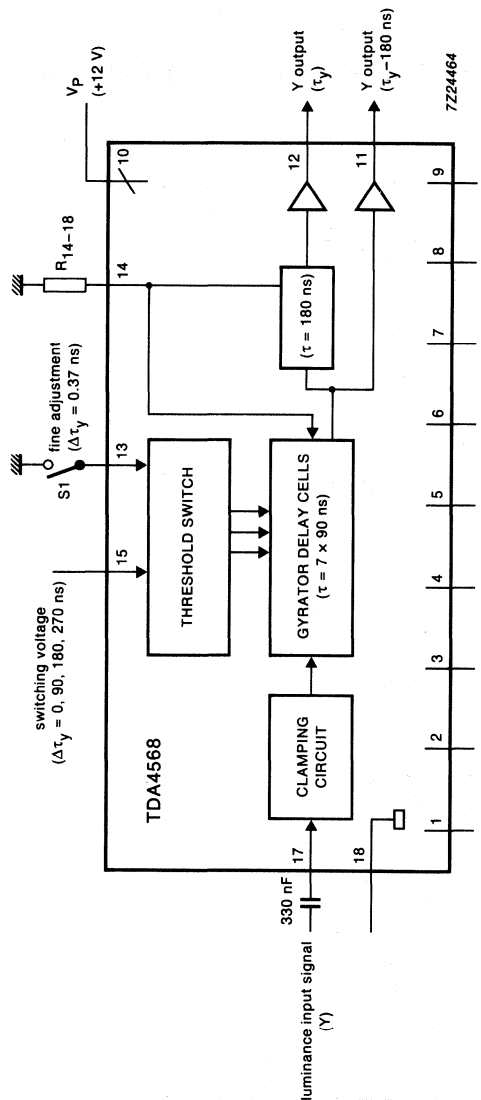


Fig.1 Block diagram.

DEVELOPMENT DATA

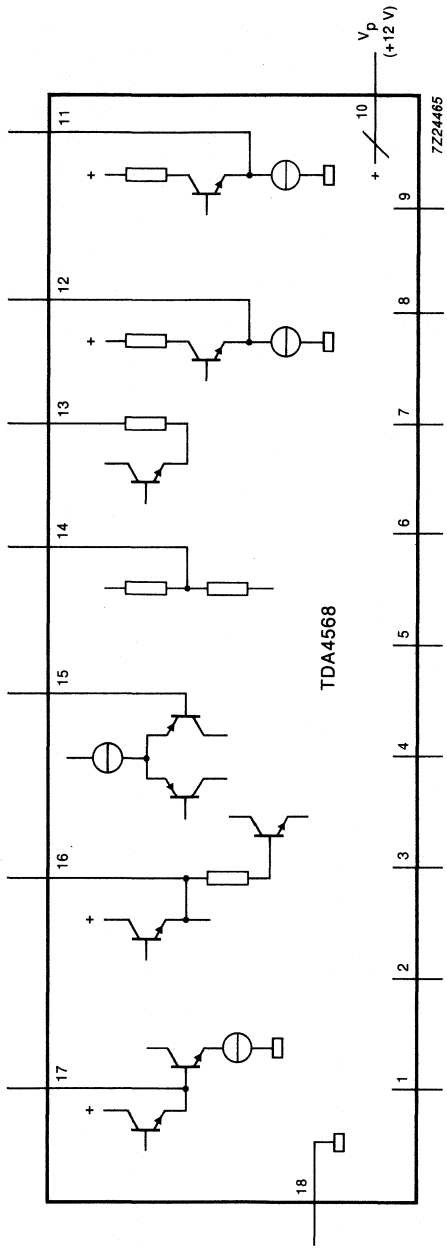


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pin 15	V_{15-18}	0	V_P	V
at pin 17	V_{17-18}	0	7	V
Current range at pins 11 and 12	$I_{11, 12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 70 K/W

Note

Pins 13 and 14, DC potential not published.

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	22	–	mA
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	V_{17-18}	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; $R_{14} = 1.2$ kΩ; notes 1 and 2					
at $V_{15-18} = 0$ to 2.5 V		t_{17-18}	490	550	610	ns
at $V_{15-18} = 3.5$ to 5.5 V		t_{17-18}	580	640	700	ns
at $V_{15-18} = 6.5$ to 8.5 V		t_{17-18}	670	730	790	ns
at $V_{15-18} = 9.5$ to 12 V		t_{17-18}	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

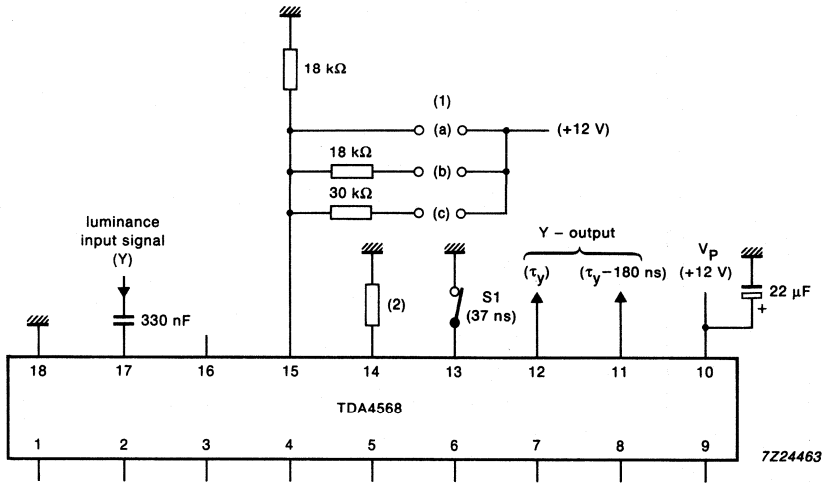
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 4					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
2. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18}$ = 1.2 kΩ.
3. Frequency response measured with $V_{15\text{-}18}$ = 9.5 V and switch S1 open.
4. Output current measured with emitter follower with constant current source of 0.6 mA.

APPLICATION INFORMATION



DEVELOPMENT DATA

(1) Switching sequence for delay times shown in Table 1.
(2) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4568.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4568A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

NTSC DECODER

GENERAL DESCRIPTION

The TDA4570 is an integrated 3,58 MHz or 4,43 MHz NTSC decoder. It is pin sequence compatible with multi-standard decoder TDA4555 and pin compatible with the PAL decoder TDA4510.

Features:

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with sampled rectification during burst-key signal
- Blanking circuit for the colour burst signal

Oscillator and control voltage part

- Voltage controlled reference oscillator for double subcarrier frequency
- Divider stages which provide the correct 90° phase between −(R-Y) and −(B-Y) reference signals for the demodulators
- Phase comparator which controls the frequency and phase of the reference oscillator and compares the (R-Y) reference with the burst pulse
- HUE control stage provides phase shifting via the combined service and hue control input (pin 11)
- Identification demodulator provides a positive-going identification signal at pin 14 for NTSC signals and acts as the automatic colour killer
- Two-function service switch:

  position one ($V_{14-3} < 1$ V): switches the colour-ON and switches the hue control and burst for the PLL oscillator-OFF, allowing the adjustment of the reference oscillator

  position two ($V_{14-3} > 5$ V): switches the colour-ON, the hue control OFF and allows the output signal to be observed
- Sandcastle pulse detector for burst-gate, horizontal and horizontal/vertical blanking pulse detection. The vertical part of the sandcastle pulse is used for the internal colour-ON and colour-OFF delay
- Pulse processing part for the prevention of premature switching ON of the colour. The colour-ON delay, two or three field periods after identification of the NTSC signal, is achieved by a counter. When there is no identification voltage present the colour is switched OFF immediately or, at the most, one field period later.

Demodulator part

- Two synchronous demodulators for the (R-Y) and (B-Y) signals, which incorporate stages for the blanking during line and field flyback
- Internal filtering of the residual carrier in the demodulated colour difference signals
- Colour switching stages controlled by the pulse processing part in front of the output stages
- The output stages for (R-Y) and (B-Y) signals are low resistance n-p-n emitter followers
- Separate colour switching output

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

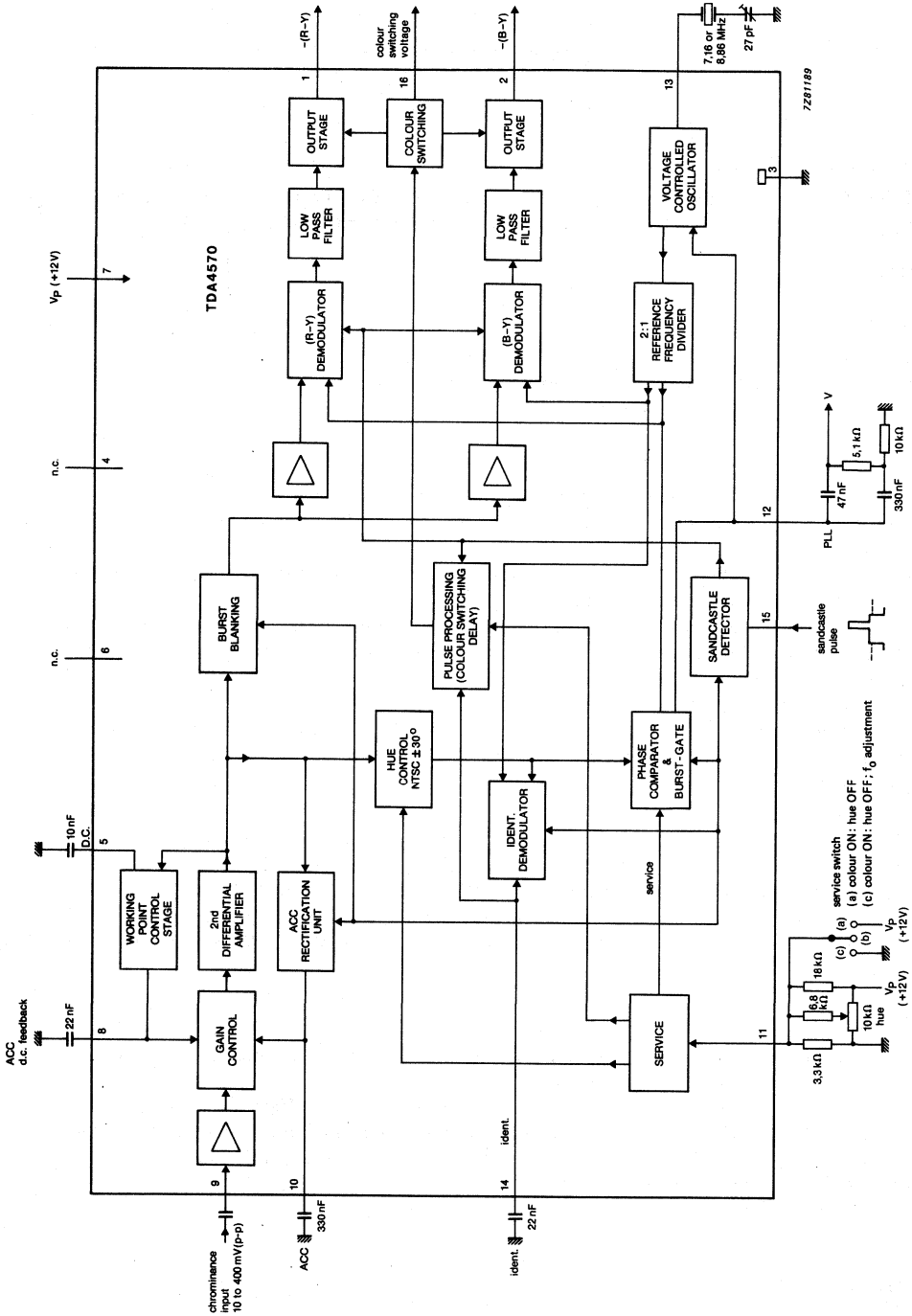


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents at:				
pins 1 and 2	$-I_{1,2}$	max.	5	mA
pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to + 150		°C
Operating ambient temperature range	T_{amb}	0 to + 70		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	max.	80	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	$I_P = I_7$	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9-3(p-p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9-3(p-p)}$	–	100	–	mV
Input impedance	$\lvert Z_{9-3}\rvert$	–	3,3	–	kΩ
Input capacitance	C_{9-3}	–	4,0	–	pF
Oscillator and control voltage part					
Oscillator frequency for subcarrier frequency					
3,58 MHz	f_{osc}	–	7,16	–	MHz
4,43 MHz	f_{osc}	–	8,86	–	MHz
Input resistance	R_{13-3}	–	350	–	Ω
Catching range (depending on RC network between pins 12 and 3)	Δf	± 300	–	–	Hz
Control voltage					
without burst signal	V_{14-3}	–	6,0	–	V
colour switching threshold	V_{14-3}	–	6,6	–	V
hysteresis of colour switching	V_{14-3}	–	150	–	mV
Colour-ON delay	$t_{d\ on}$	–	–	3	*
Colour-OFF delay	$t_{d\ off}$	–	–	1	*

* Expressed as field periods.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Colour switching output (open n-p-n emitter)					
output current	$-I_{16}$	–	–	5,0	mA
colour-ON voltage	V_{16-3}	–	6,0	–	V
colour-OFF voltage	V_{16-3}	–	0	–	V
HUE control and service switches					
Phase shift of reference carrier relative to the input signal V_{11-3} = 3 V	ϕ	–5	0	+ 5	deg
Phase shift of reference carrier relative to phase at V_{11-3} = 3 V					
V_{11-3} = 2 V	$-\phi$	30	–	–	deg
V_{11-3} = 4 V	$+\phi$	30	–	–	deg
Internal source (open pin)		–	3	–	V
First service position (PLL is inactive for oscillator adjustment, colour ON, HUE OFF)	V_{11-3}	0	–	1	V
Second service position (colour ON, HUE OFF)	V_{11-3}	5	–	V_P	V
Demodulator part					
Colour difference signals output voltage (peak-to-peak value)					
–(R-Y) signal	$V_{1-3(p-p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2-3(p-p)}$	1,06	1,33	1,67	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{1-3}}{V_{2-3}}$	0,71	0,79	0,87	
D.C. voltage at colour difference outputs	$V_{1,\,2-3}$	–	7,7	–	V
Residual carrier at colour difference outputs (peak-to-peak value)					
(1 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	20	mV
(2 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	30	mV

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (note 1)					
Input voltage level (pin 15)					
to separate vertical and horizontal blanking pulses	V_{15-3}	1,3	1,6	1,9	V
required pulse amplitude	V_{15-3}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{15-3}	3,3	3,6	3,9	V
required pulse amplitude	V_{15-3}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{15-3}	6,6	7,1	7,6	V
required pulse amplitude	V_{15-3}	7,7	–	–	V
Input voltage during horizontal scanning	V_{15-3}	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

Note

1. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

DEVELOPMENT DATA

APPLICATION INFORMATION

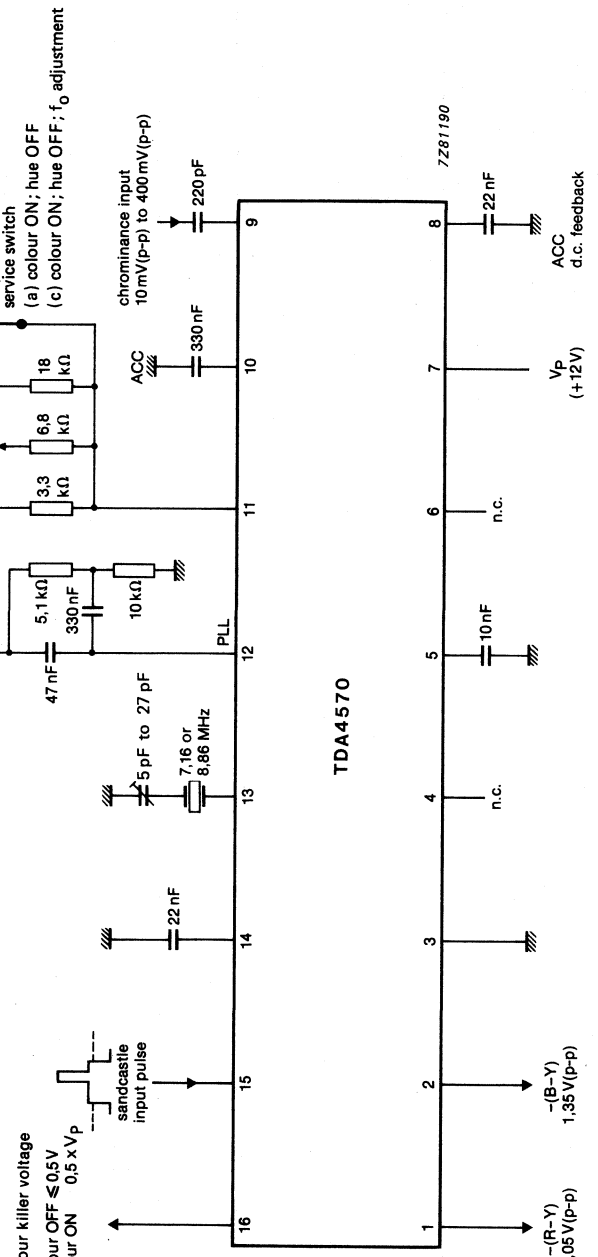


Fig. 2 Application diagram.

Crystal frequency 7, 16 or 8,86 MHz; resonance resistance 60 Ω; load capacitance 20 pF; dynamic capacitance 22 fF and static capacitance 5,5 pF.

VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

GENERAL DESCRIPTION

The TDA4580 is a monolithic integrated circuit which performs video control functions in television receivers with a colour difference interface. For example it operates in conjunction the multistandard colour decoder TDA4555. The required input signals are: luminance and negative colour difference −(R-Y) and −(B-Y), and a 3-level sandcastle pulse for control purposes. Analogue RGB signals can be inserted from two sources. One with full performance adjustment possibilities. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference, luminance and RGB input signals with black level clamping
- Two sets of analogue RGB inputs via fast switch 1 and fast switch 2
- First RGB inputs and fast switch 1 in accordance with peritelevision connector specification
- Saturation, contrast and brightness control acting on first RGB inputs
- Brightness control acting on second RGB inputs
- Equal black levels for television and inserted signals
- Clamping, horizontal and vertical blanking, and timing of automatic cut-off, controlled by a 3-level sandcastle pulse
- Automatic cut-off control with compensation for leakage current of the picture tube
- Measuring pulses of cut-off control start immediately after end of vertical part of sandcastle pulse
- Three selectable blanking intervals for PAL, SECAM and NTSC/PAL-M
- Two switch-on delays for run-in without discolouration
- Adjustable peak drive limiter
- Average beam current limiter
- G-Y and RGB matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- Bandwidth 10 MHz (typ.)
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

Supply voltage (pin 6)	$V_P = V_{6-24}$	typ.	12 V
Supply current (pin 6)	$I_P = I_6$	typ.	110 mA
Luminance input (pin 15)			
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (black to white values)	$V_{14, 13, 12-24}$	typ.	0,7 V
Inserted RGB signals for teletext use (black to white values)	$V_{23, 22, 21-24}$	typ.	1 V
Three-level sandcastle pulse (required input voltage)	V_{10-24}	typ.	2,5/4,5/8,0 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

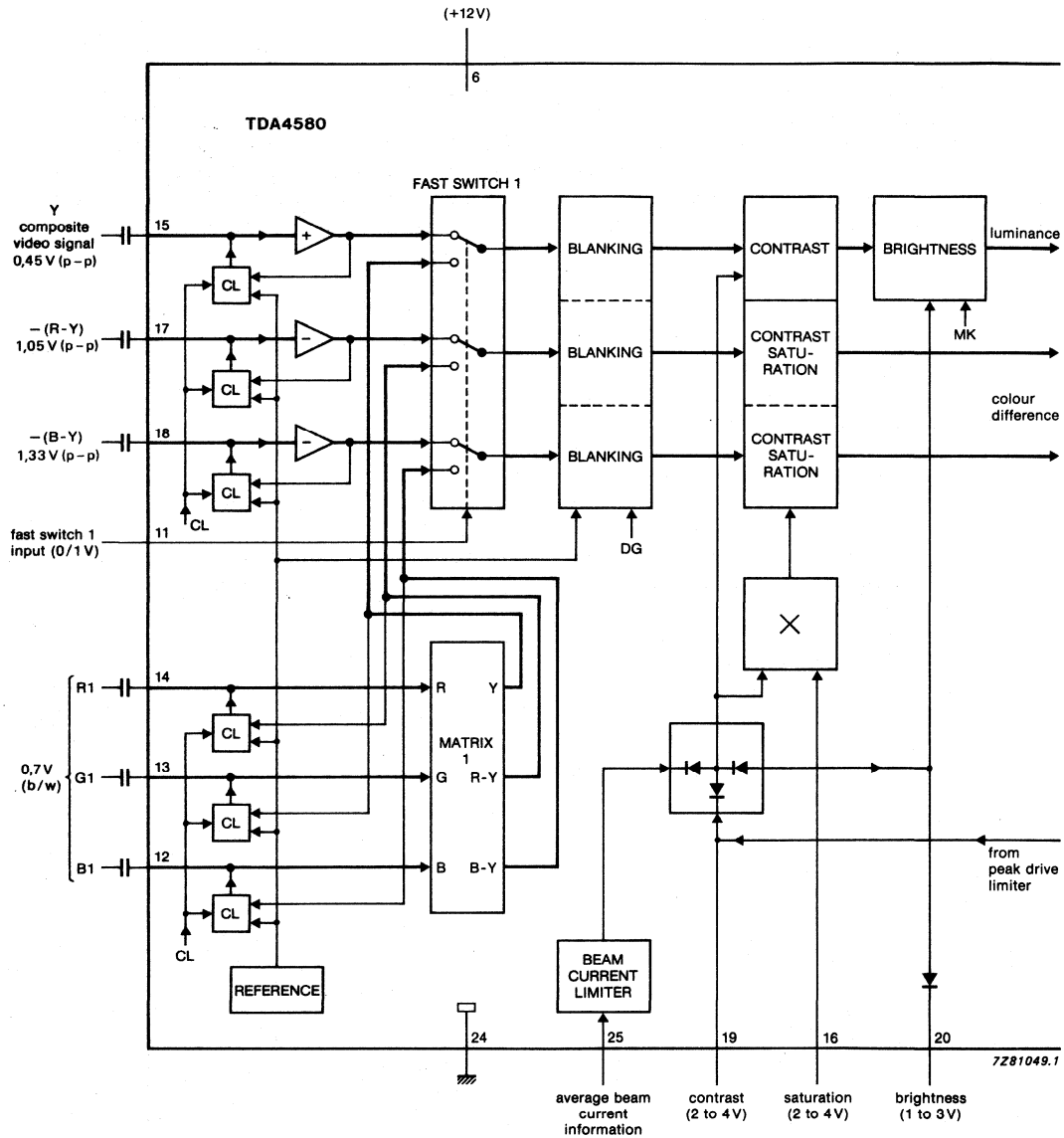


Fig. 1a Part of block diagram; continued in Fig. 1b.

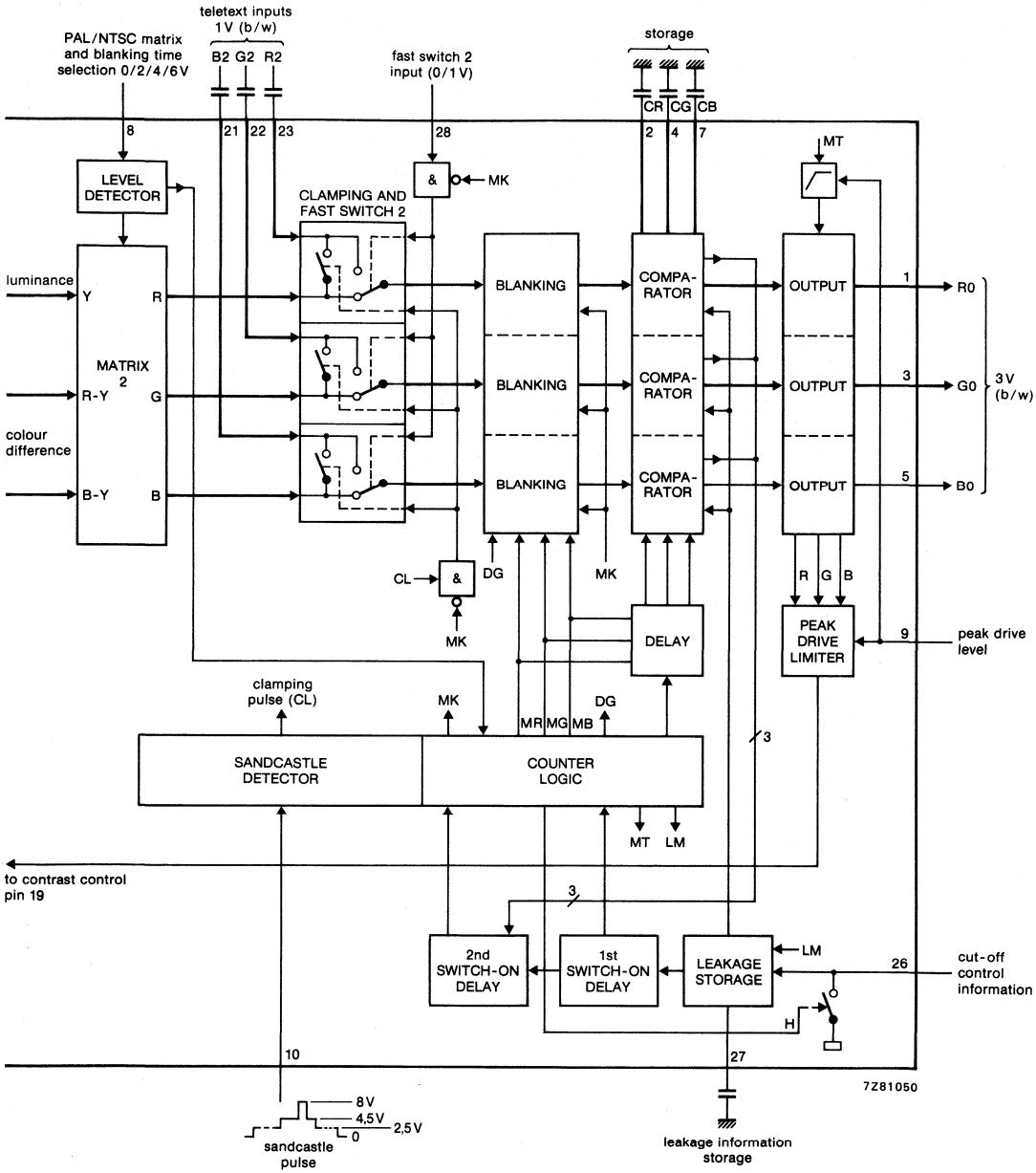


Fig. 1b Part of block diagram; continued from Fig. 1a.

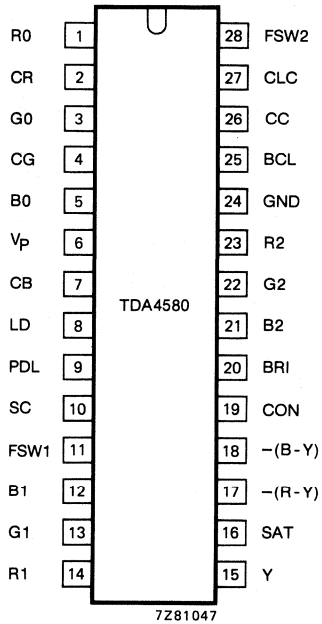


Fig. 2 Pinning diagram.

PINNING

pin no.	mnemonic	description
1	R0	Red output
2	CR	Red storage capacitor for cut-off control
3	G0	Green output
4	CG	Green storage capacitor for cut-off control
5	B0	Blue output
6	V_P	Positive supply voltage (+ 12 V)
7	CB	Blue storage capacitor for cut-off control
8	LD	PAL/NTSC matrix and blanking time level detector input
9	PDL	Peak drive limiting input
10	SC	Sandcastle pulse input
11	FSW1	Fast switch 1 for Y, CD and RGB inputs
12	B1	Blue input (external signal)
13	G1	Green input (external signal)
14	R1	Red input (external signal)
15	Y	Luminance input
16	SAT	Saturation control input
17	−(R-Y)	Colour difference input −(R-Y)
18	−(B-Y)	Colour difference input −(B-Y)
19	CON	Contrast control input
20	BRI	Brightness control input
21	B2	Teletext blue input
22	G2	Teletext green input
23	R2	Teletext red input
24	GND	Ground
25	BCL	Average beam current limiting input
26	CC	Automatic cut-off control input
27	CLC	Storage capacitor for leakage current
28	FSW2	Fast switch 2 for teletext inputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 6)	$V_P = V_{6-24}$		0 to 13,2	V
Voltage range at pins 2, 4, 7, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 25, 27 to pin 24 (ground)	V_{n-24}		0 to V_P	V
Voltages ranges				
at pins 8, 11, 28	$V_{8, 11, 28-24}$		$-0,5$ to V_P	V
at pin 10	V_{10-24}		0 to $V_P + 0,7$	V
at pin 26	V_{26-24}		$-0,7$ to $V_P + 0,7$	V
Currents				
at pins 1, 3, 5 (average)	$-I_{1, 3, 5(AV)}$	max.	3	mA
at pins 1, 3, 5 (peak)	$-I_{1, 3, 5(M)}$	max.	10	mA
at pin 19 (average)	$I_{19(AV)}$	max.	5	mA
at pin 26	I_{26}	max.	1	mA
Total power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		-20 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	37	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in a circuit similar to Fig. 4 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to pin 24 (ground) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage range	$V_P = V_{6-24}$	10,8	–	13,2	V
Supply current	$I_P = I_6$	–	110	–	mA
Colour difference inputs (pins 17 and 18)					
–(R-Y) input signal at pin 17 (notes 1 and 2) (peak-to-peak value)	$V_{17-24(p-p)}$	–	1,05	–	V
–(B-Y) input signal at pin 18 (notes 1 and 2) (peak-to-peak value)	$V_{18-24(p-p)}$	–	1,33	–	V
Input current during scanning	$\|I_{17,\ 18}\|$	–	–	0,3	μA
Input resistance	$R_{17,\ 18}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{17,\ 18-24}$	–	7,5	–	V
Luminance input (pin 15; note 2)					
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	–	0,45	–	V
Input current during scanning	$\|I_{15}\|$	–	–	0,3	μA
Input resistance	R_{15}	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	V_{15-24}	–	7,4	–	V
Signal switch 1 input (pin 11)					
Input voltage level for insertion of Y and CD signals	V_{11-24}	–	–	0,4	V
RGB1 signals	V_{11-24}	0,9	–	3,0	V
Internal resistor to ground	R_{11}	–	10	–	kΩ
RGB1 inputs (R1 pin 14, G1 pin 13, B1 pin 12; note 2) (signals controlled by saturation, contrast and brightness)					
Input signal (black to white value)	$V_{12,\ 13,\ 14-24}$	–	0,7	–	V
Input current during scanning	$\|I_{12,\ 13,\ 14}\|$	–	–	0,3	μA
Input resistance	$R_{12,\ 13,\ 14}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{12,\ 13,\ 14-24}$	–	8,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB/Y, (R-Y), (B-Y) – Matrix					
Matrixed according to the equations $V_{(R-Y)} = 0{,}7\ V_R - 0{,}59\ V_G - 0{,}11\ V_B$ $V_{(B-Y)} = -0{,}3\ V_R - 0{,}59\ V_G + 0{,}89\ V_B$ $V_{(Y)} = 0{,}3\ V_R + 0{,}59\ V_G + 0{,}11\ V_B$					
Contrast control input (pin 19; note 3) (contrast control acts on Y and CD signals or RGB1 signals respectively)					
Maximum contrast	V_{19-24}	–	4	–	V
Nominal contrast (6 dB below max.)	V_{19-24}	–	3	–	V
Attenuation of contrast at V_{19-24} = 2 V (related to max.)		–	22	–	dB
Input current at V_{19-24} = 2 to 4 V	$-I_{19}$	–	–	3	μA
Peak drive limiting input (pin 9; note 4)					
Internal d.c. bias voltage	V_{9-24}	–	9	–	V
Input resistance at $V_{9-24} > 9$ V	R_9	–	10	–	kΩ
Control current into contrast input (pin 19) during peak drive $V_{1,\ 2\ or\ 3-24} > V_{9-24}$	I_{19}	–	20	–	mA
Average beam current limiting input (pin 25; note 5)					
Start of contrast reduction at maximum contrast setting	V_{25-24}	–	8,5	–	V
Input range for full contrast reduction	ΔV_{25-24}	–	1,0	–	V
Input resistance at $V_{25-24} < 6$ V	R_{25}	–	2,2	–	kΩ
Saturation control input (pin 16) (saturation control acts on CD signals or RGB1 signals respectively)					
Maximum saturation	V_{16-24}	–	4	–	V
Nominal saturation (6 dB below max.)	V_{16-24}	–	3	–	V
Attenuation of saturation at V_{16-24} = 1,8 V (related to max. at 100 kHz)		50	–	–	dB
Input current at V_{16-24} = 1,8 to 4 V	I_{16}	–	–	10	μA

parameter	symbol	min.	typ.	max.	unit
Brightness control input (pin 20; note 6 and 7)					
Control voltage range	V_{20-24}	1	–	3	V
Input current at V_{20-24} = 1 to 3 V	$-I_{20}$	–	–	10	μA
Control voltage for nominal brightness	V_{20-24}	–	2,2	–	V
Change of black level in the control range related to the nominal output signal (black/white) for ΔV_{20-24} = 1 V		–	33	–	%
Signal switched off and black level equal to cut-off measuring level at	V_{20-24}	11,5	–	–	V
Y, (R-Y), (B-Y)/RGB – Matrix (note 8)					
PAL matrix (V_{8-24} = < 4,5 V)					
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$					
NTSC matrix (V_{8-24} = > 5,5 V)					
(Adaption for NTSC-FCC primaries, nominal hue control set on -5^{o})					
Matrixed according to the equation $V_{(G-Y)}{}^{*} = -0{,}43\ V_{(R-Y)} - 0{,}11\ V_{(B-Y)}$					
$V_{(R-Y)}{}^{*} = 1{,}57\ V_{(R-Y)} - 0{,}41\ V_{(B-Y)}$					
$V_{(B-Y)}{}^{*} = V_{(B-Y)}$					
RGB2 inputs (Teletext) (R2 pin 23, G2 pin 22, B2 pin 21; note 2)					
(RGB signals controlled by brightness control)					
Input signal for 100% output signals (black to white value)	$V_{21, 22, 23-24}$	–	1	–	V
Input current during scanning	$I_{21, 22, 23}$	–	–	0,3	μA
Input resistance	$R_{21, 22, 23}$	5	–	–	MΩ
Signal switch 2 input (pin 28)					
Input voltage level for insertion of Y, CD signals or RGB1 signals respectively					
RGB signals from matrix (note 9)	V_{28-24}	–	–	0,4	V
RGB2 signals (note 9)	V_{28-24}	0,9	–	3,0	V
Internal resistor to ground	R_{28-24}	–	10	–	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Automatic cut-off control input (pin 26; note 10) (leakage current measuring time and insertion of RGB cut-off measuring lines see Fig. 5; types of ultra-black level see Fig. 3)					
Allowed maximum external D.C. bias voltage	$V_{26\text{-}24}$	5,5	–	–	V
Voltage difference between cut-off current measurement and leakage current measurement	$\Delta V_{26\text{-}24}$	–	0,5	–	V
Warm-up test pulse	$V_{1,\,3,\,5\text{-}24}$	–	$V_{9\text{-}24}$*	–	V
Threshold for warm-up detector	$V_{26\text{-}24}$	–	8	–	V
Storage input for leakage current (pin 27)					
Internal resistance during leakage current measuring time (current limiting at I_{27} = 0,2 mA)	R_{27}	–	400	–	Ω
Input current except during cut-off control cycle	$\|I_{27}\|$	–	–	0,5	μA
Storage inputs for automatic cut-off control (pins 2, 4, 7)					
Charge and discharge currents	$\|I_{2,\,4,\,7}\|$	–	0,3	–	mA
Input currents of storage inputs out of control time	$\|I_{2,\,4,\,7}\|$	–	–	0,1	μA
Switch input for PAL/NTSC matrix and vertical blanking time (pin 8; note 11)					
Switching voltage input for					
PAL matrix and vertical blanking period of					
25 lines	$V_{8\text{-}24}$	–	0	0,5	V
22 lines	$V_{8\text{-}24}$	1,5	2	2,5	V
18 lines	$V_{8\text{-}24}$	3,5	4	4,5	V
NTSC matrix and vertical blanking period of					
18 lines	$V_{8\text{-}24}$	5,5	6	12	V
Input current	I_8	–	–	50	μA

* Maximum 8 V.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10; note 12)					
The following amplitudes are required for separating the various pulses:					
horizontal and vertical blanking pulses	V_{10-24}	2,0	2,5	3,0	V
horizontal pulses for counter logic	V_{10-24}	4,0	4,5	5,0	V
clamping pulses	V_{10-24}	7,5	–	–	V
delay of leading edge of clamping pulse	t_d	–	1	–	µs
Input current at V_{10-24} = 0 V	$-I_{10}$	–	–	100	µA
Outputs for positive RGB signals (R0 pin 1, G0 pin 3, B0 pin 5; note 13)					
Nominal signal amplitude (black/white)	$V_{1, 3, 5-24}$	–	3	–	V
Spreads between channels		–	–	10	%
Maximum signal amplitude (black/white)	$V_{1, 3, 5-24}$	4	–	–	V
Internal current source	$I_{1, 3, 5}$	–	3	–	mA
Output resistance	$R_{1, 3, 5}$	–	160	220	Ω
Minimum output voltage	$V_{1, 3, 5-24}$	–	1	–	V
Maximum output voltage	$V_{1, 3, 5-24}$	–	10	–	V
Horizontal and vertical blanking to ultra-black level 2 related to nominal signal black level in percentage of nominal signal amplitude		45	55	–	%
Vertical blanking to ultra-black level 1 related to cut-off measuring level in percentage of nominal signal amplitude		25	35	–	%
Recommendation:					
Range for cut-off measuring level 1,5 to 5,0 V; nominal value at 3 V (note 14)					
Gain data (note 15)					
Frequency response of Y path (0 to 8 MHz) pins 1, 3 and 5 to pin 15	d	–	–	3	dB
Frequency response of CD path (0 to 8 MHz) pin 1 to pin 17 = pin 5 to pin 18	d	–	–	3	dB
Frequency response of RGB1 path (0 to 8 MHz) pin 1 to pin 14 = pin 3 to pin 13 = pin 5 to pin 12	d	–	–	3	dB
Frequency response of RGB2 path (0 to 10 MHz) pin 1 to pin 23 = pin 3 to pin 22 = pin 5 to pin 21	d	–	–	3	dB

Notes to the characteristics

1. The value of the colour difference input signals, −(B-Y) and −(R-Y), is given for saturated colour bar with 75% of maximum amplitude.
2. Capacitive coupled to a low ohmic source; recommended value 600 Ω (max.).
3. At pin 19 for $V_{19-24} \leqslant 2{,}0$ V, no further decrease of contrast is possible.
4. The peak drive limiting of output signals is achieved by contrast reduction. The limiting level of the output signals is equal to the voltage V_{9-24}, adjustable in the range 5 to 11 V. After exceeding the adjusted limiting level at peak drive limiter will not be active during the first line.
5. The average beam current limiting acts on contrast and at minimum contrast on brightness (the external contrast voltage at pin 19 is not affected).
6. At nominal brightness the black level at the output is 0,3 V ($\hat{=}$ −10% of nominal signal amplitude) below the measuring level.
7. The internal control voltage can never be more positive than 0,7 V above the internal contrast voltage.
8. Matrix equation

   $V_{(R-Y)}$, $V_{(B-Y)}$: output of NTSC decoder of PAL type demodulating axis and amplitudes

   $V_{(G-Y)}{}^*$, $V_{(R-Y)}{}^*$, $V_{(B-Y)}{}^*$: for NTSC modified CD signals; equivalent to demodulation with the following axes and amplification factors:−

(B-Y)* demodulator axis	0°	
(R-Y)* demodulator axis	115°	(PAL 90°)
(R-Y)* amplification factor	1,97	(PAL 1,14)
(B-Y)* amplification factor	2,03	(PAL 2,03)

   $V_{(G-Y)}{}^* = -0{,}27\ V_{(R-Y)}{}^* - 0{,}22\ V_{(B-Y)}{}^*$.
9. During clamping time, in each channel the black level of the inserted signal is clamped on the black level of the internal signal behind the matrix (dependent on brightness control).
10. During warm-up time of the picture tube, the RGB outputs (pins 1, 3 and 5) are blanked to minimum output voltage. An inserted white pulse during the vertical flyback is used for beam current detection. If the beam current exceeds the threshold of the warm-up detector at pin 26, the cut-off current control starts operating, but the video signal is still blanked. After run-in of the cut-off current control loop, the video signal will be released.
    The first measuring pulse occurs in the first complete line after the end of the vertical part of the sandcastle pulse. The absolute minimum vertical part must contain 9 line-pulses. The cycle time of the counter is 63 lines. When the vertical pulse is longer than 61 lines, the IC is reset to the switch-on condition. In this event the video signal is blanked and the RGB-outputs are blanked to minimum output voltage as during warm-up time.
    During leakage current measurement, all three channels are blanked to ultra-black level 1. With the measuring level only in the controlled channel, the other two channels are blanked to ultra-black level 1. The brightness control shifts both the signal black level and the ultra-black level 2. The brightness control is disabled from line 4 to the end of the last measuring line (see Fig. 3).
    With the most adverse conditions (maximum brightness and minimum black level 2) the blanking level is located 30% of nominal signal amplitude below the cut-off measuring level.

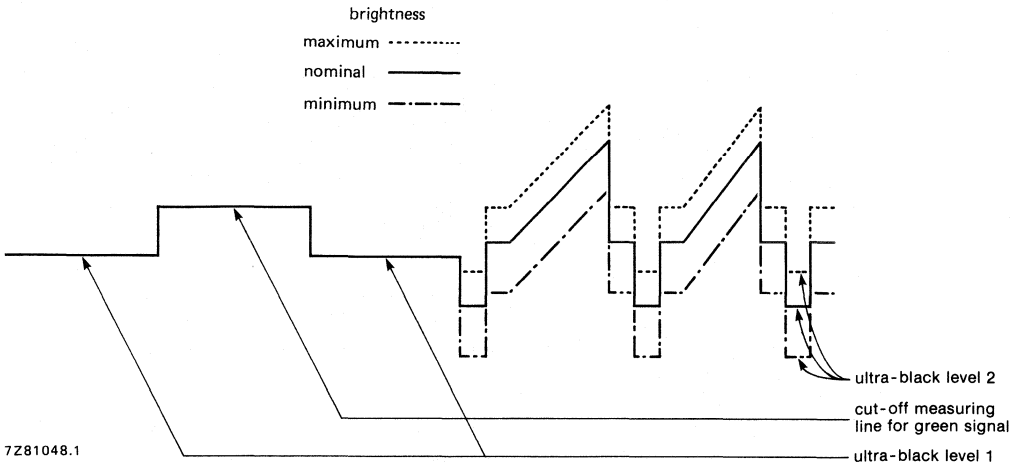
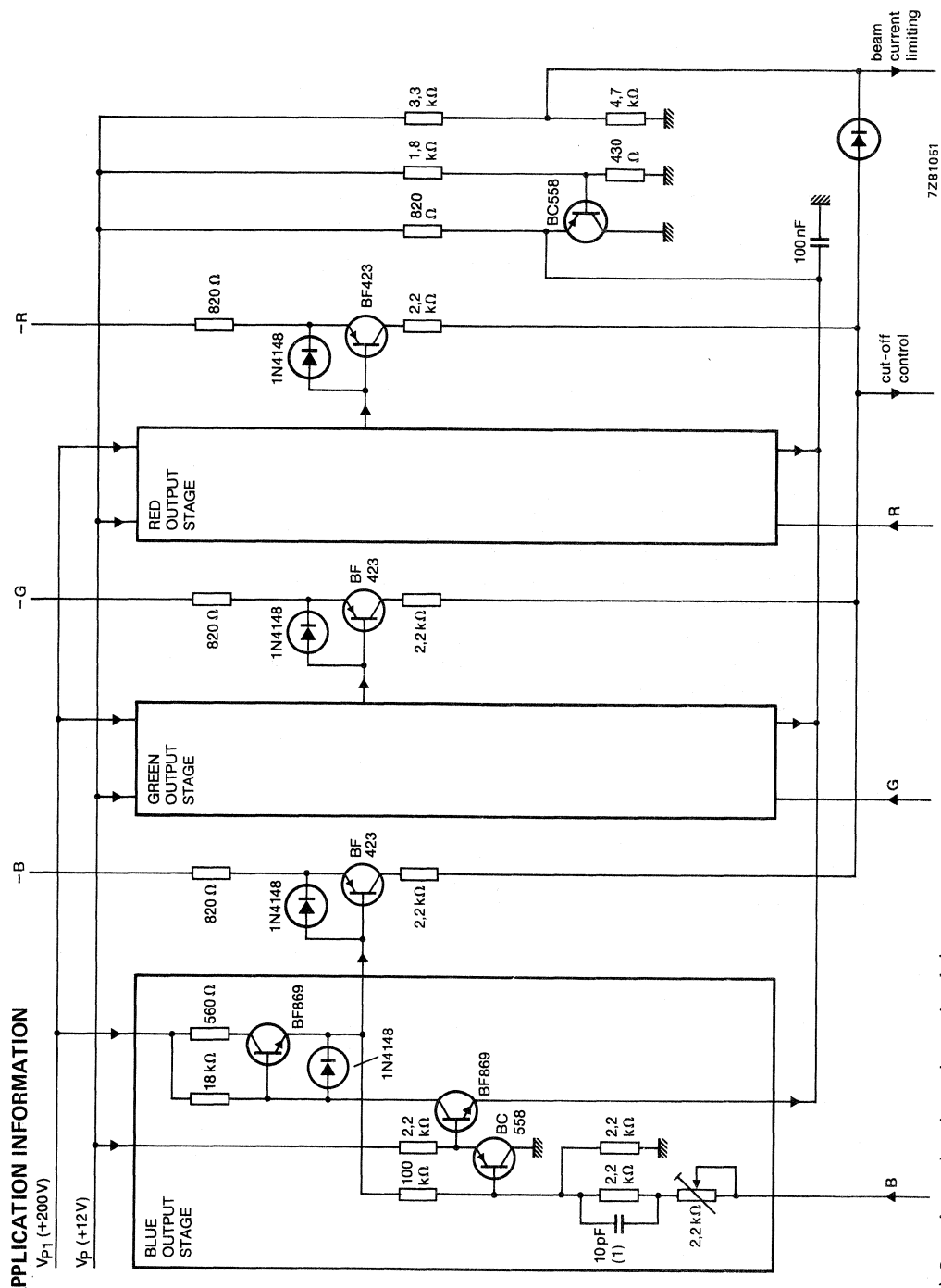


Fig. 3 Types of ultra-black levels.

11. The given blanking times are valid for the vertical part of the sandcastle pulse of 9 to 15 lines. If the vertical part is longer and the cut-off lines are outside the vertical blanking period of 18, 22 or 25 lines respectively, the blanking of the signal ends with the end of last of the three cut-off measuring pulses as shown in Fig. 5.
12. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) to separate the various pulses. The internal pulses are generated when the input pulse at pin 10 exceeds the thresholds. The thresholds are for:
    - Horizontal and vertical blanking $V_{10\text{-}24} = 1{,}5$ V
    - Horizontal pulse $V_{10\text{-}24} = 3{,}5$ V
    - Clamping pulse $V_{10\text{-}24} = 7{,}0$ V
13. The outputs at pins 1, 3 and 5 are emitter followers with current sources and emitter protection resistors.
14. The value of the cut-off control range for the positive RGB output signals is given for a nominal output signal. If the signal amplitude is reduced, the cut-off range can be increased.
15. The gain data is given for a nominal setting of the contrast and saturation controls, measured without load at the RGB outputs (pins 1, 3 and 5).



(1) Capacitor value depends on circuit layout.

Fig. 4a Part of typical application circuit diagram using the TDA4580; continued in Fig. 4b.

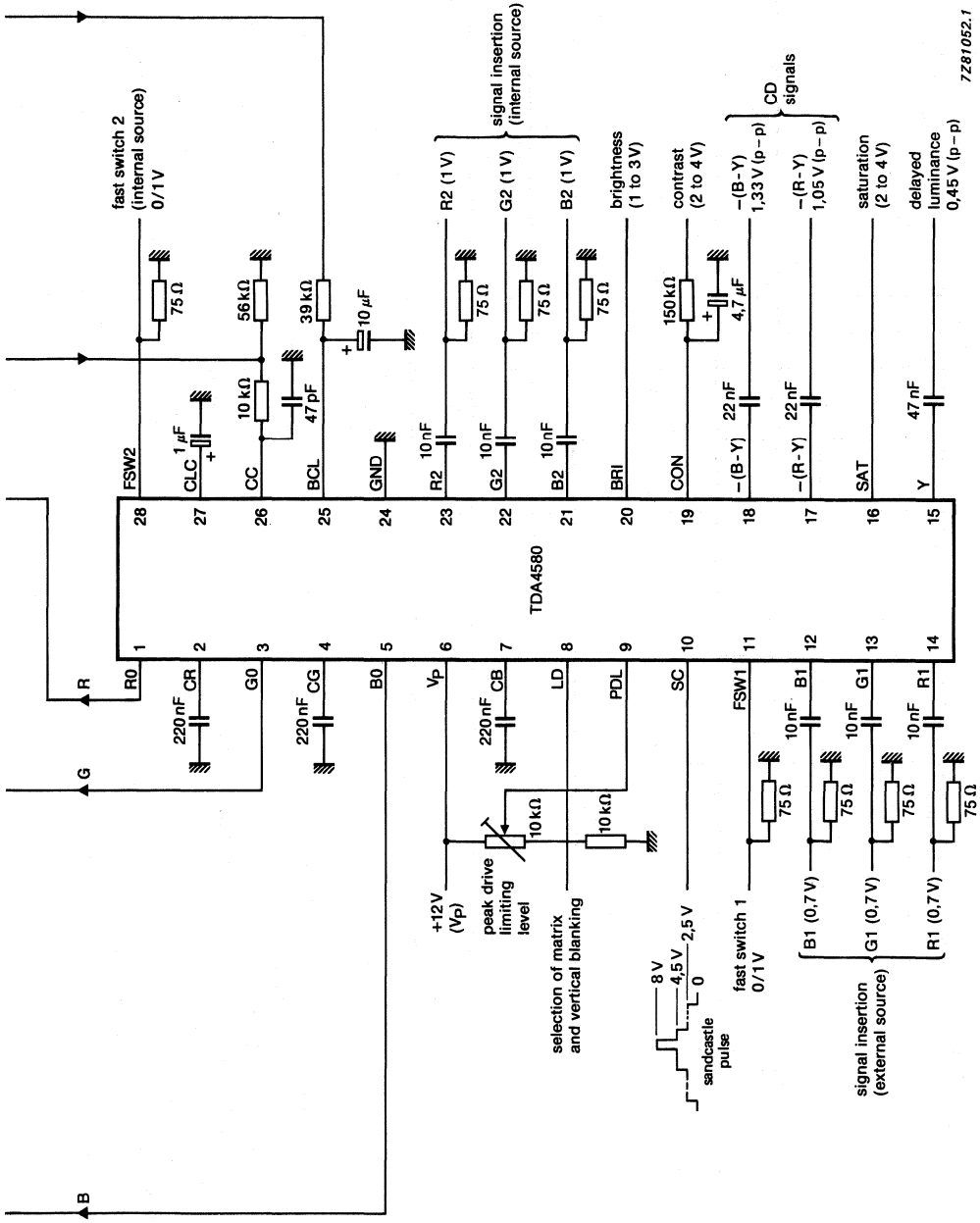
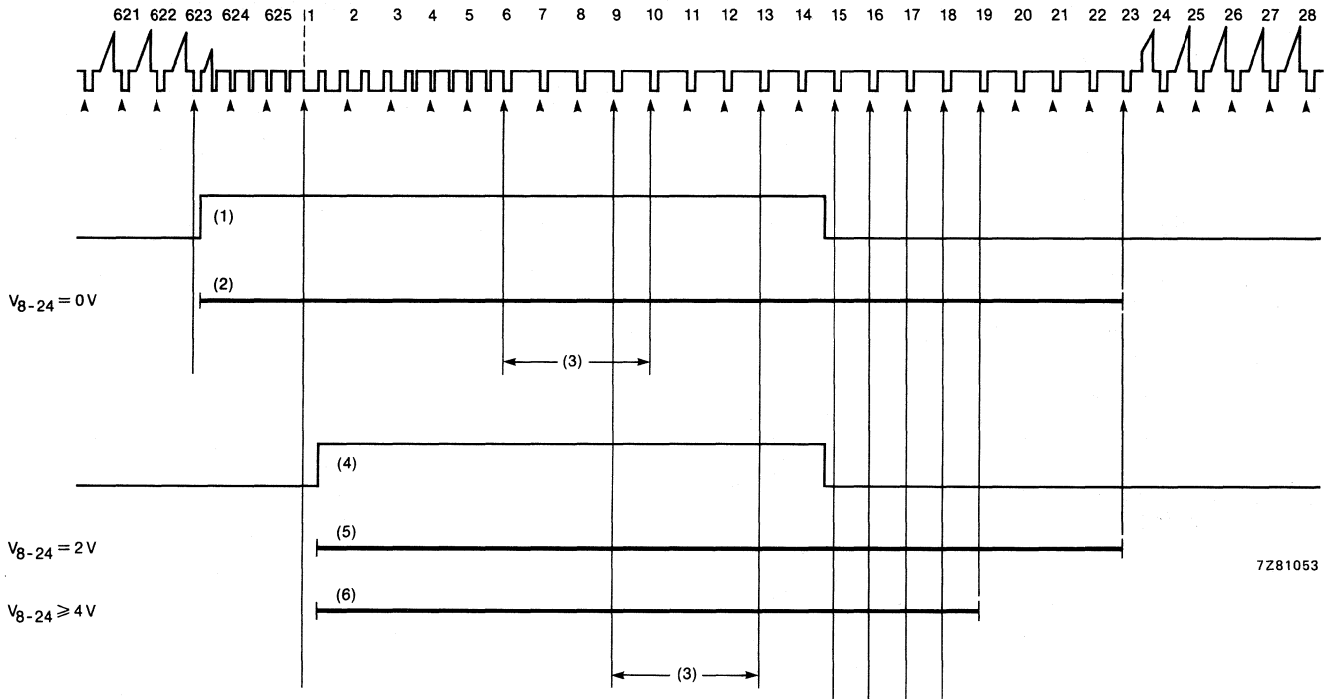


Fig. 4b Part of typical application circuit diagram using the TDA4580; continued from Fig. 4a.

APPLICATION INFORMATION (continued)



(1) vertical part of sandcastle pulse starts with equalizing pulses and ends with flyback.
(2) blanking period of 25 complete lines.
(3) leakage measuring period (LM).
(4) vertical part of sandcastle pulse starts and ends with flyback.
(5) blanking period of 22 complete lines.
(6) blanking period of 18 complete lines.
(7) cut-off measuring line for red signal (MR).
(8) cut-off measuring line for green signal (MG).
(9) cut-off measuring line for blue signal (MB).

Fig. 5 Blanking and measuring lines.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4650

Multistandard colour decoder, with negative colour difference output signals

FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter-amplifier
  - quadrature-demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour-difference signal output filters to remove the residual subcarrier

GENERAL DESCRIPTION

The TDA4650 is a monolitic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour-difference output signals are fed to the TDA4660/TDA4661, Switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 13)		10.8	12.0	13.2	V
I_P	supply current (pin 13)		–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)		20	100	400	mV
$V_{o(p-p)}$	colour-difference output voltage (pin 1) (peak-to-peak value)	PAL/NTSC	0.42	0.525	0.66	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	PAL/NTSC	0.53	0.665	0.84	V
	colour-difference output voltage (pin 1) (peak-to-peak value)	SECAM	0.83	1.05	1.32	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	SECAM	1.06	1.33	1.67	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4650	28	DIL	plastic	SOT117
TDA4650WP	28	PLCC	plastic	SOT261

Multistandard colour decoder, with negative colour difference output signals

TDA4650

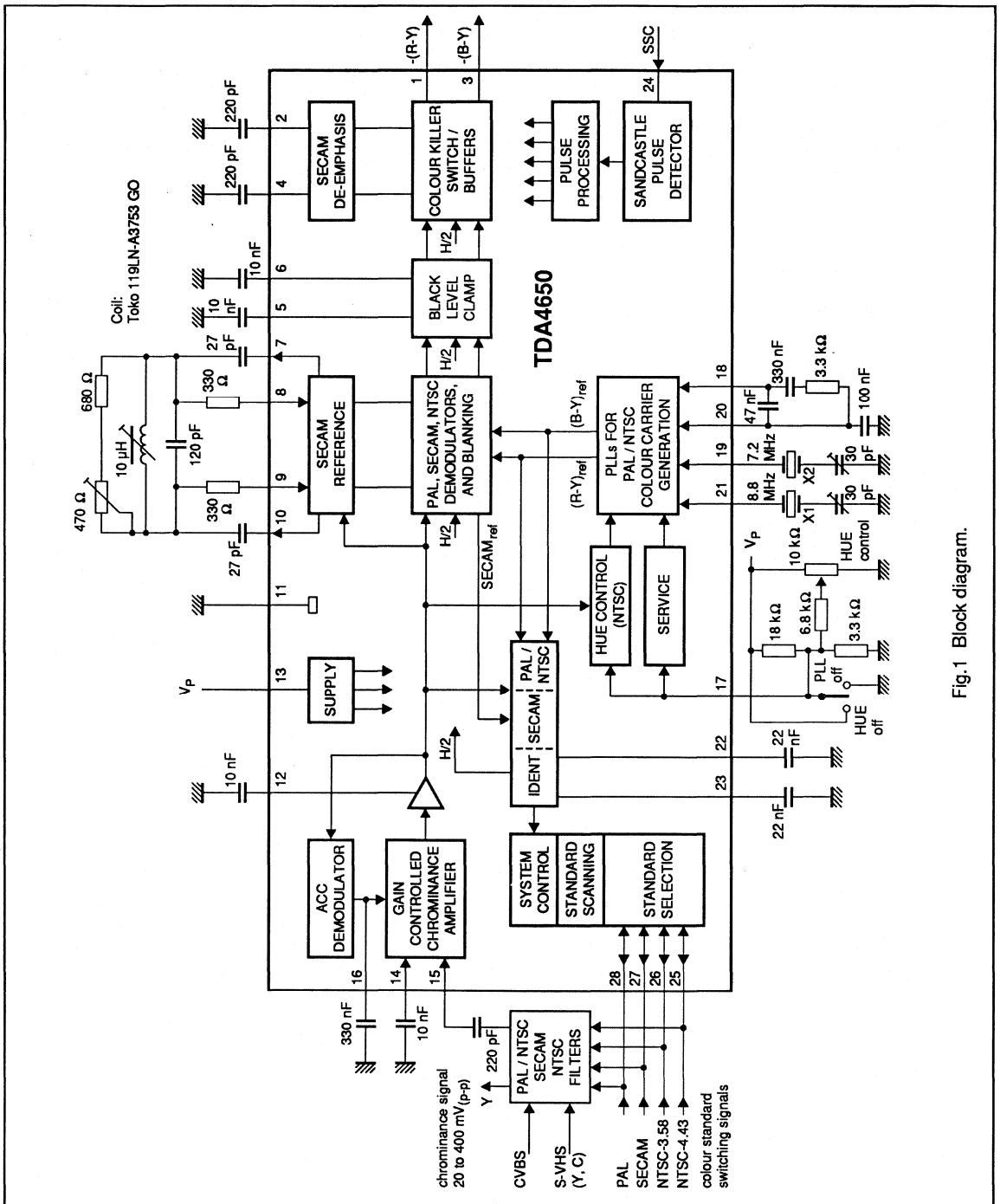


Fig.1 Block diagram.

Multistandard colour decoder, with negative colour difference output signals

TDA4650

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	-(R-Y) output
$-(R-Y)_{DE}$	2	(R-Y) de-emphasis
$-(B-Y)_O$	3	-(B-Y) output
$-(B-Y)_{DE}$	4	(B-Y) de-emphasis
$-(B-Y)_{CL}$	5	(B-Y) clamping
$-(R-Y)_{CL}$	6	(R-Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
SEC_{REF}	8	
SEC_{REF}	9	
SEC_{REF}	10	
GND	11	ground
C_D	12	DC for demodulators
V_P	13	supply voltage
C_{DC}	14	DC feedback

SYMBOL	PIN	DESCRIPTION
CHR_I	15	chrominance input
C_{ACC}	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C_{PLL}	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N_{IDENT}	22	NTSC identification
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N_{O1}	25	NTSC (4.43 MHz) identification
N_{O2}	26	NTSC (3.58 MHz) identification
SEC_O	27	SECAM identification
PAL_O	28	PAL identification

PIN CONFIGURATIONS

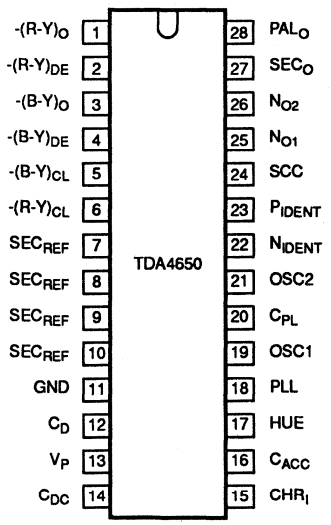


Fig.2(a) Pin configuration for DIL package.

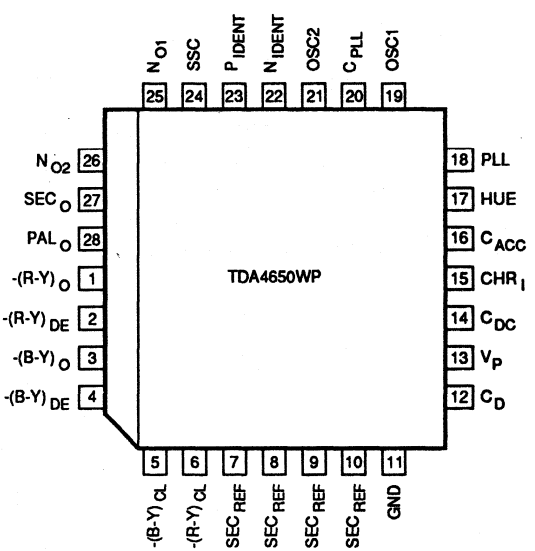


Fig.2(b) Pin configuration for PLCC package.

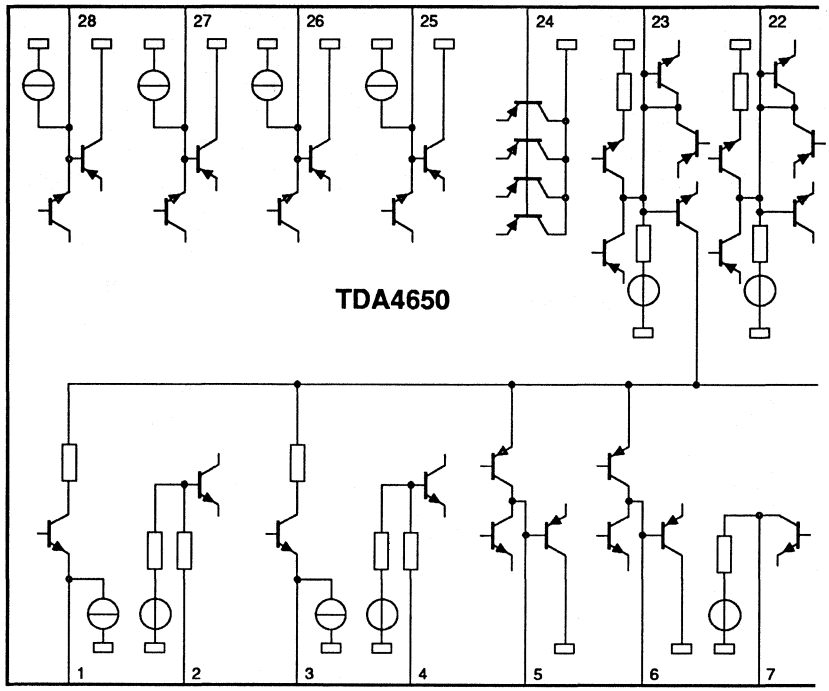


Fig.3a Internal circuits (continued in Fig.3b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13) –	13.2	V	
V_I	voltage range at pins 1, 3, 17 and 24 to 28	0	V_P	V
I_o	output current (pins 1 and 3)	–	–5	mA
$I_{i/o}$	input/output current (pins 25 to 28)	–	–5	μA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
$R_{th\ j\text{-}a}$	from junction to ambient in free air: SOT117	–	37	K/W
	SOT261	–	70	K/W
P_{tot}	total power dissipation (SOT117)	–	1.4	W
	total power dissipation (SOT261)	–	1.1	W

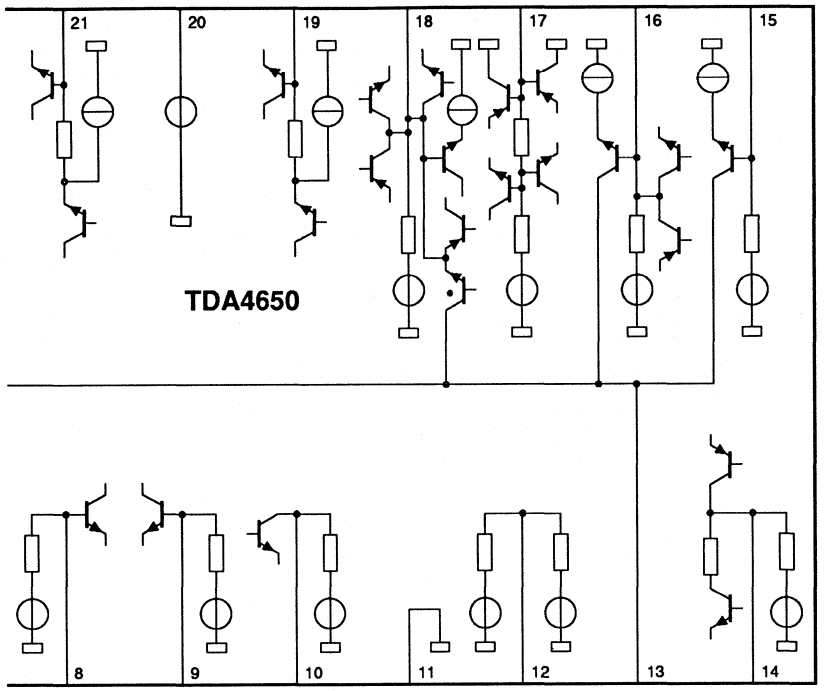


Fig.3b Internal circuits (continued from Fig.3a).

Multistandard colour decoder, with negative colour difference output signals

TDA4650

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15(p-p)}$ = 100 mV (with 75 % colour bar signal); 4 µs burst-blanking pulse and vertical blanking superimposed on super sandcastle pulse; T_{amb} = 25 °C; measured in test circuit of Fig. 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		10.8	12.0	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i(p-p)}$	input signal (pin 15) (peak-to-peak value)		20	100	400	mV
R_i	input resistance (pin 15)		7	10	13	kΩ
C_i	input capacitance (pin 15)		–	4	5	pF
Demodulator part (PAL/NTSC)						
$V_{1(p-p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.42	0.525	0.66	V
$V_{3(p-p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.53	0.665	0.84	V
V_1/V_3	ratio of colour difference signals (R-Y)/(B-Y) for NTSC	at nominal phase of hue control	0.75	0.79	0.83	
V_1/V_1	ratio of PAL/NTSC signals $(R\text{-}Y)_{PAL}/(R\text{-}Y)_{NTSC}$	at nominal phase of hue control	–	–	1	dB
m	signal linearity	$V_{1(p-p)}$ = 0.8 V – (R-Y)	0.8	–	–	
		$V_{3(p-p)}$ = 1.0 V – (B-Y)	0.8	–	–	
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	Ω
Demodulator part (SECAM); note 1						
$V_{1(p-p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	every second line blanked	0.83	1.05	1.32	V
$V_{3(p-p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	every second line blanked	1.06	1.33	1.67	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV

Multistandard colour decoder, with negative colour difference output signals

TDA4650

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator part (SECAM) (continued); note 1						
$\Delta V_{1,3}/\Delta V_P$	shift of blanking levels relative to demodulated f_o levels		–	–	3	mV/V
$\Delta V_1/\Delta T$			–	0.16	–	mV/K
$\Delta V_3/\Delta T$			–	–0.25	–	mV/K
Hue control part						
ϕ	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 2 V	–30	–40	–	deg
	phase shift of reference carrier	V_{17} = 3 V	–	0	± 5	deg
	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 4 V	30	40	–	deg
V_{17}	internal bias voltage		–	3	–	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	–	0.5	V
	switching voltage for forced colour ON	burst ON; colour ON	5.5	–	V_P	V
R_{17}	input resistance		3.8	5.0	6.2	kΩ
Reference oscillator (PLL); note 2						
$R_{19,21}$	input resistance		–	350	–	Ω
$C_{19,21}$	input resistance		–	–	10	pF
f_c	catching range	at 4.43 MHz	± 400	–	–	Hz
		at 3.57 MHz	± 330	–	–	Hz
Identification part switching voltages for chrominance filters and crystals: at pin 28 for PAL at pin 27 for SECAM at pin 26 for NTSC (3.58 MHz) at pin 25 for NTSC (4.43 MHz)						
$V_{28\ to\ 25}$	switching voltages	control voltage OFF state	–	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	–	V_P	V
$I_{28\ to\ 25}$	output currents		–	–	–3	mA
t_d	delay time for system hold		2	–	3	cycles
	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
t_s	scanning time for each standard	note 3	–	4	–	cycles

Multistandard colour decoder, with negative colour difference output signals

TDA4650

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Super sandcastle pulse detector (note 4)						
V_{24}	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	voltage pulse amplitude		7.7	–	V_P	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	μA

Notes to the characteristics

1. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R-Y) and (B-Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_o voltage level is zero in the -(B-Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_o voltage level is zero in the -(R-Y) output channel at pin 1. If necessary, the f_o voltage level in the -(B-Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at the pins 2 and 4 (220 pF each) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
2. The f_o frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
3. The inquiry sequence for the standard is:
   PAL – SECAM – NTSC (3.58 MHz) – NTSC (4.43 MHz).
   PAL has priority with respect to SECAM, etc.
4. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

Multistandard colour decoder, with negative colour difference output signals

TDA4650

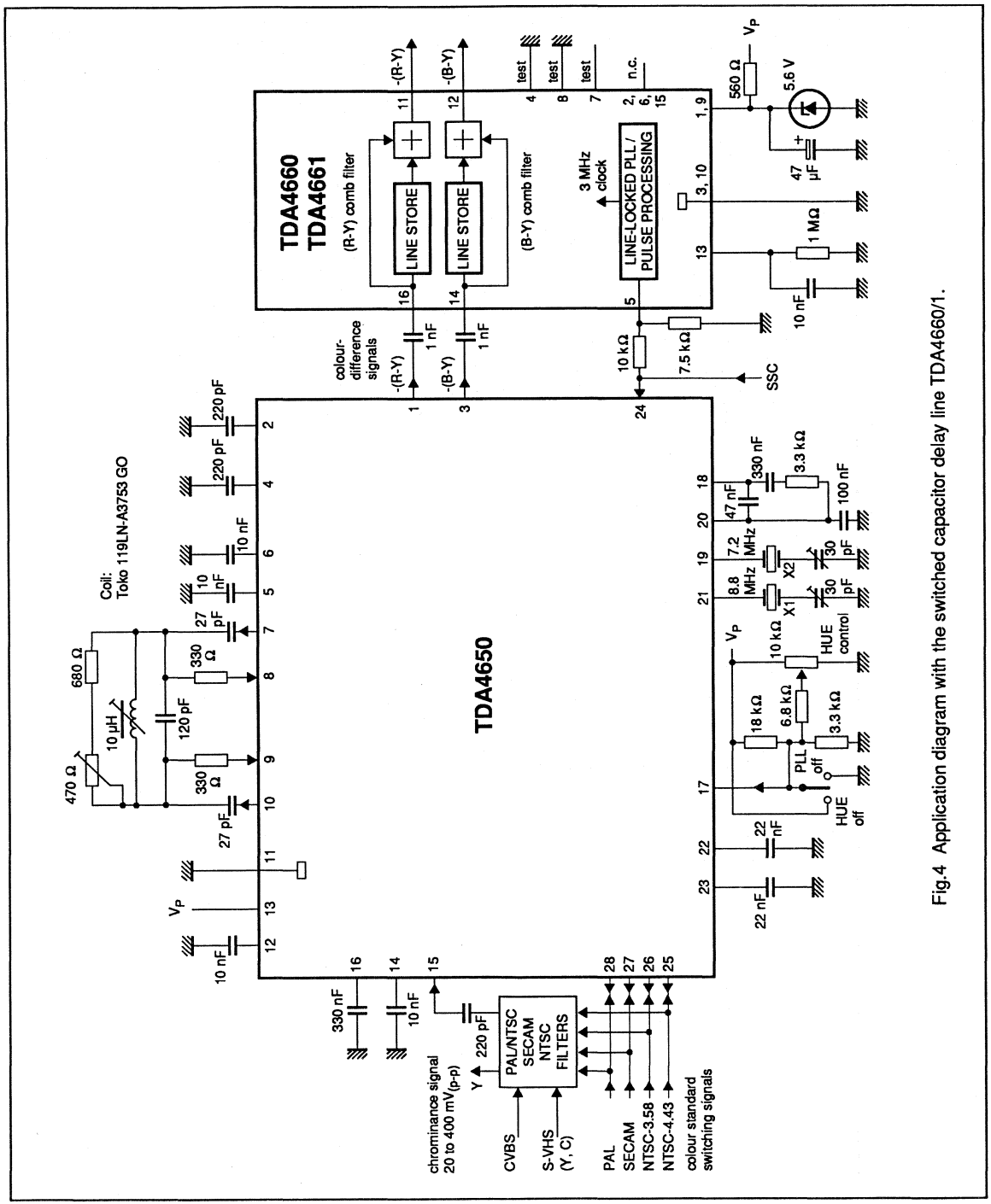


Fig.4 Application diagram with the switched capacitor delay line TDA4660/1.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	March 1991

TDA4660

64 µs baseband delay line

FEATURES

- Two comb filters using the switched-capacitor technique and with a delay time of 64 µs
- Generation of a 3 MHz internal clock that is line-locked via the sandcastle pulse

GENERAL DESCRIPTION

The TDA4660 is an integrated baseband delay line circuit. It provides a delay of 64 µs for the colour difference signals, –(R-Y) and –(B-Y), in multi-standard TVs.

The colour difference signals are AC-coupled to pins 16 and 14 respectively and clamped at the input stages. The signals are then fed via buffers to the delay line circuit. The delay line circuit is driven by a 3 MHz internal clock which enables the circuit to produce the required delay of 64 µs.

The outputs from the delay line circuit are fed through sample-and-hold and low-pass filters to suppress the clock signal. The delayed and non-delayed signals are then added and fed to the output pins, 11 and 12, via buffers.

The internal clock is derived from a 6 MHz voltage controlled oscillator (VCO) which is line-locked via a PLL to the sandcastle pulse at pin 5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{1-3}	digital supply voltage		5.3	-	6.0	V
V_{9-10}	analog supply voltage		5.3	-	6.0	V
I_1	digital supply current		-	1.0	2.0	mA
I_9	analog supply current		-	4.5	8.0	mA
Colour difference input signals PAL and NTSC						
V_{16-10}	–(R-Y) (peak-to-peak value)		-	0.525	-	V
V_{14-10}	–(B-Y) (peak-to-peak value)		-	0.675	-	V
SECAM						
V_{16-10}	–(R-Y) (peak-to-peak value)	note 1	-	1.05	-	V
V_{14-10}	–(B-Y) (peak-to-peak value)	note 1	-	1.35	-	V
Gain of colour difference output signals (V_O/V_I)						
V_{11}/V_{16}	PAL, NTSC		4.5	5.5	6.5	dB
V_{12}/V_{14}			4.5	5.5	6.5	dB
V_{11}/V_{16}	SECAM	note 1	–1.5	–0.5	0.5	dB
V_{12}/V_{14}		note 1	–1.5	–0.5	0.5	dB

Note to the quick reference data

1. The signals must be blanked line-sequentially. The blanking levels must be equal to the uncoloured signal.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4660	16	DIL	plastic	SOT38
TDA4660T	16	SO16L	plastic	SOT162A

64 μs baseband delay line

TDA4660

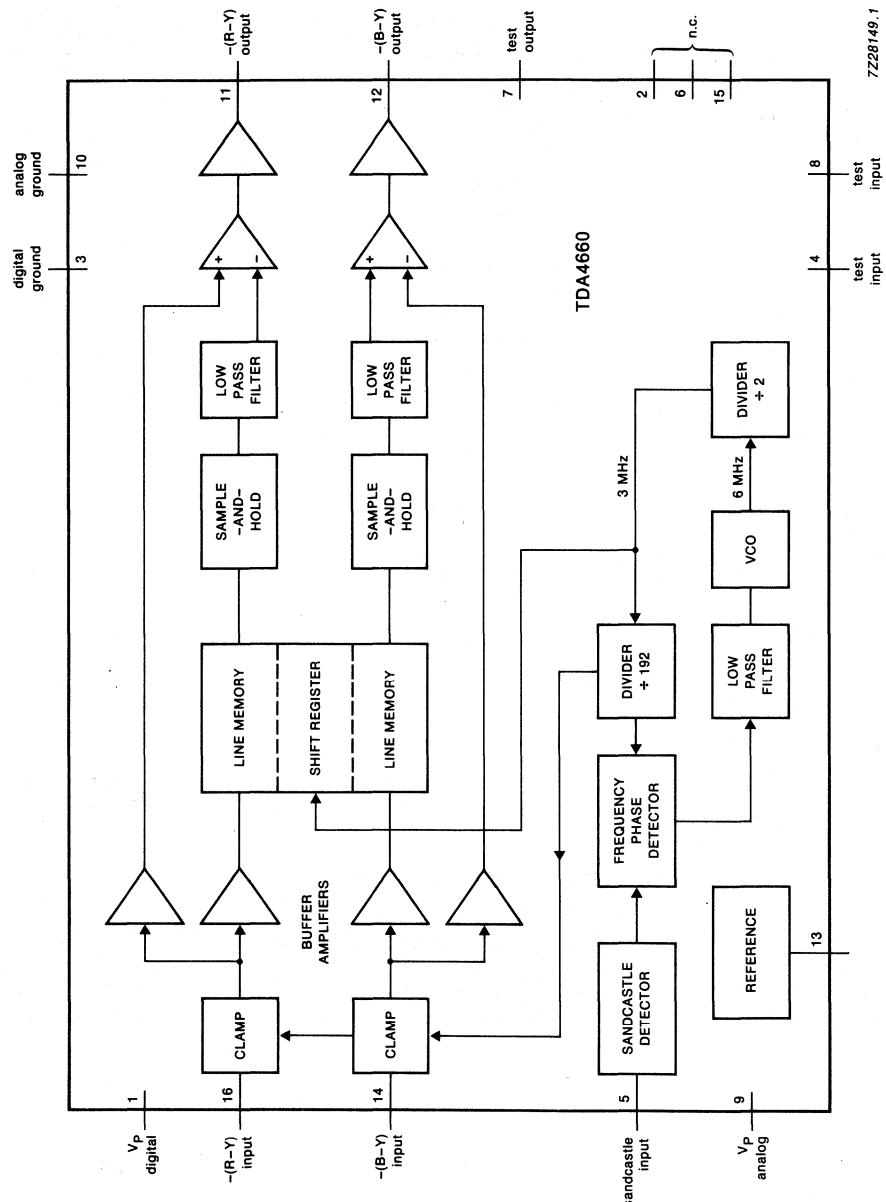


Fig.1 Block diagram.

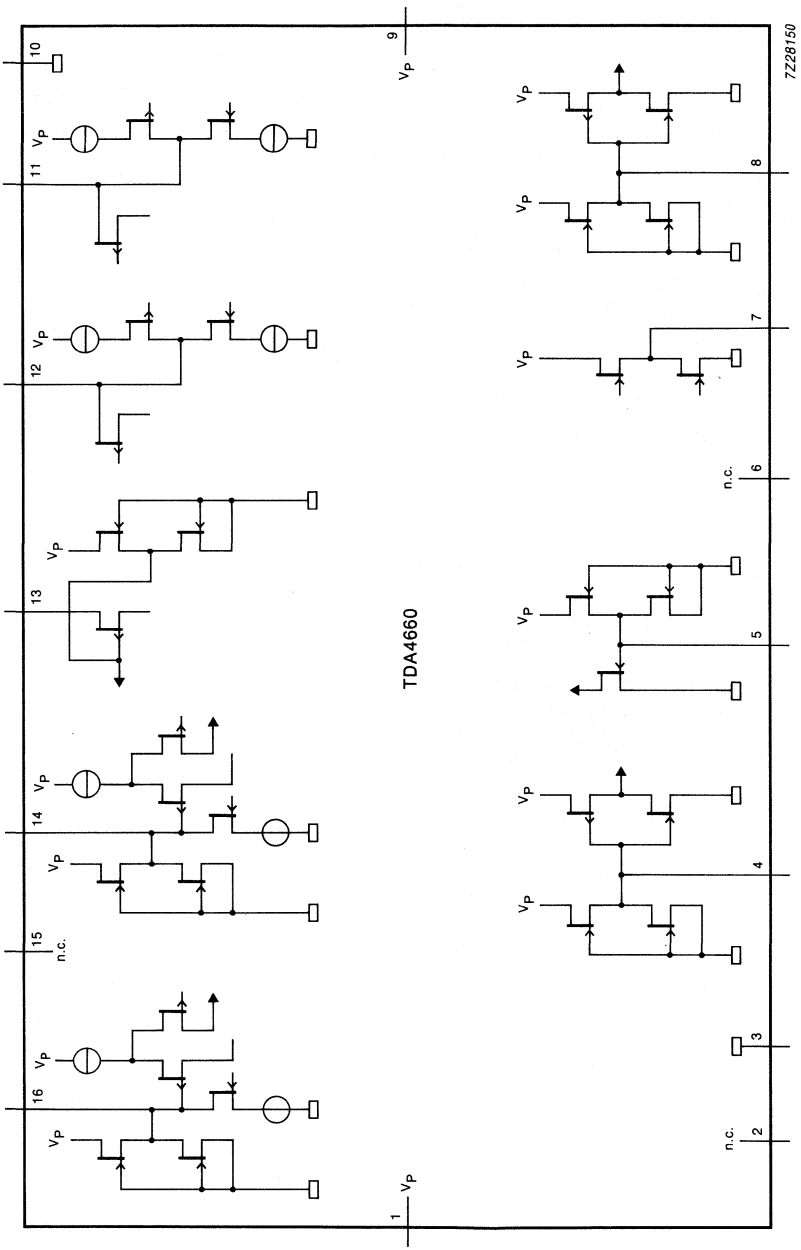


Fig.2 Internal pin circuit diagram.

PINNING

PIN	DESCRIPTION
1	digital supply voltage
2	not connected
3	digital ground
4	test input
5	sandcastle input
6	not connected
7	test output
8	test input
9	analog supply voltage
10	analog ground
11	-(R-Y) output
12	-(B-Y) output
13	reference current
14	-(B-Y) input
15	not connected
16	-(R-Y) input

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{1-3}, V_{9-10}	supply voltages		−0.5	+ 7	V
V_{n-3}, V_{n-10}	voltage at pins 4, 5, 7, 8, 11, 12, 14 and 16		−0.5	+ 7	V
T_{amb}	operating ambient temperature range		0	+ 70	°C
T_{stg}	storage temperature range		−25	+ 150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j-a}$	from junction to ambient in free air	-	80	K/W

CHARACTERISTICS

V_P = 5.6 V; f_H = 15.625 kHz; T_{amb} = 25 °C; R13 = 1 MΩ, C13 = 10 nF (see Fig.3); nominal signal for 75% colour bars; sandcastle with burst-key-pulse; supply voltages, digital and analog, must be connected; (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{1-3}	digital supply voltage		5.3	5.6	6.0	V
V_{9-10}	analog supply voltage		5.3	5.6	6.0	V
I_1	digital supply current		-	1	2	mA
I_9	analog supply current		-	4.5	8	mA
P_{tot}	total power dissipation		-	31	60	mW
Colour difference input signals PAL, NTSC						
$V_{16(p-p)}$	–(R-Y) input signal (peak-to-peak value)		-	0.525	-	V
$V_{14(p-p)}$	–(B-Y) input signal (peak-to-peak value)		-	0.675	-	V
$V_{14,16(p-p)}$	maximum symmetrical input signal (peak-to-peak value)	before clipping	1	-	-	V
SECAM (note 1)						
$V_{16(p-p)}$	–(R-Y) input signal (peak-to-peak value)		-	1.05	-	V
$V_{14(p-p)}$	–(B-Y) input signal (peak-to-peak value)		-	1.33	-	V
$V_{14,16(p-p)}$	maximum symmetrical input signal (peak-to-peak value)	before clipping	2	-	-	V
C14, C16	input capacitance		-	-	10	pF
R14, R16	input resistance during clamping		-	-	40	kΩ
$V_{14,16-10}$	clamping voltage	proportional to V_P	1.55	1.65	1.75	V
Sandcastle pulse (note 2)						
I_5	input leakage current		-	-	10	μA
C5	input capacitance		-	-	10	pF
V_{se}	slicing level below top sync level		-	1.5	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{bk}	input frequency of burst key		14.2	15.6	17	kHz
V_5	top sync pulse		3	-	7	V
Delayed colour difference output signals						
	amplitude ratio V_{11}/V_{16}, V_{12}/V_{14}	PAL, NTSC	4.5	5.5	6.5	dB
		SECAM	−1.5	−0.5	+ 0.5	dB
V_{11}/V_{12}	ratio of output amplitudes for equal input signals	$V_{14,16(p-p)}$ = 1.35 V	−0.4	0	+ 0.4	dB
t_d	time difference between non-delayed and delayed signals		63.94	64	64.06	μs
t_{ud}	delay time for non-delayed signal pulse response	$V_{14,16(p-p)}$ = 1.35 V	-	85	-	ns
t_{rud}	output transient time of; undelayed signal V_{11} and V_{12}	transient = 300 μs; SECAM mode	*	320	*	ns
t_{rd}	delayed signal V_{11} and V_{12}		*	350	*	ns
V_{11n}/V_{11n+1} V_{12n}/V_{12n+1}	ratio of the output signal for adjacent time samples at constant input signal	$V_{11,12(p-p)}$ = 1.35 V; SECAM mode	−0.1	0	+ 0.1	dB
V_{11}, V_{12}	noise voltage (RMS value)	V_{16-10}, V_{14-10} = 0 V; R_S = 300 Ω (source); f = 10 kHz to 1 MHz	-	-	1.2	mV
R11, R12	output resistance		-	330	400	Ω
V_{11}, V_{12}	DC output voltage	proportional to V_P	2.9	3.1	3.3	V

Notes to the characteristics

1. The signals must be blanked line-sequentially. The blanking levels must be equal to the uncoloured signal.
2. The leading edge of the burst key is used for timing.

* Value to be fixed.

APPLICATION INFORMATION

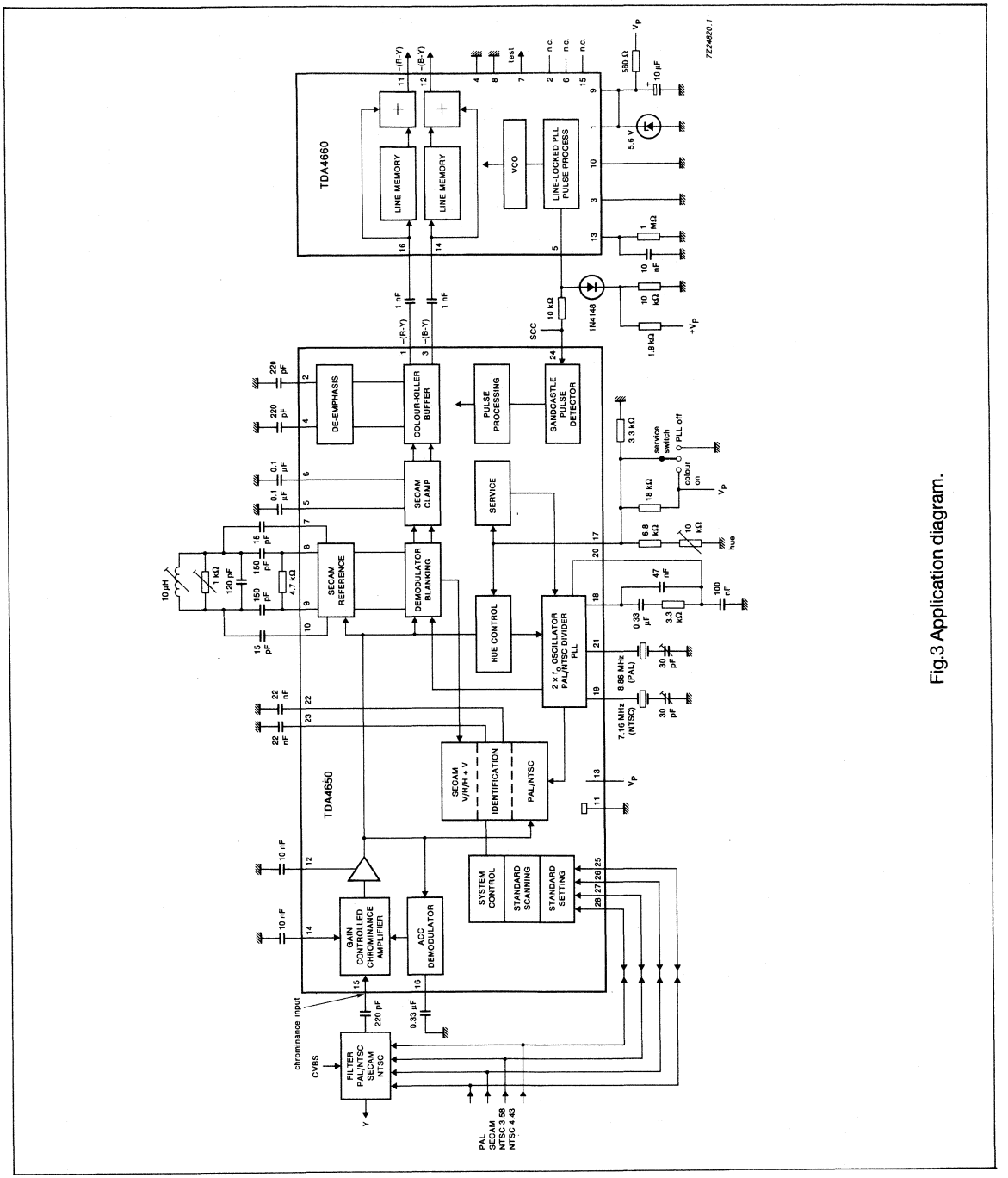


Fig.3 Application diagram.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	August 1990

TDA4670

Picture signal improvement circuit (PSI) in colour television receivers

GENERAL DESCRIPTION

The TDA4670 contains a luminance signal path which consists of a switchable delay line with peaking and coreing stage as well as two colour difference channels each consisting of a sample and hold circuit for improving the transient time of the chroma signal (see Fig.1).

Y-signal path

The Video Blanking Signal (VBS) input is capacitively coupled to pin 16. In the first stage the signal is clamped to the black level and then reduced to a suitable level for the following delay line. This delay line consists of 13 all-pass cells (t_{cell} = 90 ns) which are built with gyrators. The maximum possible delay time is 1135 ns. This delay time is switchable via the I²C-bus from 25 to 1135 ns in steps of 45 ns. An automatic control circuit ensures a good accuracy for the delay time (t_d = ±30 ns). The control voltage is generated from the line frequency between the 16th and 17th burstkey pulse after start of V-blanking. During the time from the 16th to the 18th burstkey pulse an oscillation voltage is present at the output pin 12.
A peaking circuit is incorporated with two selectable centre frequencies (2.6 and 5 MHz). This circuit consists of two additional delay cells, two 0.5 gain inverting amplifiers and a summation stage. For better noise behaviour the peaking signal is applied via a coreing stage and a switchable amplifier before being added to the main signal.
The suitable centre frequency and the grade of peaking can be controlled by means of I²C-bus commands.
The output buffer stage ensures a low ohmic output signal with zero gain with respect to the input.

Colour difference path

Both colour difference channels consist of a clamping stage at the input, a buffer amplifier, a storage stage and an output amplifier. The storage, which is operated by a differential amplifier, stores the colour difference signal during the transient time of the input signal and then switches rapidly to accept the new signal.
A signal formed by differentiating, full wave rectifying and summing the two colour difference signals is compared with a reference signal. The resultant signal is used to switch the sample-and-hold circuits.

Both CD channels have good uniformity and no signal attenuation. The colour transient improvement function can be switched on or off by means of the I²C-bus commands.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4670	18	DIL	plastic	SOT102

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670

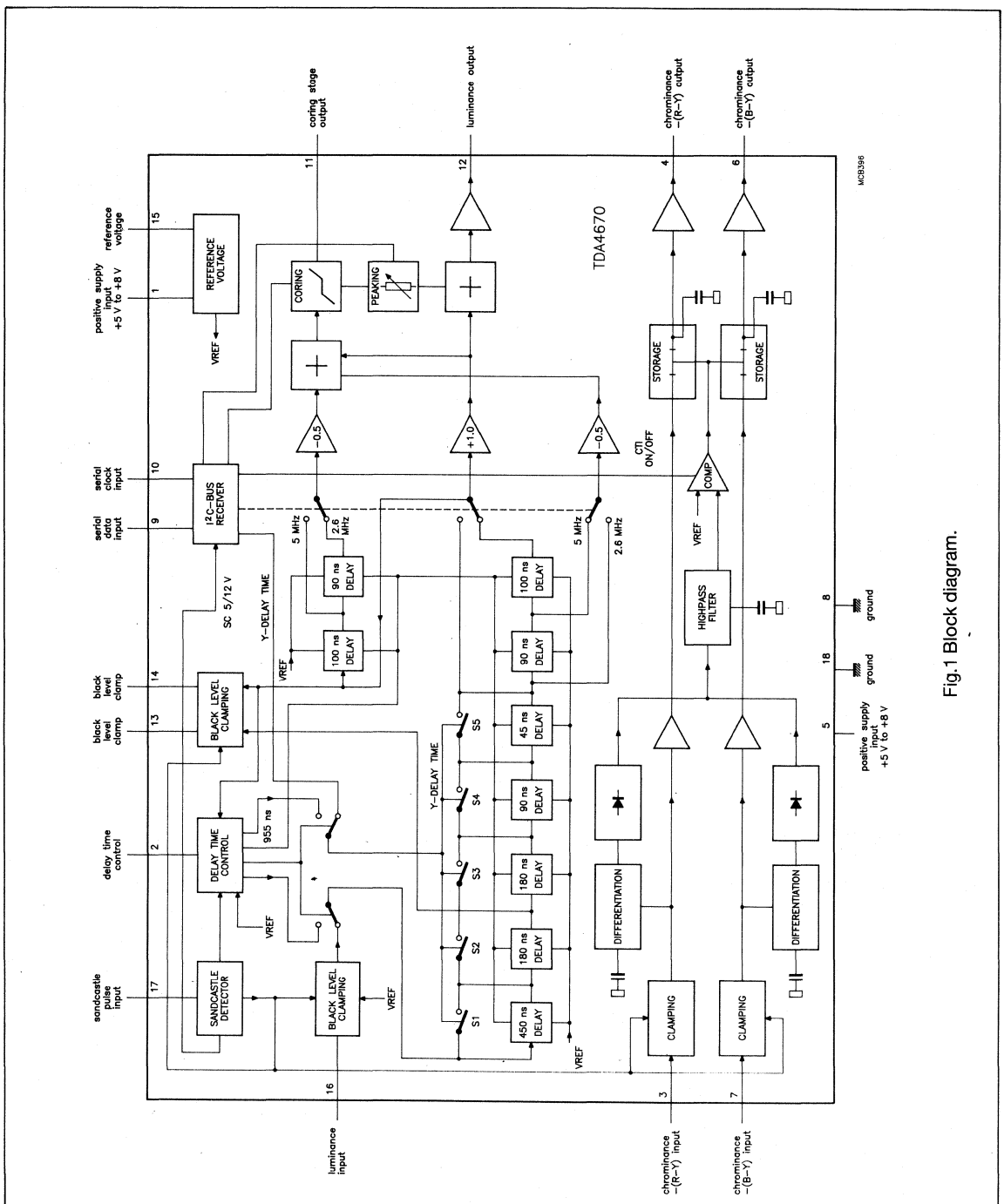
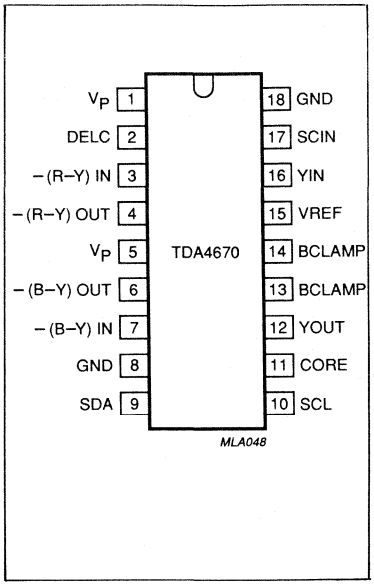


Fig.1 Block diagram.

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670



PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply input +5 V to +8 V
DELC	2	delay time control
-(R-Y)IN	3	chrominance -(R-Y) input
-(R-Y)OUT	4	chrominance -(R-Y) output
V_P	5	positive supply input +5 V to +8 V
-(B-Y)OUT	6	chrominance -(B-Y) output
-(B-Y)IN	7	chrominance -(B-Y) input
GND	8	ground
SDA	9	serial data input I^2C-bus
SCL	10	serial clock input I^2C-bus
CORE	11	coring stage output
YOUT	12	luminance output
BCLAMP	13	black level clamp
BCLAMP	14	black level clamp
VREF	15	reference voltage
YIN	16	luminance input
SCIN	17	sandcastle pulse input
GND	18	ground

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.5	5.0	8.8	V
I_P	supply current	31	41	52	mA
Y_d	Y-delay time	25	-	1135	µs
Y_{att}	Y-attenuation	-	1.0	-	dB
CD_{att}	(R-Y) and (B-Y) attenuation	-	0	-	dB

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{stg}	storage temperature range		-25	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
P_{tot}	total power dissipation	t_j = 150 °C; t_{amb} = 70 °C	-	0.97	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	82	K/W

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in application circuit see Fig.3 all voltages measured with respect to pin 18; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
V_P	supply voltage		4.5	-	8.8	V
I_P	supply current		31	41	52	mA
Y-signal path Luminance delay (note 1)						
$V_{16(p-p)}$	Y-input signal composite signal) peak-to-peak value)	capacitive coupling	-	0.45	0.64	V
V_{16}	internal bias voltage	during clamping to black level	-	3.10	-	V
R_{16}	input resistance	outside clamping	5	-	-	MΩ
C_{16}	input capacitance		-	3	10	pF
I_{16}	input current outside clamping		−0.1	-	0.1	µA
$\pm I_{16}$	input current during clamping		95	-	190	µA
t_{Ymax}	maximum Y-signal delay time	note 2	1105	1135	1165	ns
d_{tY}	minimum switchable delay step	delay time adjustable by I²C-bus	40	45	50	ns
t_{Ymin}	minimum Y-signal delay time	without peaking	-	25	-	ns
t_{Ymin}-t_{CDmin}	delay time difference luminance- to chrominance-signal	CTI and peaking off	70	100	130	ns
t_{Ywp}	minimum delay time peaking		185	215	245	ns
G_Y	Y-signal gain at 500 kHz (t_{Ymax}) between pins 12 and 16		−2.0	−1.0	0.0	dB
	Y-signal frequency response from 0.5 to 3 MHz (t_{Ymax})		−2.0	−1.0	0	dB
	Y-signal frequency response from 0.5 to 5 MHz (t_{Ymax})		−4.0	−3.0	−1.0	dB
Y_{tdg}	Y-signal group delay time difference from 0.5 to 5 MHz (t_{Ymax})		−25	0	25	ns
$m=a_{min}/a_{max}$ m	linearity for content	V_{VB} = 315 mV; (V_{VBS} = 0.45 V)	0.85	-	-	
		V_{VB} = 450 mV; (V_{VBS} = 0.64 V)	0.60	-	-	
Luminance peaking						
f_{C1} f_{C2}	peaking frequency	selectable via I²C-bus	4.5 2.3	5.0 2.6	5.5 2.9	MHz MHz
 P_{a1} P_{a2} P_{a3} P_{a4}	peaking amplitude selection (amplitude f_C/amplitude 0.5 MHz)	via I²C-bus	 - - - -	 6 3.5 0 -4.4	 - - - -	 dB dB dB dB
L	limitation of peaking (positive amplitude of correction signal/nominal VB-signal)		-	+20	-	%

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670

SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
VN	noise voltage (RMS value)	0 to 5 MHz; without peaking	-	-	1	mV
C	coreing of peaking (coreing part/nominal VB-signal)	switchable via I²C-bus	-	20	-	%
	output current	emitter follower with constant current source I_{source}	1.0	-	-	mA
I_{sink}			0.4	-	-	mA
R_O	output resistance		-	-	160	Ω
Colour-difference path (note 3)						
$V_{3(p-p)}$	(R-Y) signal (75% colour bar signal) (peak-to-peak value)		-	1.05	1.48	V
$V_{7(p-p)}$	(B-Y) signal (75% colour bar signal) (peak-to-peak value)		-	1.33	1.88	V
C_3, C_7	input capacitance		-	6	12	pF
I_3, I_7	input current outside clamping		−0.1	0	0.1	μA
$\pm I_3, I_7$	input current during clamping		100	-	190	μA
V_3, V_7	internal bias voltage during clamping		-	2.45	-	V
$V_3, V_7/d_t$	input transient sensitivity		0.15	-	-	V/μS
$V_6/V_3, V_6/V_7$	signal gain		−1	0	1	dB
	uniformity (R-Y/B-Y)		−0.3	0	0.3	dB
$m=a_{min}/a_{max}$	linearity	V_{IN} = 1.33 V_{pp} (nom.)	0.90	-	-	
m		V_{IN} = 1.86 V_{pp} (+3 dB)	0.65	-	-	
V_{Of}/V_{Onom}	signal reduction	higher frequency t_{sig} = 50 ns, $t_r = t_f$ = 1 μs	−1.5	-	-	dB
	switching spikes and offsets in an unused channel with nominal signal in the other channel	R_{source} <= 300 Ω				
V_4, V_6	spikes		−30	-	+30	mV
dV_4, dV_6	offsets		−5	-	+5	mV
dV_4, dV_6	offsets in signal during and after storage time		−18	-	+18	mV
I_{source}	output source current		1.0	-	-	mA
I_{sink}	output sink current		0.4	-	-	mA
$V_{O4,6}$	DC output voltage		-	2.0	-	V
$R_{O4,6}$	output resistance		-	-	100	Ω
sandcastle pulse input						
	12 V sandcastle pulse	SC5 = 0 selectable by I²C-bus				
V_{thHV}	threshold voltage line/field		1.1	1.5	1.9	V
V_{thBG}	threshold voltage burstgate		6.0	7.0	8.0	V
R_{17}	input resistance		30	40	50	kΩ
C_{17}	input capacitance		-	4	8	pF
	5 V sandcastle pulse	SC5 = 1				
V_{thHV}	threshold voltage line/field		1.1	1.5	1.9	V
V_{thBG}	threshold voltage burstgate		3.0	3.5	4.0	V

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670

SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
R_{17}	input resistance		15	20	25	kΩ
C_{17}	input capacitance		-	4	8	pF
t_d	time difference between leading edge of burst gate and internal clamping pulse		-	1	-	µs
t_{BG}	pulse duration of burstgate		3.4	4.0	4.6	µs
SDA, SCL inputs						
f_{SCL}	clock frequency range		0	-	100	kHz
$t_{SU,STA}$	start code set-up		4.7	-	-	µs
$t_{HD,STA}$	start code hold		4	-	-	µs
$t_{SU,STO}$	stop code set-up		4.7	-	-	µs
t_{BUF}	bus free		4.7	-	-	µs
$t_{SU,DAT}$	data set-up		250	-	-	ns
t_{CLKH}	clock pulse HIGH		4	-	-	µs
t_{CLKL}	clock pulse LOW		4.7	-	-	µs
t_r	rise time		-	-	1	µs
t_f	fall time		-	-	0.3	µs

Notes to the characteristics

1. All values specified with V_{VB} = 315 mV (nom), T_{line} = 64.0 µs and $t_{burst\ gate}$ = 4.0 µs unless otherwise stated.
2. The delay time is proportional to $t_{line} + t_{bg/2}$
3. All values specified with $V_{(p-p)}$ = 1.33 V, t_r = 1 µs, t_f = 1 µs, t_{signal} = 1 µs and $t_{burst\ gate}$ = 4 µs

I²C-BUS

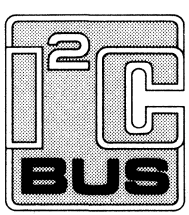
Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	0	0	0

Slave receiver format

S	SLAVE ADDR.	0	A,	SUB ADDR.	A,	DATA BYTE A P

1 or 2 data bytes
auto increment



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Picture signal improvement circuit (PSI) in colour television receivers

TDA4670

Subaddress byte and data byte format

Function	subaddr.	data	byte						
		D7	D6	D5	D4	D3	D2	D1	D0
00 to 0F (note 1)									
Delay line adjust CTI + sandcastle control	10	0	SC5	CTI	D5	D2B	D2A	D1	D/2
Peaking control	11	COR	PEAK	LCF	0	0	0	PCON1	PCON0
Reserved 12 to 1F		X	X	X	X	X	X	X	X
Test data 0	F0	TB07							TB00
F1 to FE (note 2)									
Test data F	FF	TBF7							TBF0

Notes

1. reserved for colour decoders and RGB processors
2. reserved for testing this device

Bit definition

DXX	bits are activating delay line segments Logic 1: delay line segment active Logic 0: delay line segment inactive		
D/2	control of 45 ns delay line segment		
D1	control of 90 ns delay line segment		
D2A,D2B	control of 180 ns delay line segments		
D5	control of 450 ns delay line segment		
CTI	colour transient improvement control Logic 1: CTI-function operative Logic 0: no CTI-function		
SC5	sand castle detector level control Logic 1: 5 V sandcastle pulse Logic 0: 12 V sandcastle pulse		
LCF	peaking frequency response control Logic 1: low centre frequency 2.6 MHz Logic 0: high centre frequency 5.0 MHz		
PEAK DELAY	peaking delay set up Logic 1: peaking delay operative Logic 0: no peaking delay		
PCON0,1	peaking amplitude control		
	PCON1	PCON0	grade of peaking
	0 0 1 1	0 1 0 1	−4.4 dB 0 dB +3.5 dB +6 dB
COR	coering control Logic 1: coering operative Logic 0: coering		

Slave transmitter format is not acknowledged.

General call address is not acknowledged.

After power-on reset the first 7 control bits of the data byte are set to 0 and the 8th bit (LSB) is set to 1.

Subaddresses 00 to 0F are reserved for colour decoders and for RGB processors and are not acknowledged by this device. Only subaddress 10 and 11, each with 8 bits, are acknowledged by thisdevice.

Data registers with subaddress outside the range 00 to 1F are not tested and are therefore forbidden for the user.

Data registers with subaddress F0 to FF may be used to test the IC in the factory. Thus these subaddresses are forbidden for the user. The bits TBx of these registers may be unique for each device.

The bits presented as don't cares (X) are reserved for functions not yet built-in. Their value should not influence any other function in the device. These bits have to be tested on their don't care function if other devices are available which are using these bits. Thus the microcontroller software can be written in such a way that the whole family of circuits can be used with the same address.

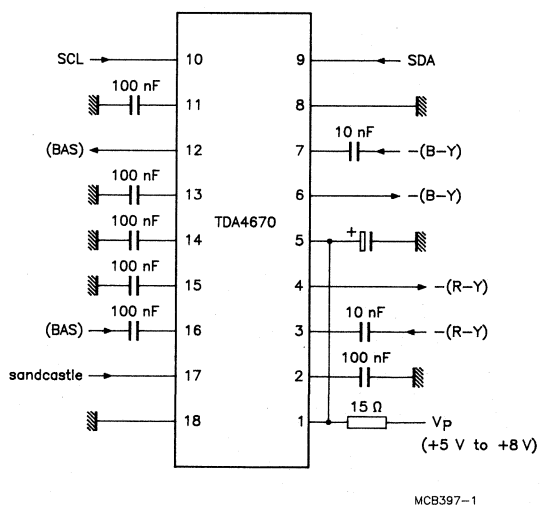


Fig.3 Application circuit.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4680

Video processor, with automatic cut-off and white level control

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two fully-controlled, analog RGB inputs, selected either by fast switch signals or via I²C-bus
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, horizontal and vertical synchronization, cut-off and white level timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Software-based automatic white level control or fixed white levels via I²C-bus
- Cut-off and white level measurement pulses in the last 4 lines of the vertical blanking interval (I²C-bus selection for PAL, SECAM, or NTSC, PAL-M)
- Increased RGB signal bandwidths for progressive scan and 100 Hz operation (selected via I²C-bus)
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting

(continued)

DESCRIPTION

The TDA4680 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	85	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse: H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse: H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24,22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature range	0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4680	28	DIL	plastic	SOT117
TDA4680WP	28	PLCC	plastic	SOT261

Video processor, with automatic cut-off and white level control

TDA4680

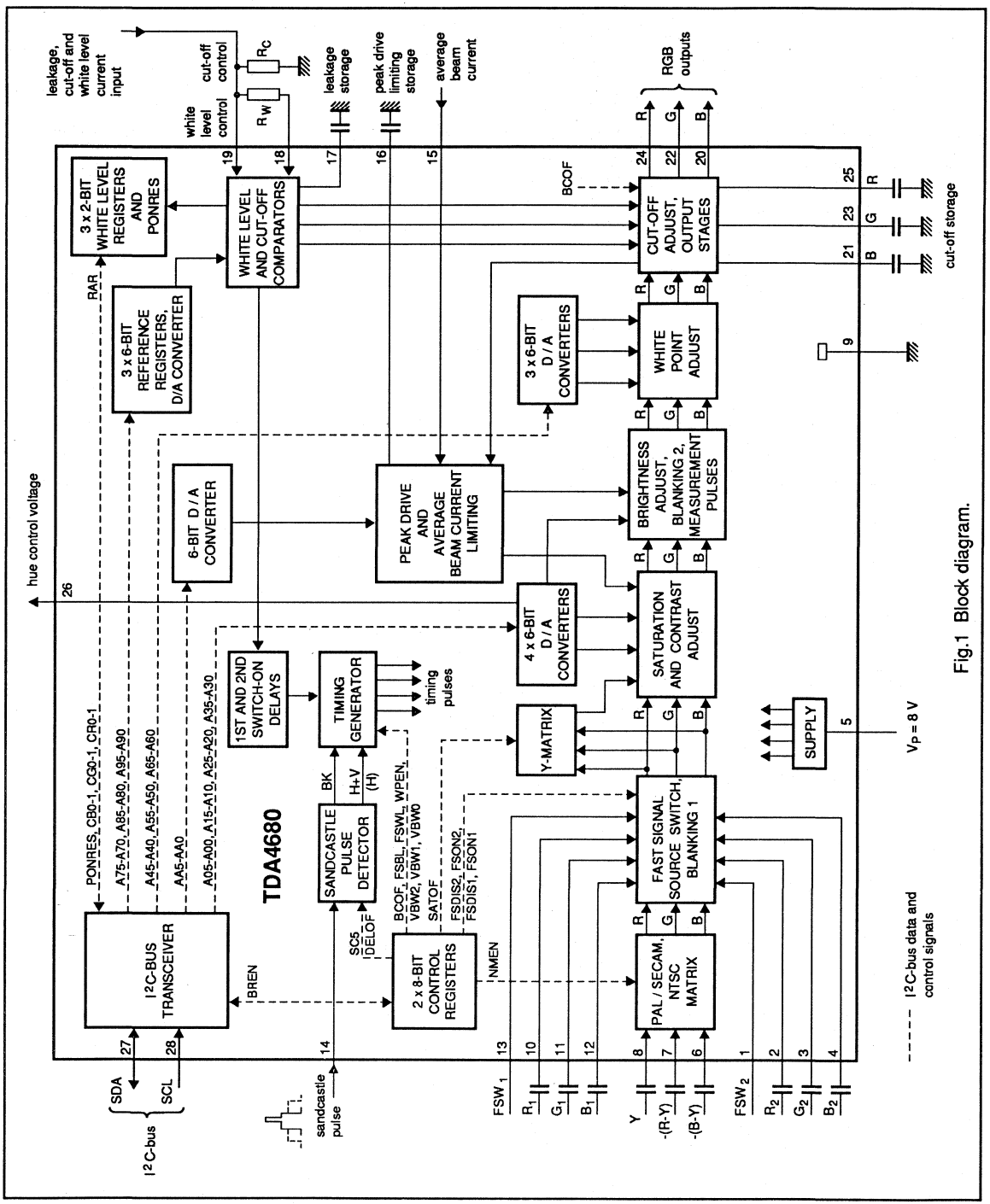


Fig.1 Block diagram.

Video processor, with automatic cut-off and white level control

TDA4680

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	colour difference input -(B-Y)
-(R-Y)	7	colour difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
WI	18	white level measurement input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

PIN CONFIGURATIONS

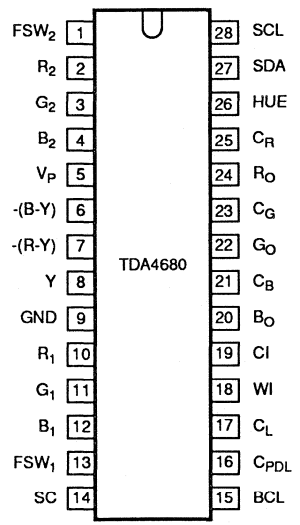


Fig.2(a) Pin configuration for DIL package.

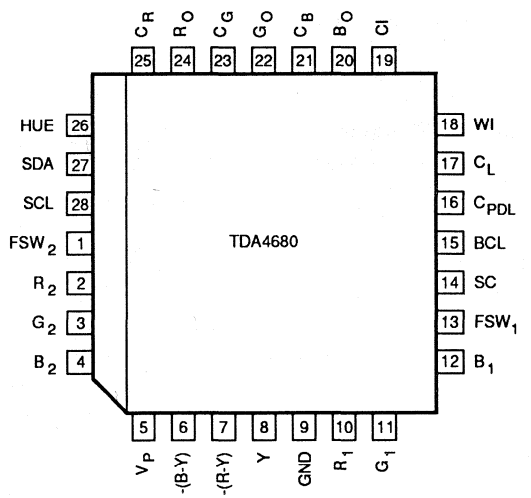


Fig.2(b) Pin configuration for PLCC package.

Video processor, with automatic cut-off and white level control

TDA4680

FEATURES (continued)

- PAL/SECAM or NTSC matrix selection via I²C-bus
- Three adjustable reference voltage levels (via I²C-bus) for automatic cut-off and white level control
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650

DESCRIPTION (continued)

Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator; both inputs are fully-controlled internally . The TDA4680 includes full I²C-bus control of all parameters and functions with automatic cut-off and white level control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

I²C-BUS CONTROL

The I²C-bus transmitter/receiver provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting
- selection of the vertical blanking interval and measurement lines for cut-off and white level control according to transmission standard
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables/disables input clamping pulse delay
- enables/disables white level control
- enables cut-off control/ enables output clamping
- enables/disables full screen white level
- enables/disables full screen black level
- selects either PAL/SECAM or NTSC matrix
- enables saturation adjust/ enables nominal saturation
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- reads the result of the comparison of the nominal and actual RGB signal levels for automatic white level control.

I²C-BUS TRANSMITTER / RECEIVER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits/receives data from the I²C-bus transceiver in the TDA4680 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This consists of the module address, 1000100_2 for the TDA4680, plus the R/WN bit (see Fig.3). When the TDA4680 is a slave receiver

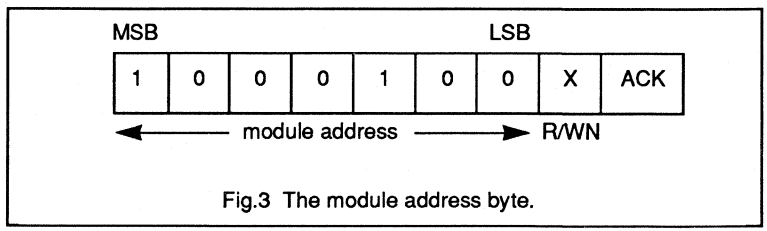


Fig.3 The module address byte.

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD	MSB			DATA BYTE				LSB
	(Hex)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	DELOF	BREN	WPEN	NMEN	VBW2	VBW1	VBW0
Control Register 2	0D	SATOF	FSWL	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

(R/WN = 0) the module address byte is 10001000_2 (88 Hex). When the TDA4680 is a slave transmitter (R/WN = 1) the module address byte is 10001001_2 (89 Hex).

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

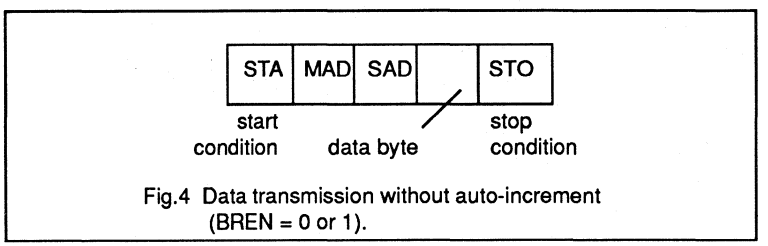


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

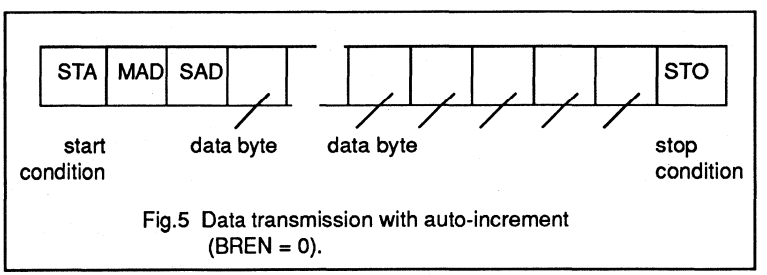


Fig.5 Data transmission with auto-increment (BREN = 0).

Auto-Increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I²C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

If the auto-increment format is

selected, the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5).

All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are acknowledged by the device but neither auto-increment nor any other internal operation takes place.

Sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

VBWx (Vertical Blanking Window):
x = 0, 1 or 2. VBWx selects the vertical blanking interval and positions the measurement lines for cut-off and white level control.

The actual lines in the vertical blanking interval after the start of the V-pulses selected as measurement lines for cut-off and white level control are shown in Table 2.

The standards marked with (*) are for progressive line scan at double the line frequency ($2F_L$), i.e. approximately 31 kHz.

NMEN (NTSC - Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.

WPEN (White Pulse ENable):
0 = white measuring pulse disabled
1 = white measuring pulse enabled.

BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I^2C-bus transceiver does not accept any new data until this data is transferred into the data registers.

DELOF (DELay OFf) delays the leading edge of clamping pulses:
0 = delay enabled
1 = delay disabled.

SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 3).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

FSBL - Full Screen Black Level:
0 = normal mode
1 = full screen black level (cut-off measurement level during full field).

FSWL - Full Screen White Level:
0 = normal mode
1 = full screen white level (white measurement level during full field).

SATOF - SATuration control OFf
0 = saturation control enabled
1 = saturation control disabled, nominal saturation enabled.

Table 2 Cut-off and white level measurement lines

VWB2	VWB1	VWB0	R	G	B	WHITE	STANDARD
0	0	0	19	20	21	22	PAL/SECAM
0	0	1	16	17	18	19	NTSC/PAL M
0	1	0	22	23	24	25	PAL/SECAM (EB)
1	0	0	38, 39	40, 41	42, 43	44, 45	PAL*/SECAM*
1	0	1	32, 33	34, 35	36, 37	38, 39	NTSC*/PAL M*
1	1	0	44. 45	46, 47	48, 49	50, 51	PAL*/SECAM* (EB)

Notes to Table 2
1. The line numbers given are those of the horizontal pulse counts after the start of the vertical component of the sandcastle pulse.
2. * line frequency of approximately 31 kHz.
3. (EB) is extended blanking.

Table 3 Signal input selection by the fast source switches

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 3
Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

I^2C-bus transmitter
(microcontroller read mode)
As an I^2C-bus transmitter, R/WN = 1, the TDA4680 sends a data byte from the status register to the microcontroller. The data byte consists of following bits:
PONRES, CB1, CB0, CG1, CG0, CR1, CR0 and 0, where PONRES is the most significant bit.
PONRES (Power ON RESet) monitors the state of TDA4680's supply voltage:
0 = normal operation
1 = supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage was interrupted).
When PONRES changes state from a logic LOW to a logic HIGH all data and function bits are set to logic LOW.

Table 4 2-bit white level error signals, CX1 and CX0

CX1	CX0	INTERPRETATION
0	0	RAR (Reset-After-Read): no new measurements since last read
1	0	actual (measured) white level *less than* the tolerance range
1	1	actual (measured) white level *within* the tolerance range
0	1	actual (measured) white level *greater than* the tolerance range

2-bit white level error signal
(see Table 4).
CB1, CB0 = 2-bit white level of the *blue* channel.
CG1, CG0 = 2-bit white level of the *green* channel.
CR1, CR0 = 2-bit white level of the *red* channel.

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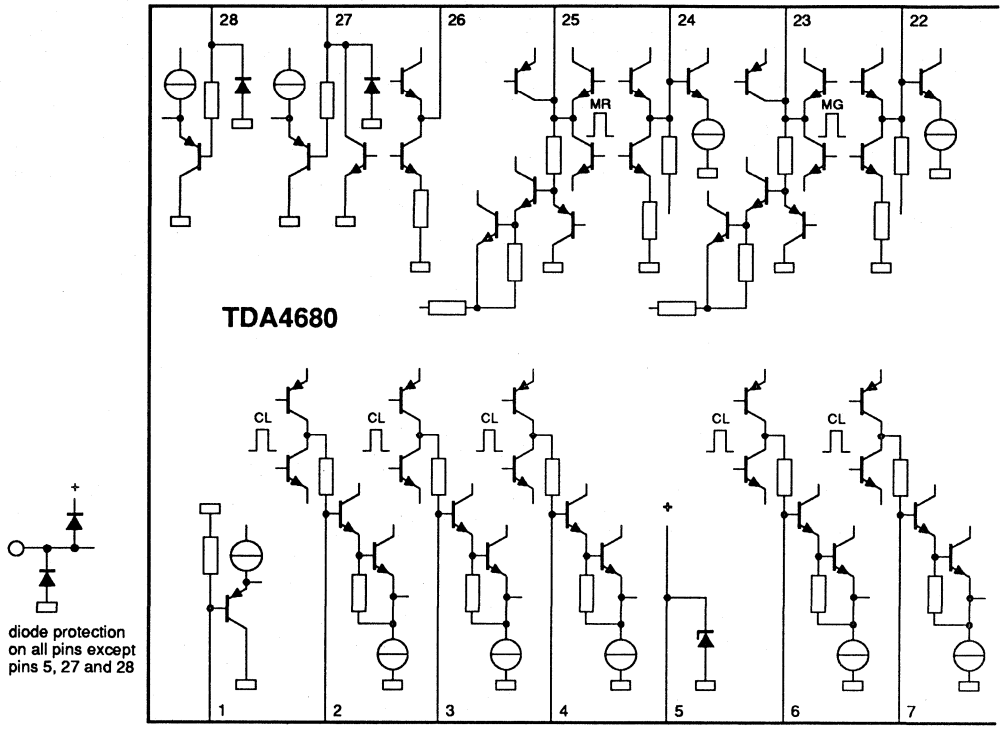

Fig.6(a) Internal circuits (continued in Fig.6b).

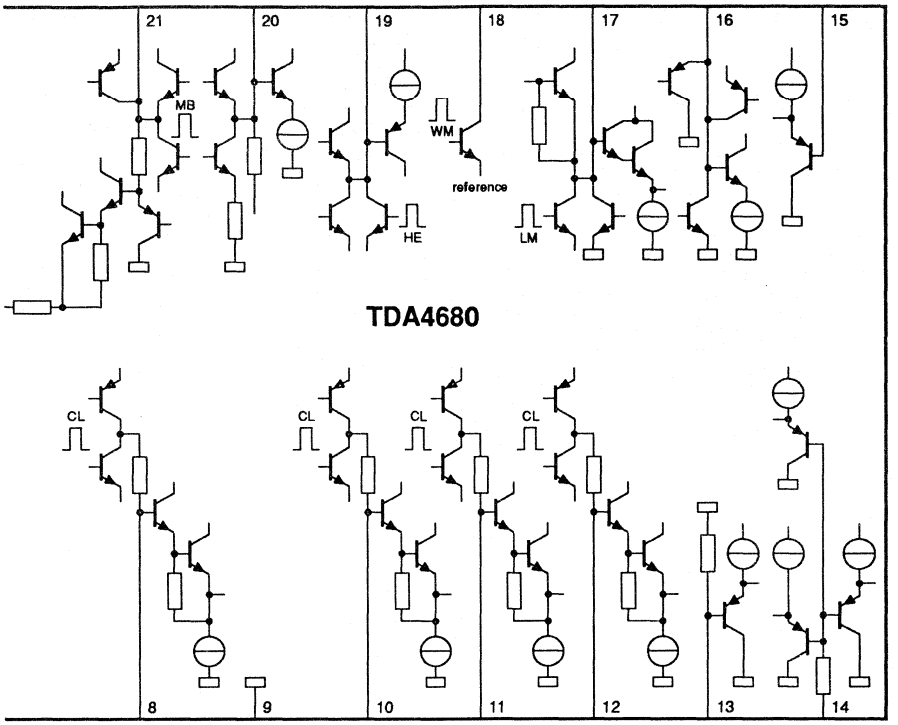

Fig.6(b) Internal circuits (continued from Fig.6a).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	−0.1	V_P	V
	voltage range (pins 14, 15, 18 and 19)	−0.7	V_P + 0.7	V
I_{AV}	current range (pins 20, 22 and 24)	4	−10	mA
I_M	peak current range (pins 20, 22 and 24)	4	−20	mA
I_{18}	input current range	0	2	mA
I_{26}	output current range	0.5	−8	mA
T_{stg}	storage temperature range	−20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

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CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	85	110	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	3.1	–	V
I_8	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (notes 3 and 4)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs (control bits: see table 3)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs (control bits: see table 3)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Saturation adjust acts on internal RGB signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte $2C_{Hex}$ for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at $2C_{Hex}$	–	3	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of brightness range); data byte $3F_{Hex}$ for maximum brightness; data byte 27_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 5. data byte $3F_{Hex}$ for maximum gain data byte 22_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	60	–	%
	decrease of gain	at 00_{Hex}	–	60	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 6.						
$V_{o(b-w)}$	nominal output signals (black-to-white value)		–	2	–	V
	maximum output signals (black-to-white value)		3.2	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	output clamping (BCOF = 1)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	65	110	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 7 and 8						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses		6.3	–	V_P + 0.7	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; note 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 0.7	V
Sandcastle pulse detector						
I_{14}	input current	V_{14} = 0 V	–	–	100	µA
t_d	leading edge delay of the clamping pulse	control bit DELOF = 0	–	1.5	–	µs
		control bit DELOF = 1	–	0	–	µs
t_{BK}	required burst key pulse time	control bit DELOF = 0; normally used with f_L	3	–	–	µs
		control bit DELOF = 1; normally used with $2f_L$	1.5	–	–	µs
n_{pulse}	required horizontal or burst key pulses during vertical blanking interval	e.g. at interlace scan (VWB2 = 0)	4	–	29	
		e.g. at progressive line scan (VWB2 = 1)	8	–	57	
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	6.5	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off and white level control (notes 11, 12 and 13) see Fig.9						
V_{19}	external measurement voltage		–	–	V_P –1.4	V
I_{19}	output current		–	–	–140	µA
	input current		150	–	–	µA
	additional input current	during monitor pulse	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1	–	V_{pdl} –0.7	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	5.0	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	3.0	–	V
data byte 07_{Hex} for red reference level data byte 08_{Hex} for green reference level data byte 09_{Hex} for blue reference level						
ΔV_{19}	difference between V_{MEAS} (cut-off or white level measurement voltage) and V_{REF}	$3F_{Hex}$ (maximum V_{MEAS})	1.5	–	–	V
		20_{Hex} (nominal V_{MEAS})	–	1.0	–	V
		00_{Hex} (minimum V_{MEAS})	–	–	0.5	V
I_{18}	input current	white level measurement	–	–	800	µA
R_{18}	internal resistance	to V_{REF}; $I_{18} \leq 800$ µA	–	100	–	Ω
ΔV_{19}	white level register (measured value within tolerance range)	white level measurement	–	250	–	mV
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	< 3.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hue control (note 14) under I²C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.0	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA
I²C-bus transceiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	input current LOW		–	–	–10	µA
I_{IH}	input current HIGH		–	–	10	µA
t_d	pulse time LOW		4.7	–	–	µs
	pulse time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I²C-bus transceiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	input current LOW		–	–	–10	µA
I_{IH}	input current HIGH		–	–	10	µA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{su;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

   $$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

   NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):

   $$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
   $$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
   $$V_{B-Y}^* = V_{B-Y}$$

   In the matrix equations:
   V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

   V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*$.
4. The vertical blanking interval is selected via the I²C-bus (see Table 2 and Fig.9). Vertical blanking is determined by the vertical component of the sandcastle pulse; this vertical component has priority when it is longer than the vertical blanking interval of the transmission standard.
5. The white potentiometers affect the amplitudes of the RGB output signals including the white measurement pulses.
6. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
7. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.0 V for the burst key pulse.

   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
8. A sandcastle pulse with a maximum voltage equal to (V_P + 0.7 V) is obtained by limiting a 12 V sandcastle pulse.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I²C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. The vertical blanking interval is defined by a V pulse which contains 4 (8) or more H pulses; it begins with the start of the V pulse and ends with the end of the white measuring line. If the V pulse is longer than the selected vertical blanking window the blanking period ends with the end of the complete line after the end of the V pulse. The counter cycle time is 31 (63) H pulses if the V pulse contains more than 29 (57) H pulses. With more than 29 (57) H pulses, the black level storage capacitors will be discharged while all signals are blanked. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 5.0 V, the monitor pulse is switched off and cut-off and white level control are activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

Video processor, with automatic cut-off and white level control

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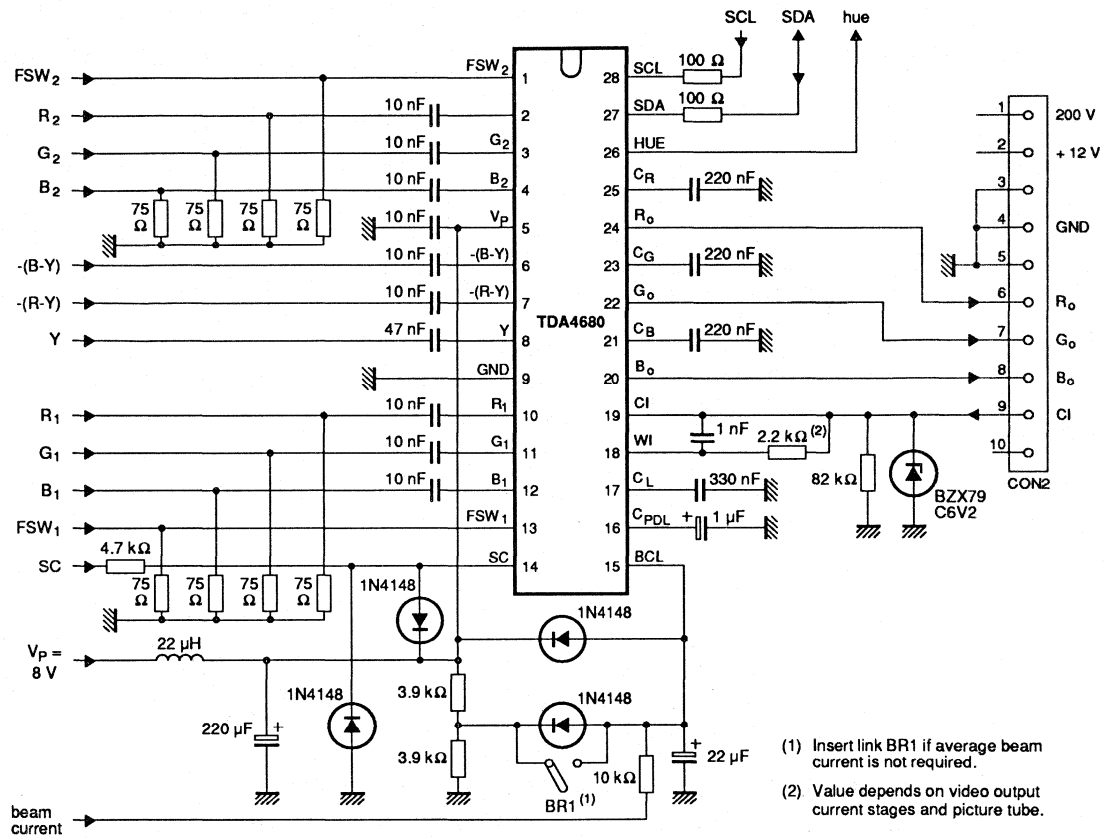

Fig.7 Test and application circuit.

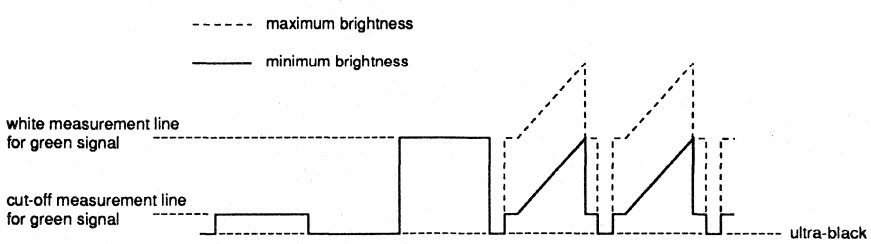

Fig.8 Cut-off and white level measurement pulses.

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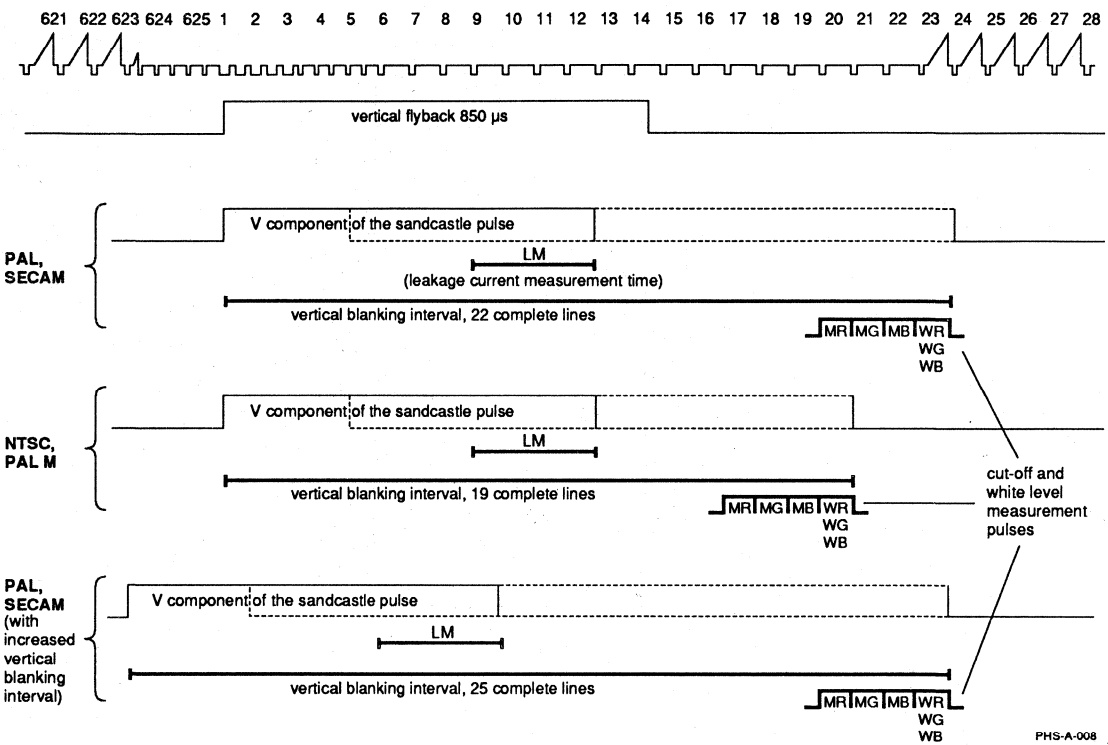

Fig.9 Leakage current, cut-off and white level current measurement timing diagram.

Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4685

Video processor, with automatic cut-off control

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Increased RGB signal bandwidths
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650

DESCRIPTION

TDA4685 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers. *(continued)*

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse: H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse: H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24,22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature range	0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4685	28	DIL	plastic	SOT117

Video processor, with automatic cut-off control

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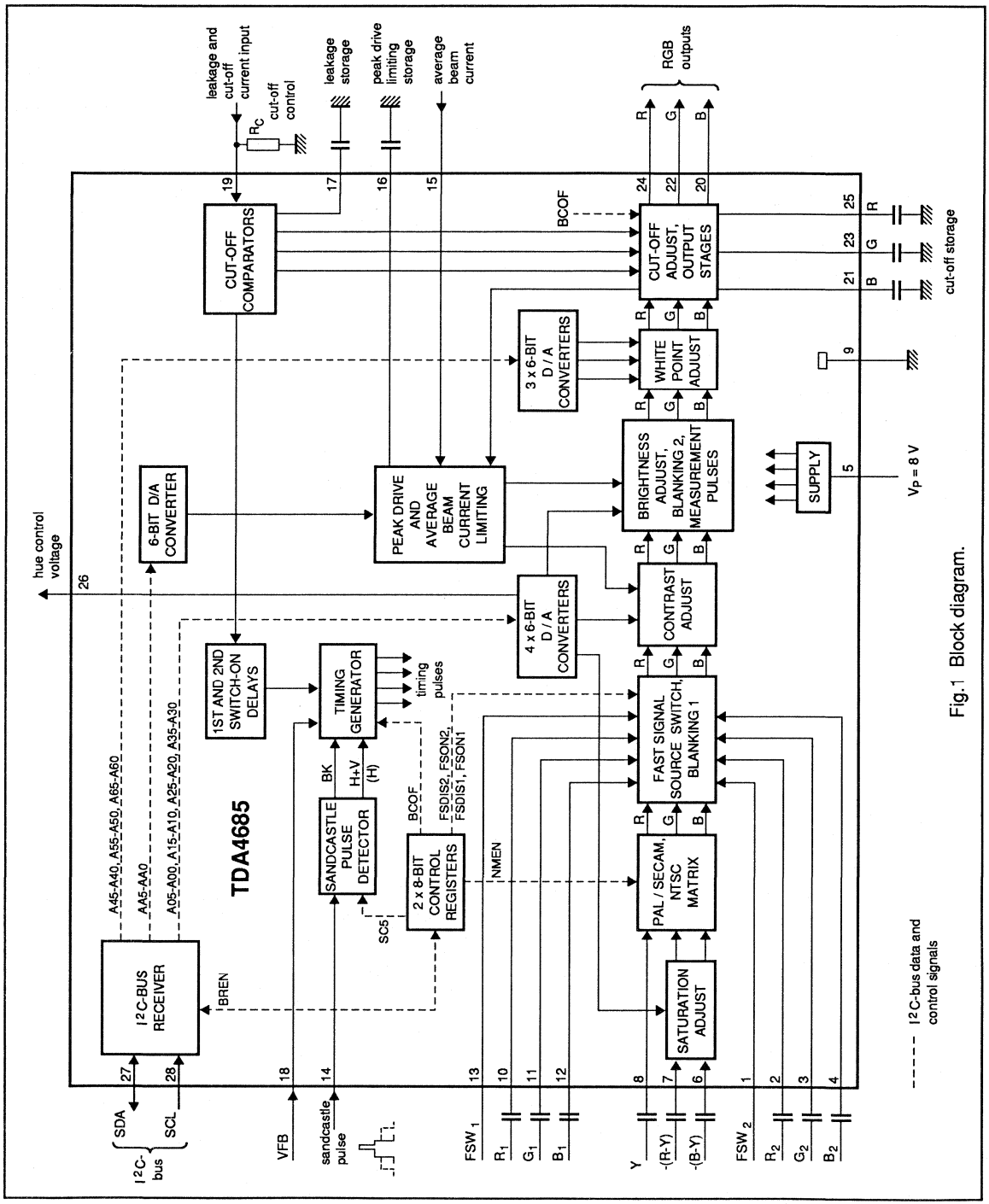

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	colour difference input -(B-Y)
-(R-Y)	7	colour difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

DESCRIPTION (continued)

Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4685 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4685 then the I^2C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not generated
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

PIN CONFIGURATION

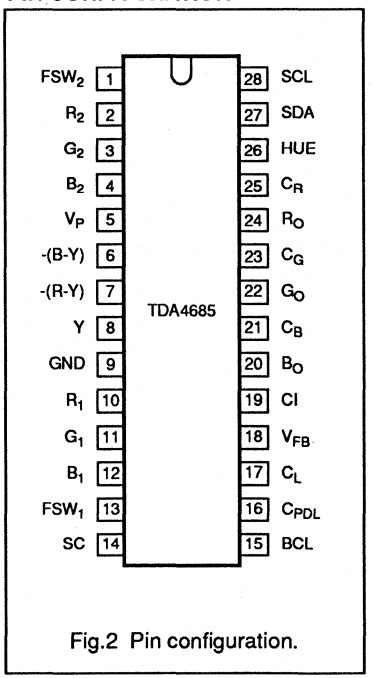

Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control control/ enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of the I²C-bus command with the vertical blanking interval.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA4685 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4685 is a slave receiver (R/WN = 0), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

Auto-increment

Auto-increment format enables quick slave receiver initialization by one transmission, when the I²C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

If auto-increment format is selected the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5). All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device.

The sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

NMEN (NTSC - Matrix ENable):
- 0 = PAL/SECAM matrix
- 1 = NTSC matrix.

BREN (Buffer Register ENable):
- 0 = new data is enabled as soon as it is received
- 1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I²C-bus transceiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):
- 0 = 3-level sandcastle pulse
- 1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

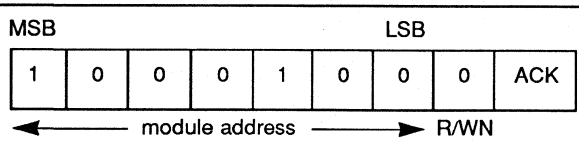

Fig.3 The module address byte.

Video processor, with automatic cut-off control

TDA4685

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD	MSB			DATA BYTE				LSB
	(Hex)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control Register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

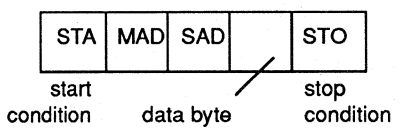

Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

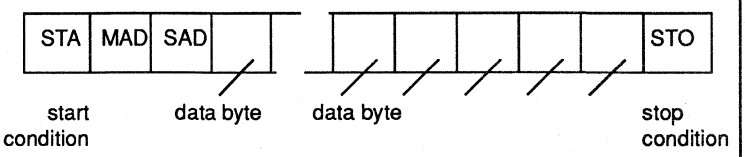

Fig.5 Data transmission with auto-increment (BREN = 0).

Table 2 Signal input selection by the fast source switches

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

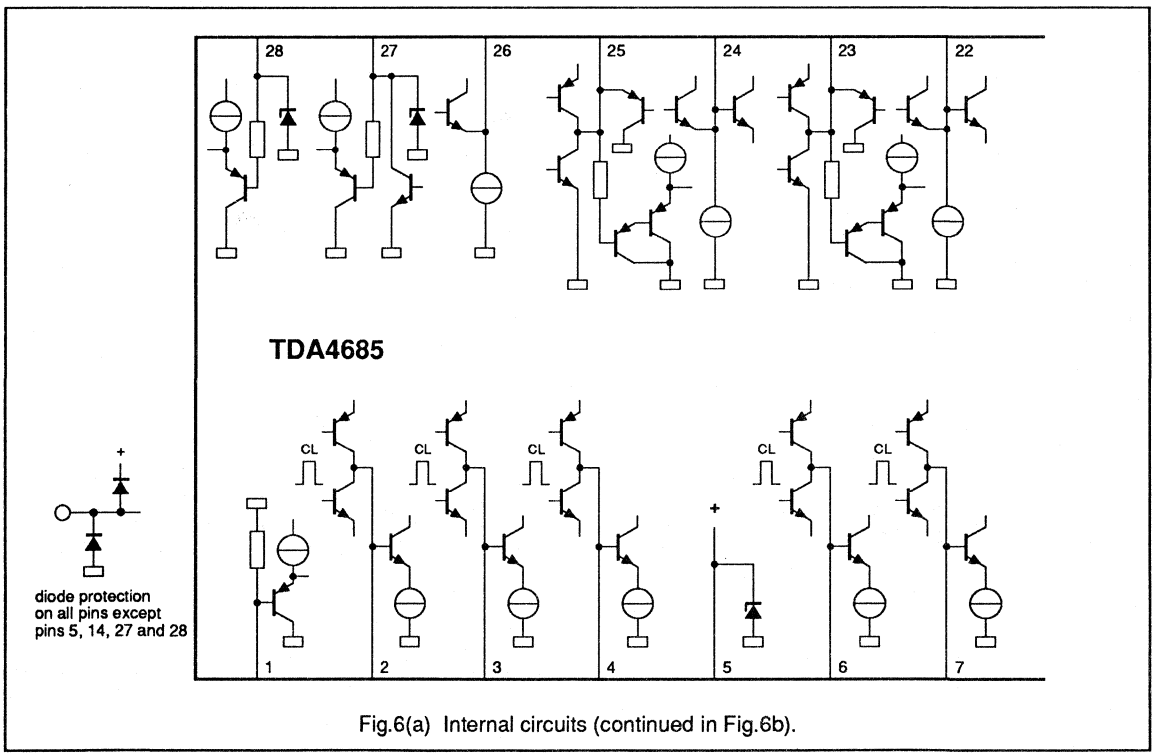

Fig.6(a) Internal circuits (continued in Fig.6b).

Video processor, with automatic cut-off control

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	–0.1	V_P	V
	voltage range (pins 15, 18 and 19)	–0.7	V_P + 0.7	V
V_{14}	sandcastle pulse voltage range	–0.7	V_P + 5.8	V
I_{AV}	current range (pins 20, 22 and 24)	4	–10	mA
I_M	peak current range (pins 20, 22 and 24)	4	–20	mA
I_{26}	output current range	0.6	–8	mA
T_{stg}	storage temperature range	–20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

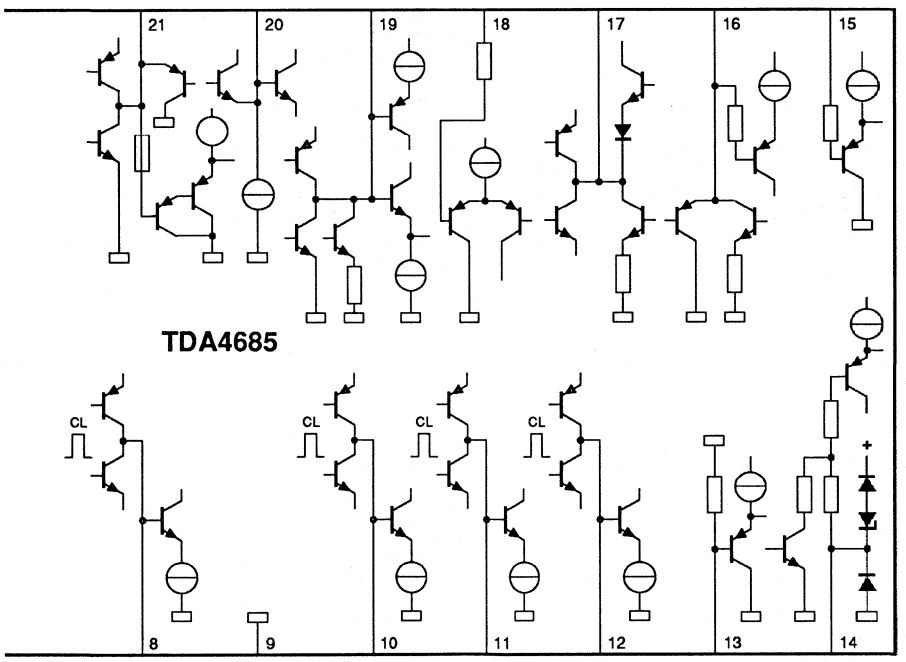

Fig.6(b) Internal circuits (continued from Fig.6a).

Video processor, with automatic cut-off level control

TDA4685

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (see note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Saturation adjust acts on -(R-Y) and -(B-Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte 22_{Hex} for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5.0	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of maximum brightness); data byte $3F_{Hex}$ for maximum brightness; data byte 26_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	V_P + 5.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 5.8	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	1.5	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open (note 8)	–	5.0	–	V
I_{18}	input current		–	–	5	µA
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	cut-off measurement voltage (V_{MEAS})		–	–	V_P –1.4	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I²C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1 (note 14)	–	V_{pdl} –0.1	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} and V_{REF}		–	1.0	–	V
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	2.5	–	V
Hue control (note 14) under I²C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
t_d	pulse time LOW		4.7	–	–	μs
	pulse time HIGH		4.0	–	–	μs
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
I²C-bus receiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
$t_{su;DAT}$	data set-up time		0.25	–	–	μs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

$$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

NTSC signals are matrixed by the equations (hue phase shift of −5 degrees):

$$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
$$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
$$V_{B-Y}^* = V_{B-Y}$$

In the matrix equations:
V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

$V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*$.

4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent from V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9(b). In this case the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open or connected to V_P.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitoring pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

Video processor, with automatic cut-off control

TDA4685

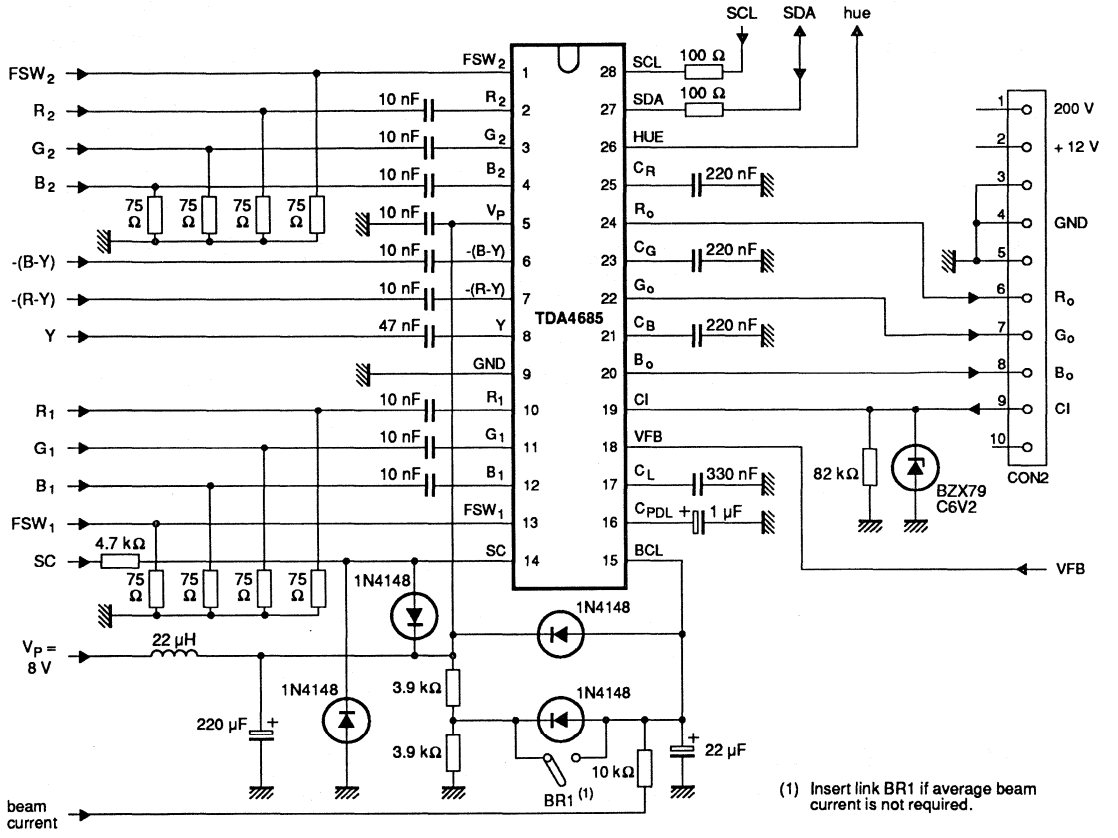

Fig.7 Test and application circuit.

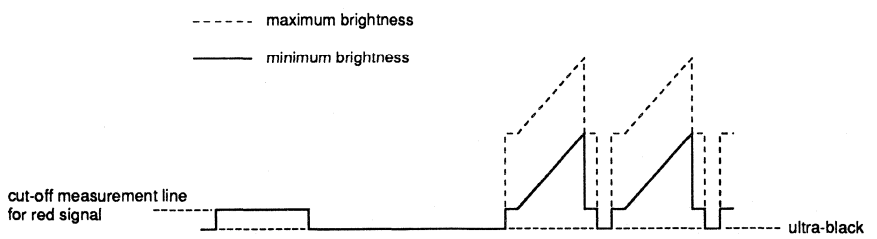

Fig.8 Cut-off measurement pulse.

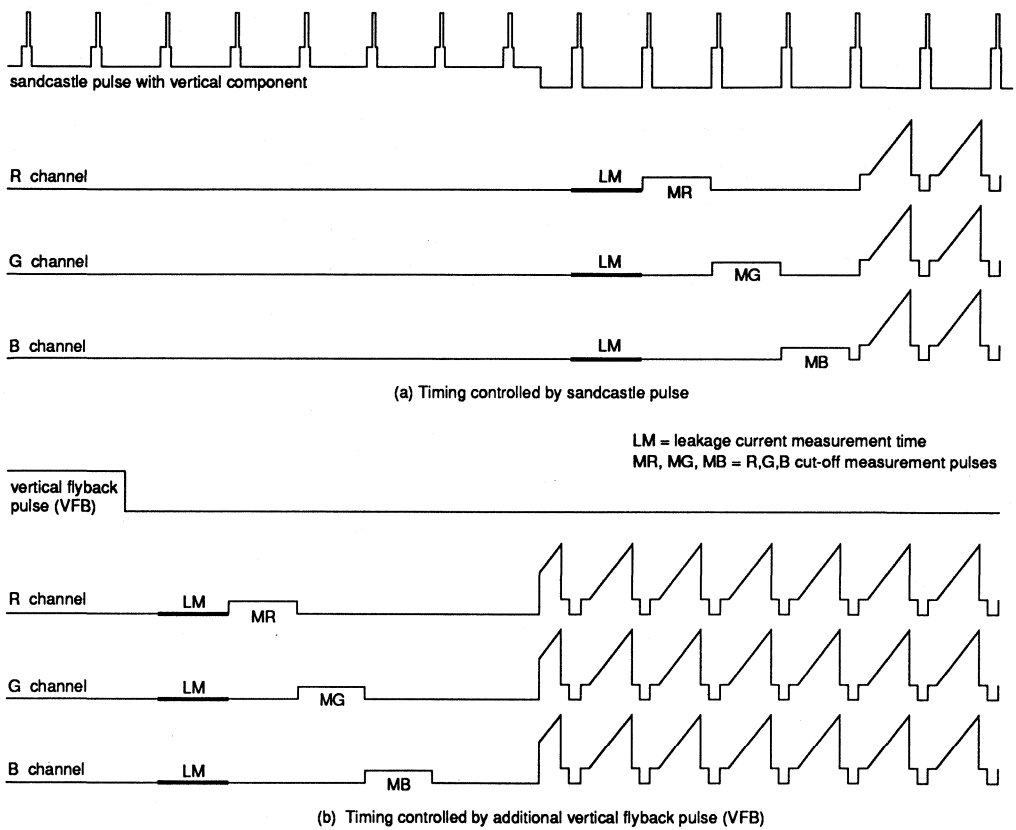

Fig.9 Leakage and cut-off current measurement timing diagram.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4710H

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

GENERAL DESCRIPTION

The TDA4710 is an integrated circuit for VHS PAL, SECAM ME or NTSC chrominance and synchronization processing in (S) VHS cassette recorders.

FEATURES

Chrominance

- 4.43/3.58 MHz chrominance output with colour-killer for record, electronic-to-electronic (e.g. direct to a SCART connector) and playback modes
- 627/629 kHz chrominance output with colour-killer
- 8.86/7.16 MHz crystal oscillator (voltage controlled oscillator in record mode and fixed frequency oscillator during playback mode)
- Separate automatic gain control (AGC) for record and playback (two channel hold capacity)
- Burst pre-emphasis/de-emphasis selection input (for NTSC)
- Subcarrier phase rotion and head-pulse input
- PAL error detector and correction circuit for longplay multispeed (LP MS)
- Test picture generator

Synchronization

- Phase-locked loop (PLL) with coincidence detector and mute output stage for the line frequency
- Sandcastle output signal

Additional features

- Standard/longplay multispeed mode selection
- 32 µs SKEW detector and output stage
- Selectable burst pulse insert for longplay feature mode (PAL)
- NTS to PAL-M transcoder at playback

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4710H	48	QFP48	plastic	SOT196A

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
V_{17-19}	digital part		-	5	-	V
V_{41-43}	analog part		-	5	-	V
$I_{17}+I_{41}$	supply current		-	45	-	mA
V_{20-19}	sync input signal slicing level		-	1.5	-	V
V_{23-19}	sandcastle output signal		-	4	-	V
V_{16-19}	test picture output signal		-	1	-	V
$V_{31(p-p)}$	4.43/3.58MHz subcarrier output (peak-to-peak value)		-	400	-	mV
Record (PAL) note 1						
$V_{48(p-p)}$	composite video input signal (peak-to-peak value)		-	450	-	mV
$V_{44(p-p)}$	AGC chrominance input signal (peak-to-peak value)		10	-	210	mV
$V_{37(p-p)}$	627 kHz subcarrier mixer output signal (peak-to-peak value)		-	1.06	-	V
Playback (PAL) note 1						
$V_{42(p-p)}$	627kHz chrominance input signal (peak-to-peak value)		-	24	-	mV
$V_{8(p-p)}$	4.43MHz chrominance output signal (peak-to-peak value)		-	420	-	mV
Playback (SECAM) note 2						
$V_{8(p-p)}$	chrominance output signal (peak-to-peak value)		-	200	-	mV

Notes to the quick reference data

1. PAL signal (red) with 75% saturation, –9 dB bandpath (pins 44 to 46), 6 dB trap pins 2 to 4 and chrominance-to-burst ratio of 2.2:1.
2. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the signal frequency.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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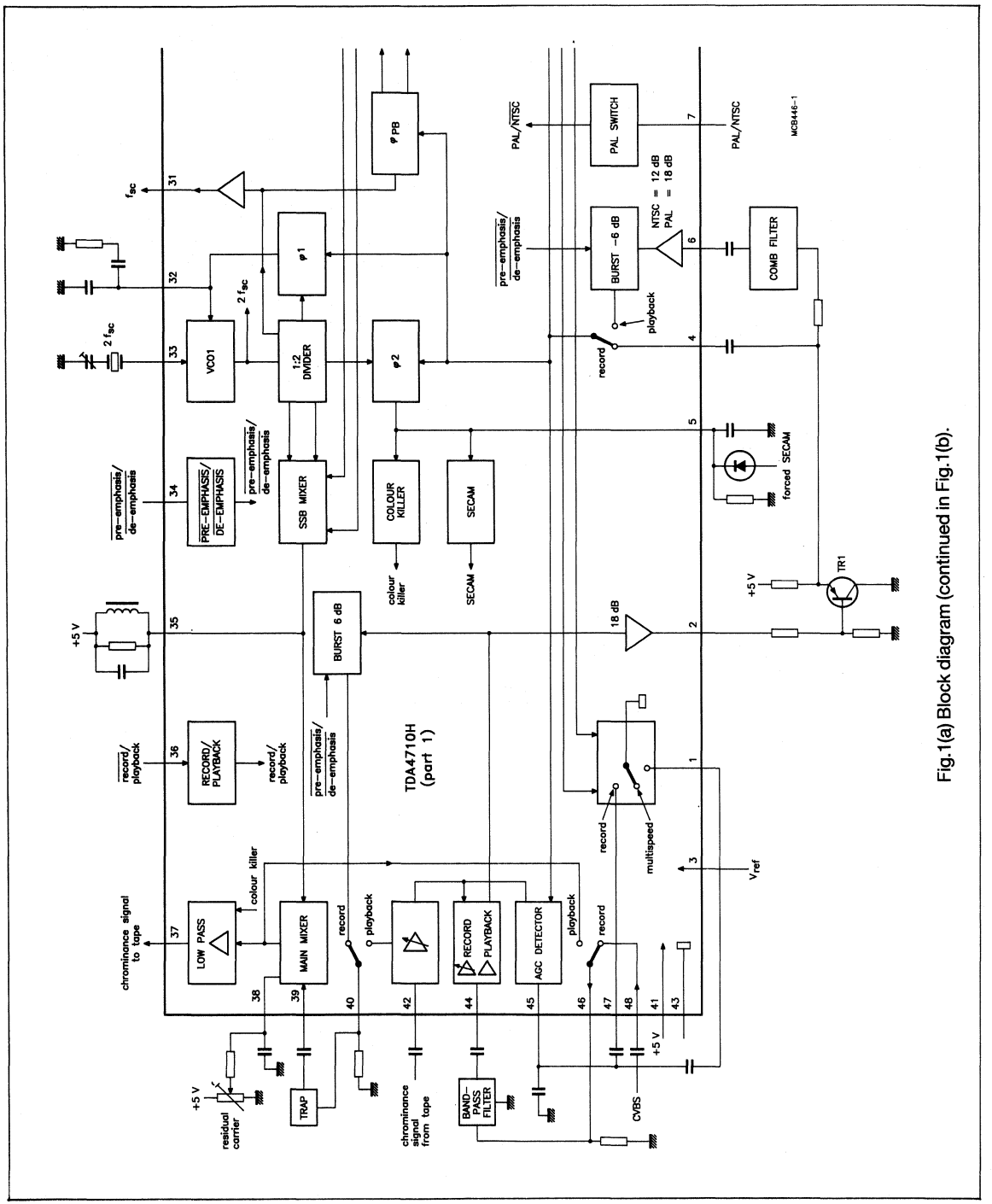

Fig.1(a) Block diagram (continued in Fig.1(b).

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

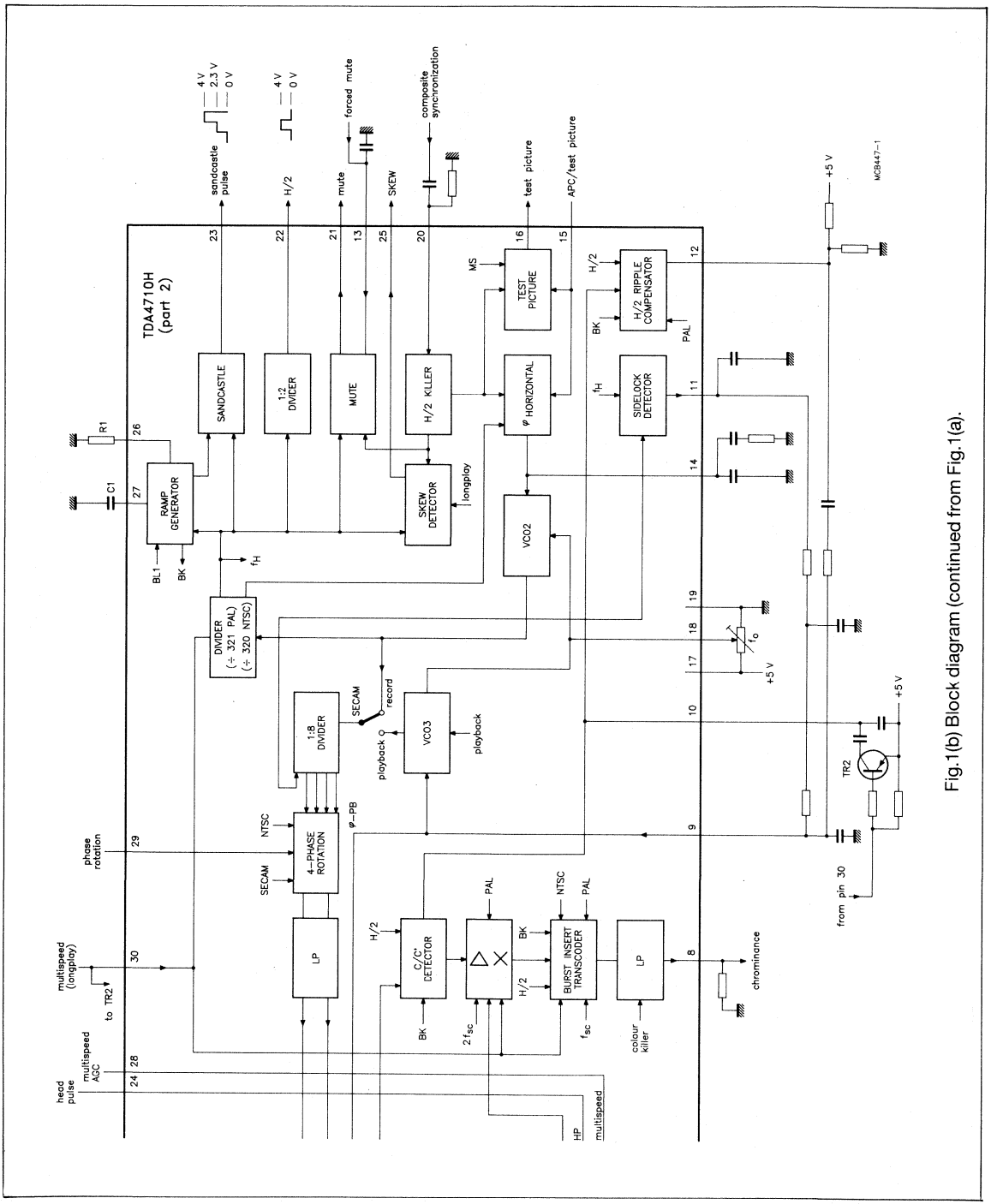

Fig.1(b) Block diagram (continued from Fig.1(a).

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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PINNING

PIN	DESCRIPTION
1	connection for an external capacitor, required for the AGC channel 2
2	chrominance/AGC output (record/playback)
3	reference voltage input
4	chrominance input (record)
5	colour-killer input/output, select colour ON, OFF or SECAM-BG mode
6	chrominance de-emphasis input (playback)
7	PAL/NTSC switch
8	chrominance output (to TV)
9	voltage controlled oscillator 3 (playback)
10	PAL sequence error detector output
11	sidelock detector output (playback)
12	H/2 ripple compensation output (playback)
13	connection for an external capacitor, required for the mute timing constant
14	voltage controlled oscillator 2
15	automatic phase correction (APC)/test picture input switch
16	test picture output
17	supply voltage, digital part
18	frequency adjustment for voltage controlled oscillator 2 and 3
19	ground, digital part
20	synchronization input
21	mute detector output
22	H/2 output
23	sandcastle pulse output
24	head-pulse input

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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PINNING (continued)

PIN	DESCRIPTION
25	SKEW detector output
26	sawtooth generator timing resistor
27	sawtooth generator timing capacitor
28	multispeed input switch (AGC)
29	phase rotation control input
30	multispeed input switch (longplay)
31	4.43/3.58 MHz subcarrier output
32	voltage controlled oscillator 1
33	crystal oscillator (8.86/7.16 MHz)
34	burst de-emphasis/pre-emphasis input switch
35	subcarrier resonance input (5.06 MHz, PAL; 4.21 MHz, NTSC)
36	record/playback input switch
37	627/629 kHz chrominance output signal to tape
38	main mixer balance capacitor
39	main mixer input
40	chrominance output signal
41	supply voltage, analog part
42	chrominance input signal from tape
43	ground, analog part
44	chrominance/AGC input (playback/record)
45	connection for an external capacitor, required for the AGC timing constant
46	chrominance selector output
47	connection for an external capacitor, required for the AGC channel 1
48	composite video blanking signal (CVBS) input

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	supply voltage				
V_{17-19}	digital part		-	6	V
V_{41-43}	analog part		-	6	V
	input voltage				
V_{13-19}			1	V_P	V
V_{18-19}			0	4	V
V_n	other voltages		0	V_P	V
	output currents				
$-I_{2,8,37,40,46}$			-	2	mA
$-I_{21,22,31}$			-	1	mA
$-I_{23}$			-	1	mA
$I_{1,25,47}$	other currents		-	3	mA
T_{amb}	operating ambient temperature range		0	70	°C
T_{stg}	storage temperature range		–25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$R_{th\ j-a}$	junction-to-ambient		-	92	K/W

Table 1 Abbreviations used in the characteristics tables

ABBREVIATION	DESCRIPTION
f_{sc}	chrominance sub-carrier frequency: PAL, 4.433619 MHz; NTSC, 3.579545 MHz
f_H	line frequency: PAL, 15.625 kHz; NTSC, 15.73426 kHz
LP	longplay mode: PAL, 1.17 cm/s; NTSC, 1.667 cm/s
N x f_H	PAL: 40.125 x f_H = 626.953 kHz NTSC: 40 x f_H = 629.370 kHz
MS	multispeed mode
V_T	temperature voltage (26 mV at 25 °C) generated at the emitter follower
I_C	collector current
C	PAL chrominance signal
C' (conjugate)	Complex PAL chrominance signal

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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CHARACTERISTICS

V_P = 5 V; V_{ref} = 1.4 V; burstkey duration = 4.0 µs; VCO 1 frequency = 4.433619/3.579545 MHz (PAL/NTSC) at pin 31 during playback mode; VCO 2 frequency = 15.625/1573426 kHz (PAL/NTSC) at pin 16 during test picture mode; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
	supply voltage range					
$V_P = V_{17-19}$	digital		4.5	5.0	5.5	V
$V_P = V_{41-43}$	analog		4.5	5.0	5.5	V
$V_{ref} = V_{3-43}$	reference input voltage		1.3	1.4	1.5	V
	input current without load					
I_{17}	digital		-	31	38	mA
I_{41}	analog		-	14	17	mA
PAL/NTSC SWITCH						
	input voltage					
V_{7-43}	PAL		3	-	V_P	V
V_{7-43}	NTSC		0	-	1.5	V
$\pm I_7$	input current		-	-	50	µA
RECORD/PLAYBACK SWITCH						
	input voltage					
V_{36-43}	record mode		0	-	3	V
V_{36-43}	playback mode		3.5	-	V_P	V
$\pm I_{7,36}$	input current		-	-	50	µA
COLOUR-KILLER (see note 1)						
	input voltage					
V_{5-43}	colour OFF		0	-	1	V
V_{5-43}	colour ON	no SECAM	2.5	-	3	V
V_{5-43}	SECAM ON (colour ON)		3.5	-	4.5	V
Record mode (see note 2)						
CONTROLLED CHROMINANCE AMPLIFIER SIGNAL						
$V_{48(P-p)}$	composite video signal input (peak-to-peak value)		-	450	-	mV
R_{48-43}	input resistance		14	20	26	kΩ
V_{48-43}	DC input voltage		-	2	-	V
$V_{40(p-p)}$	controlled output signal (peak-to-peak value)		-	335	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{40-43}	DC output voltage		-	3.1	-	V
BURST PRE-EMPHASIS						
	input voltage pre-/de-emphasis					
V_{34-43}	ON		0	-	0.8	V
V_{34-43}	OFF		1.5	-	V_P	V
$\pm I_{34}$	input current		-	-	50	µA
ΔV_{37-43}	burst pre-emphasis		5	6	7	dB

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE SELECTOR OUTPUT						
$V_{46(p-p)}$	output signal (peak-to-peak value)		-	450	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
CHROMINANCE INPUT SIGNAL						
$V_{44(p-p)}$	input signal (peak-to-peak value)		10	106	200	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V
AGC OUTPUT						
	chrominance output	note 4				
$V_{2(p-p)}$	PAL, NTSC		-	840	-	mV
$V_{2(p-p)}$	SECAM		-	290	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
PHASE SYNC						
	chrominance input signal (peak-to-peak value)					
$V_{4(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{4(p-p)}$	SECAM	note 4	-	145	-	mV
R_{4-43}	input resistance		14	20	26	kΩ
V_{4-43}	DC input voltage		-	2	-	V
627/629 kHz MIXER						
$V_{39(p-p)}$	input signal (peak-to-peak value)		-	335	-	mV
R_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC level		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{37(p-p)}$	PAL, NTSC		-	1.06	-	V
$V_{37(p-p)}$	SECAM	note 4	-	365	-	mV
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
	signal suppression					
α_{37}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{37}		f_{sc}	40	-	-	dB
α_{37}		$2 \times N \times f_H$	30	-	-	dB
α_{37}		$3 \times N \times f_H$	35	-	-	dB
α_{37}		colour OFF	40	-	-	dB
CHROMINANCE OUTPUT						
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM	note 2	-	150	-	mV
V_{8-43}	DC output voltage		-	1.8	-	V
α_{CK}	signal suppression	colour OFF	35	-	-	dB

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sc} PLL AND VC01						
V_{32-43}	DC voltage		-	2.7	-	V
V_{33-43}	DC voltage		-	1.8	-	V
R_{33-43}	input resistance		300	-	-	Ω
R_{VCO1}	crystal resistance	series	-	70	-	Ω
C_{33-43}	input capacitance		-	10	-	pF
Δf	oscillator lock-in frequency range	note 5	-	500	-	Hz
$\pm\Delta\varphi$	static phase error between reference and burst signal	Δf = 400 Hz	-	5	-	deg
TC	oscillator temperature coefficient		-	-	3	Hz/K
Playback mode (see notes 2 and 6)						
CHROMINANCE AGC						
$V42_{(p-p)}$	input signal (peak-to-peak value)		4.8	24	48	mV
R_{42-43}	input resistance		7	10	13	kΩ
V_{42-43}	DC input voltage		-	2.4	-	V
$V_{40(p-p)}$	output signal (peak-to-peak value)		-	237	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	kΩ
V_{40-43}	DC output voltage		-	2.3	-	V
4.43/3.58 MHz MIXER						
V_{39-43}	input signal		-	237	-	mV
V_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC input voltage		-	1.6	-	V
$V_{46(p-p)}$	output signal (peak-to-peak value)	note 7	-	150	-	mV
R_{46-43}	output resistance	note 3	-	V_T/I_C	-	Ω
	signal suppression	note 8				
α_{46}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - (2 \times N \times f_H)$	30	-	-	dB
CHROMINANCE AMPLIFIER						
$V_{44(p-p)}$	input signal (peak-to-peak value)		-	53	-	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE DE-EMPHASIS						
	input signal (peak-to-peak value)					
$V_{6(p-p)}$	PAL		-	53	-	mV
$V_{6(p-p)}$	NTSC		-	106	-	mV
R_{6-43}	input resistance		3.5	5.0	6.5	kΩ
V_{6-43}	DC input voltage		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM		-	150	-	mV
ΔV_{8-43}	burst de-emphasis	$V_{34-43} \leq 0.8$ V	–4.5	–5.5	–6.5	dB
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{8-43}	DC output voltage		-	1.8	-	V
AGC CAPACITOR SWITCH $V_{28-43} \leq 1.5$ V; see note 9						
$I_{1,47-43}$	saturation voltage	$I_{1,47} = 1$ mA	-	-	500	mV
	headpulse input voltage	conductive				
V_{24-43}		pin 47	-	-	1.5	V
V_{24-43}		pin 1	3	-	-	V
V_{24-23}	input threshold voltage for blanking and burstkey suppression	note 10	1.5	2.5	3.0	V
$\pm I_{24}$	input current		-	-	50	μA
MULTI-SPEED AGC INPUT						
V_{28-43}	input voltage	normal mode; note 9	0	-	1.5	V
	input voltage for picture search					
V_{28-43}	normal sync		2	-	3	V
V_{28-43}	super sync		3.5	-	V_P	V
$\pm I_{28}$	input current		-	-	50	μA
PLAYBACK PHASE CONTROL - VCO3						
V_{9-43}	PLL DC voltage	locked	-	2.5	-	V
R_9	source resistance during burstkey suppression		-	40	-	kΩ
G	loop gain		-	800[3]	-	s
Δf	oscillator deviation with respect to f_{sc}		-	76	-	kHz/V
Δf	pull-in range with respect to f_{sc}		38	-	-	kHz

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL SEQUENCE ERROR DETECTION						
	output voltage	see note 11				
V_{10-43}	HIGH		3.2	-	-	V
V_{10-43}	LOW		-	-	1.0	V
I_{10}	output current during burstkey		-	100	-	μA
$-\Delta I_{10}$	demodulated burst	polarity equal to H/2 signal	-	100	-	μA
$-\Delta I_{10}$	demodulated burst	polarity unequal to H/2 signal	-	100	-	μA
SIDELOCK DETECTOR						
$\pm I_{11}$	output current	sidelock detection	-	300	-	μA
t_p	pulse duration		-	64	-	μs
H/2 RIPPLE COMPENSATION						
$\pm I_{12}$	output current during burstkey		-	150	-	μA
V_{12-43}	DC range for linear operation		1.8	-	3.2	V
VC02 AND VCO3 f_O FREQUENCY CONTROL						
V_{18-43}	DC voltage		-	2	-	V
	nominal frequency					
f_{PAL}	PAL		-	5.016	-	MHz
f_{NTSC}	NTSC		-	4.208	-	MHz
$-I_{18}$	input current		-	100	-	μA
APC/TEST PICTURE (see note 12)						
	input voltage					
V_{15-43}	APC ON		0	-	1.4	V
V_{15-43}	APC OFF	test picture with white signal	2.7	-	3.4	V
V_{15-43}	APC OFF	test picture with white signal	4.3	-	V_P	V
$\pm I_{15}$	input current		-	-	50	μA
N x f_H PLL (VC02)						
V_{14-43}	PLL DC voltage	locked	-	1	-	V
R_{14-43}	source resistance during sync pulse		-	40	-	kΩ
G	loop gain		-	380	-	10^3/s
Δf	oscillator deviation related to f_H		-	900	-	Hz/V
Δf	pull-in range related to f_H		800	-	-	Hz

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part						
TEST PICTURE OUTPUT (see note 13)						
	output voltage					
V_{16-19}	white level		-	2.1	-	V
V_{16-19}	black level		-	1.4	-	V
V_{16-19}	sync level		-	1.1	-	V
V_{16-19}	super sync level		-	-	0.25	V
R_{16-19}	source resistance		-	10	-	kΩ
SYNC INPUT SIGNAL						
V_{20-19}	sync input voltage		2.2	4.0	V_P	V
H/2 OUTPUT						
	output voltage					
V_{22-19}	HIGH	$-I_{22} = 0.5$ mA	2.5	-	-	V
V_{22-19}	LOW	$-I_{22} = 0.5$ mA	-	-	0.8	V
SANDCASTLE OUTPUT (see note 10)						
	output voltage					
V_{23-19}	LOW	$I_{23} = 1$ mA	-	-	0.5	V
V_{23-19}	MEDIUM	$-I_{23} = 0.5$ mA	2.0	2.3	2.7	V
V_{23-19}	HIGH	$-I_{23} = 1$ mA	3.75	4.0	-	V
BURSTKEY STAGE (see note 14)						
R_{26-19}	resistor R1		-	47	-	kΩ
t_p	burstkey pulse duration		-	4	-	µs
HEAD-PULSE INPUT FOR 4 PHASE ROTATION (see note 15)						
	input voltage					
V_{29-19}	channel 1		0	-	1.5	V
V_{29-19}	channel 2		3	-	V_P	V
$\pm I_{29}$	input current		-	-	50	µA
LP MS INPUT (see note 16)						
	input voltage					
V_{30-19}	normal mode		0	-	1.5	V
V_{30-19}	LPS MG		2	-	3	V
V_{30-19}	LPS MS	auto-burst				
V_{30-19}	NTSC, PAL-M	insertion	3.5	-	V_P	V
		transcoding	3.5	-	V_P	V
SEARCH CONTROL (SKEW) (see note 17)						
	output voltage					
V_{25-19}	LOW	$I_{25} = 0.5$ mA	-	-	0.8	V
V_{25-19}	HIGH	$-I_{25} = 20$ µA	4	-	-	V

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part (continued)						
MUTE FUNCTION						
	detector output voltage					
V_{21-19}	LOW	N x f_H; PLL locked, I_{21} = 0.5 mA	-	-	0.8	V
V_{21-19}	HIGH	N x f_H; PLL unlocked, I_{21} = 0.5 mA	2.5	-	-	V
	mute voltage					
V_{13-19}	LOW		3.5	-	-	V
V_{13-19}	HIGH	active	-	-	1.5	V
V_{13-19}	forced mute		1	-	1.5	V
f_{sc} SUB-CARRIER OUTPUT						
V_{31-19}	output signal		-	400	-	mV
R_{31-19}	output resistance		-	V_T/I_C	-	Ω
V_{31-19}	DC output voltage		-	1.2	-	V

Notes to the characteristics

1. SECAM-ON switching voltage is provided by the TDA4720(T).
2. PAL signal (red) with 75% saturation, 9 dB bandpath (pins 44 to 46), 6 dB trap (pin 2 to 4) and chrominance-to-burst ratio of 2.2:1.
3. NPN open emitter output.
4. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the frequency signal.
5. VCO1 operates as a fixed frequency oscillator during SECAM-mode.
6. Comb filter attenuations: PAL = 18 dB and NTSC = 12 dB.
7. Selective measurement of the f_{sc} component.
8. Measured at $V_{42-43(p-p)}$ = 12 mV.
   The signal suppression can be balanced at pin 38 (see Fig.1(a)).
9. During playback mode, the open collector output is conductive at the upper threshold and non-conductive at the lower threshold of the head pulse. The open collector output of pin 47 is conductive at the lower threshold and non-conductive at the upper threshold of the head pulse. During LP MS mode, pins 1 and 47 are simultaneously conductive independent of the head pulse.

Notes to the Characteristics (continued)

10. When the threshold of pin 24 is passed the upper part of the sandcastle pulse (pin 23) is suppressed 11 times and the chrominance output signals (pins 8 and 37) are colour killed for 13 lines.

11. Only active in PAL mode:
    - Output is HIGH, if the polarity of the demodulated burst is equal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' mixer is active.
    - Output voltage is LOW, if the polarity of the demodulated burst is unequal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' amplifier is active.

12. If APC = OFF, the mute output (pin 21) is switched to forced HIGH (used for automatic test picture insertion).

13. Test picture output signals depend on the control voltages at pins 15 and 28 as shown in Table 2. V_{ref} at pin 3 is loaded by the output current I_{16}.

Table 2 Control of test picture output signals

CONDITION	PIN 15 (V)	PIN 28 (V)	SEE FIG.2
APC OFF, test picture without white signal	2.7 to 3.4	<3	2(b)
APC OFF, test picture with white signal	>4.3	<3	2(a)
APC ON	<1.4	<3	2(b)
APC ON, super sync ON	<1.4	>3.5	2(c)

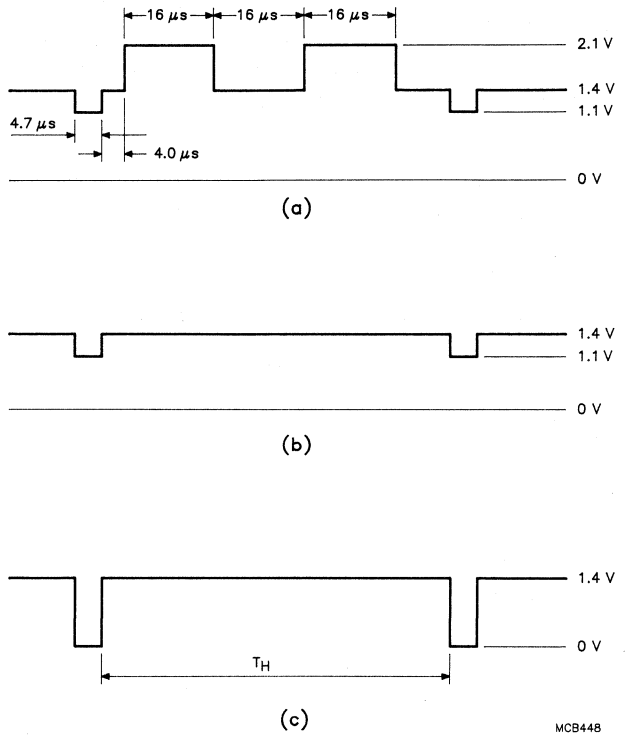

Fig.2 Test picture output.

Notes to the characteristics

14. Values refer to Fig.3 (R1 is the resistor from pin 26 to ground, C1 is the capacitor from pin 27 to ground):

- t_1 = 0.305 ms; R1C1
- t_2 = < 0.210 ms; R1C1
- t_3 = 0.1 ms; R1C1
- $t_4$1 = 0.367 ms;

15. Phase rotation:

MODE	CHANNEL 1($V_{29\text{-}19}$ = LOW)	CHANNEL 2 (V29-19 = HIGH)
PAL	0°	–90°
NTSC	+90°	–90°
SECAM	0°	0°

16. Switching to LP MS mode activates the $2f_H$ mode of the VCO2 PLL, automatic SKEW detection and automatic PAL sequence error correction.

17 If the video head changes from one track to another during LP MS mode, the 32 μs time shifted sync pulse occurs. This shift is recognized by the SKEW detector.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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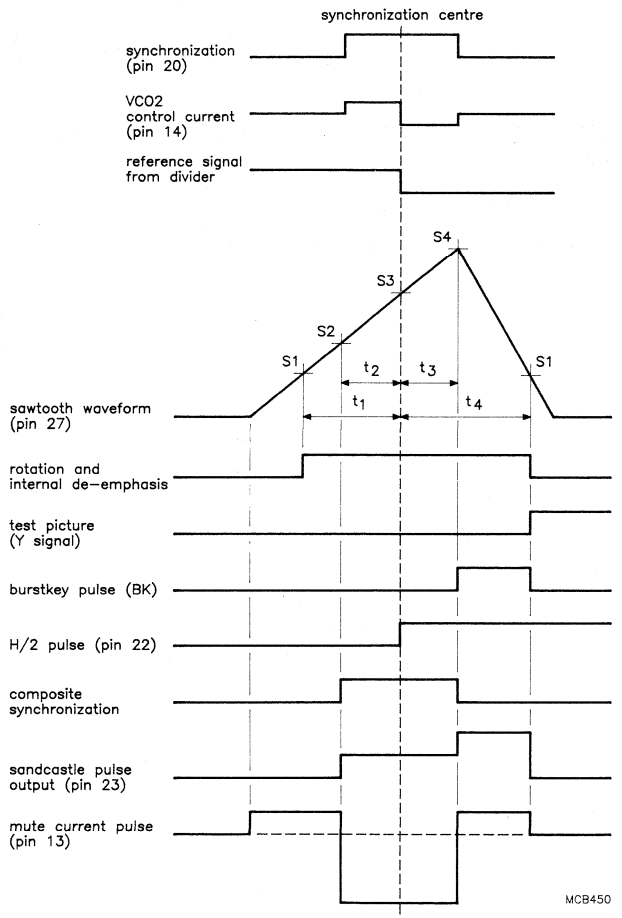

Fig.3 Timing diagram.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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APPLICATION INFORMATION

(Figs 4 to 39 show equivalent internal circuit configurations. All circuits are ESD protected).

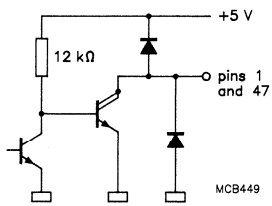


Fig.4 AGC switch output.

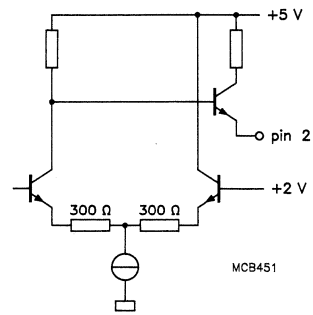


Fig.5 Chrominance output.

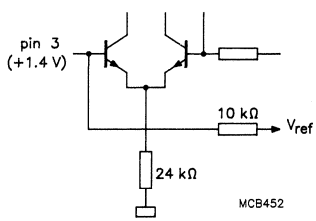


Fig.6 Voltage reference input.

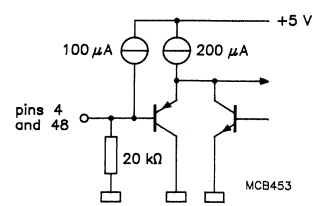
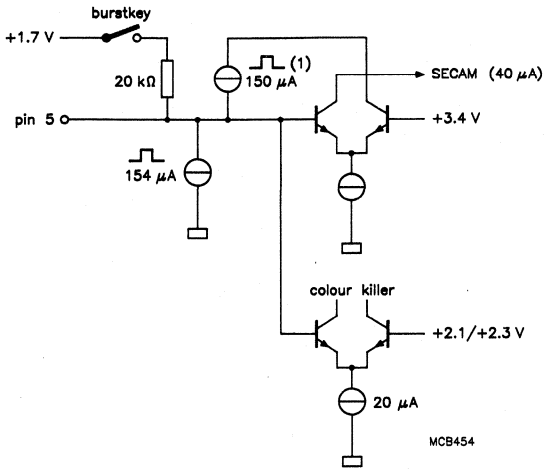


Fig.7 Chrominance/CVBS input.



(1) with an applied burst of 166 μA.

Fig.8 Colour-killer and SECAM switch input.

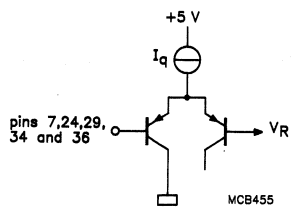


Fig.9 PAL/NTSC switch input (see Table 4).

Table 4 Switch characteristics

PIN	SIGNAL	QUIESCENT CURRENT (μA)	V(R) VOLTAGE (V)
7	PAL/NTSC switch input	20	2.5
24	HP input	30	2.5
29	phase rotation switch input	30	2.5
34	de/pre-emphasis switch input	30	1.1
36	record/playback switch input	20	3.3

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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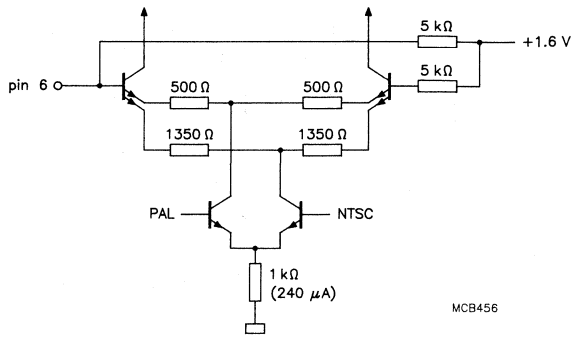

Fig.10 De-emphasis input.

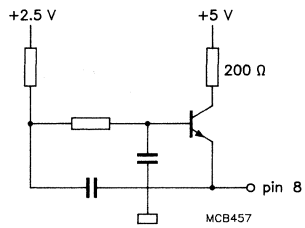

Fig.11 Chrominance output (pin 8).

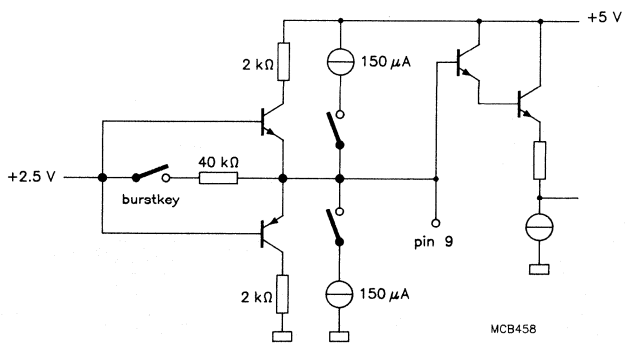

Fig.12 VCO3 control input.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

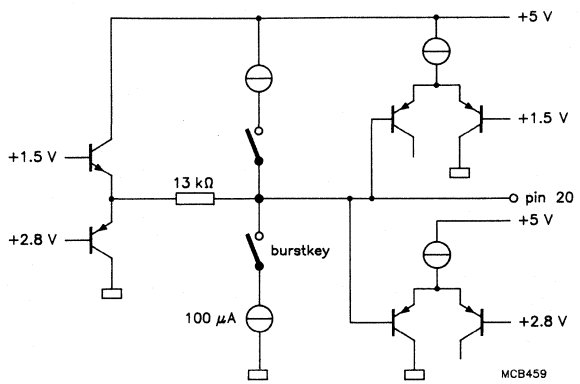

Fig.13 Sequence error detector.

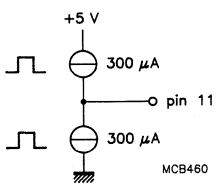

Fig.14 Sidelock detector output.

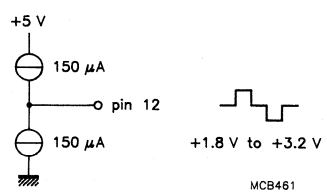

Fig.15 H/2 ripple coupling output.

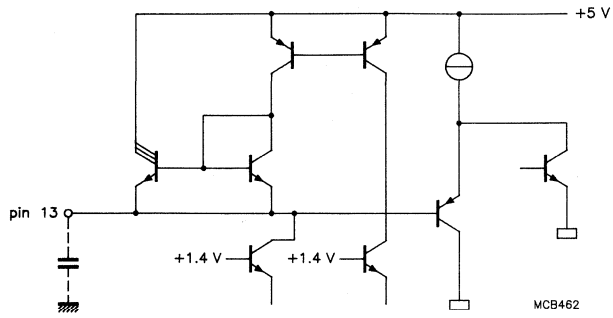

Fig.16 Mute timing input.

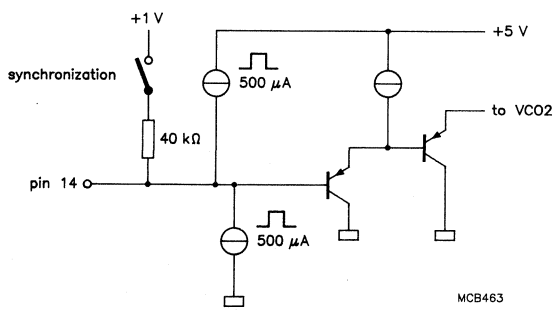

Fig.17 VCO2 control input.

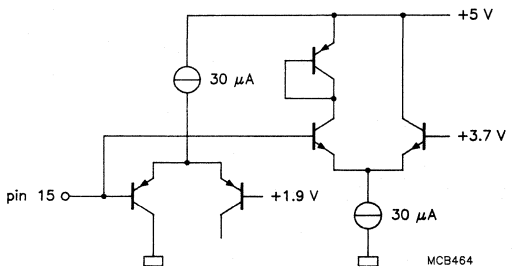

Fig.18 APC/test picture switch input.

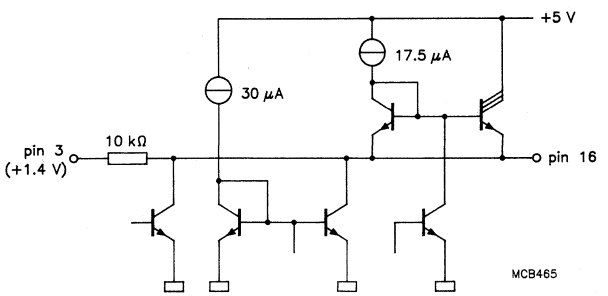

Fig.19 Test picture output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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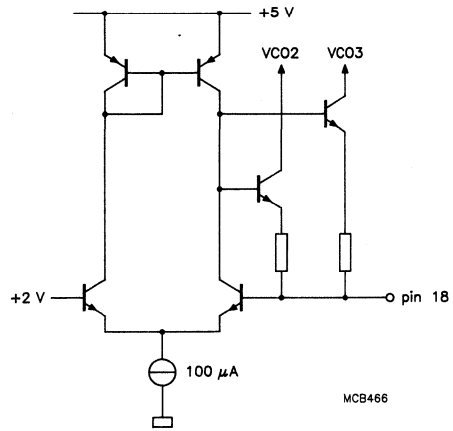

Fig.20 VCO2/VCO3 adjustment input.

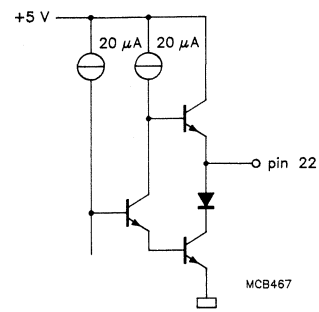

Fig.21 H/2 output.

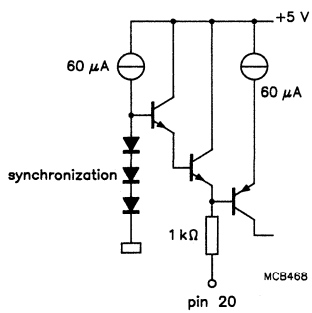

Fig.22 Synchronization input.

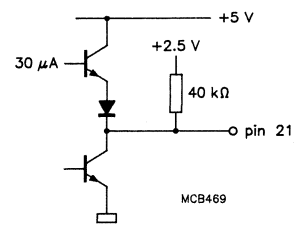

Fig.23 Mute detector output.

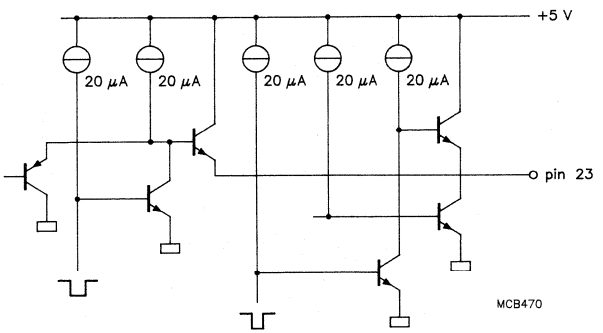

Fig.24 Sandcastle pulse output.

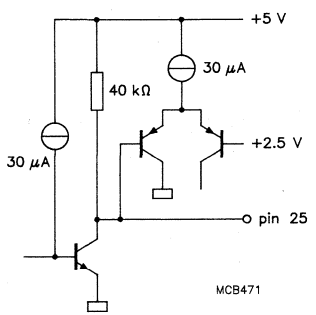

Fig.25 Skew detector output.

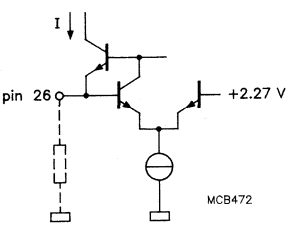

Fig.26 Reference current input for the sawtooth generator.

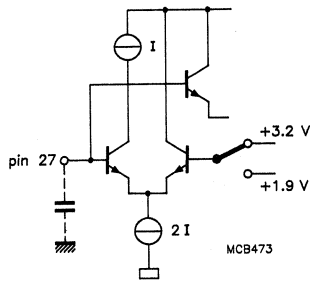

Fig.27 Sawtooth generator.

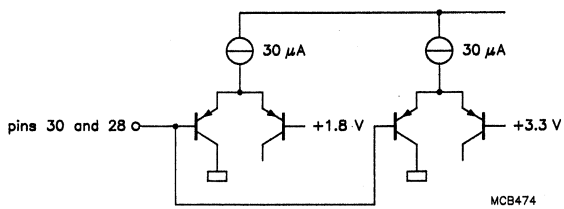

Fig.28 Multispeed AGC/LP input.

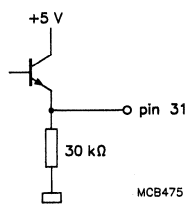

Fig.29 Subcarrier signal output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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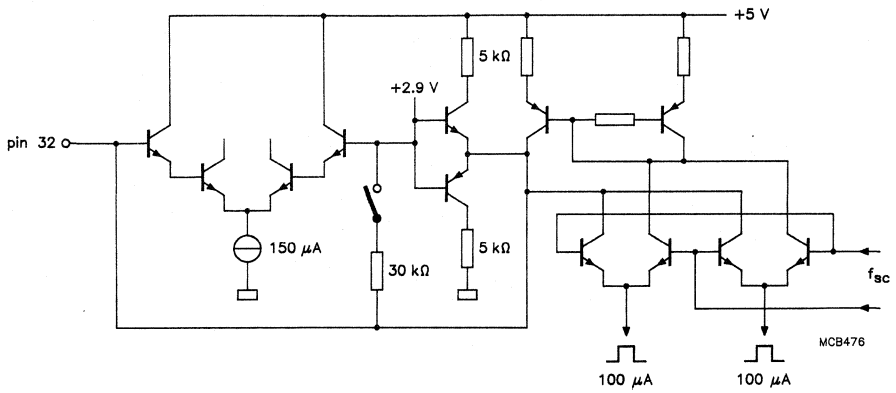

Fig.30 VCO1 control input.

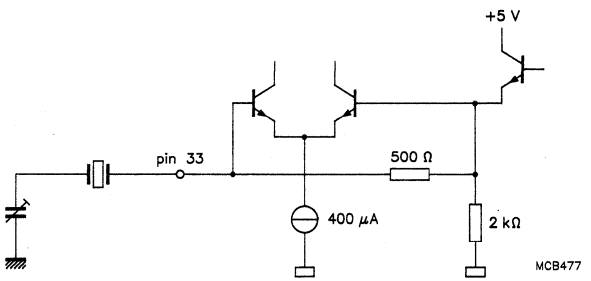

Fig.31 Oscillator input.

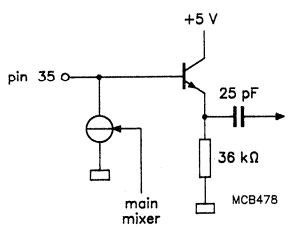

Fig.32 Subcarrier resonance output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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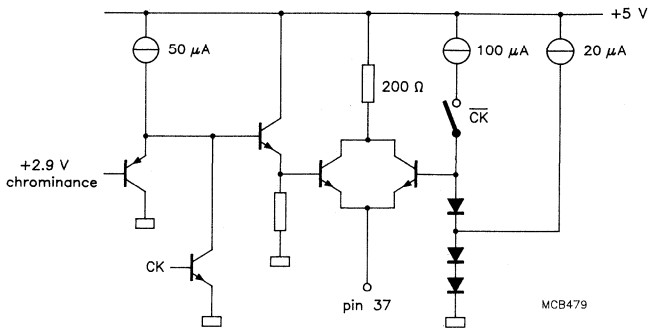


Fig.33 Chrominance signal output.

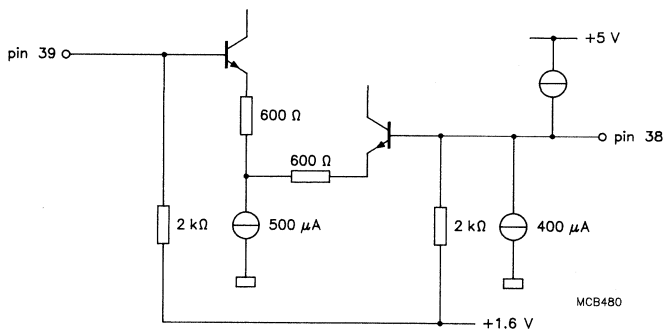


Fig.34 Main mixer input/balance circuit.

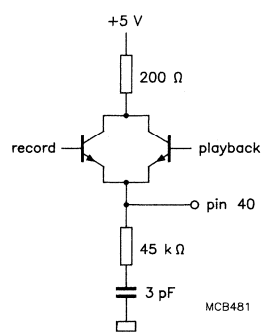


Fig.35 Chrominance output.

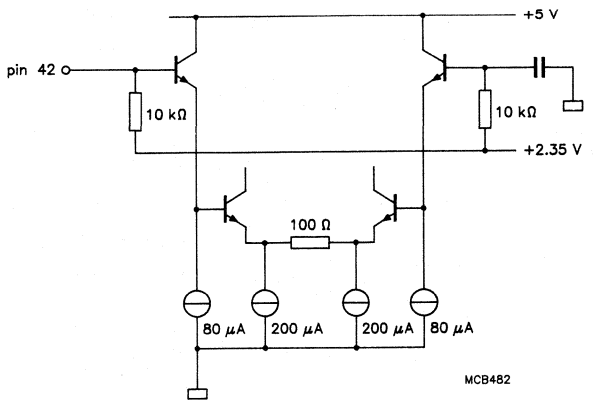


Fig.36 Chrominance input.

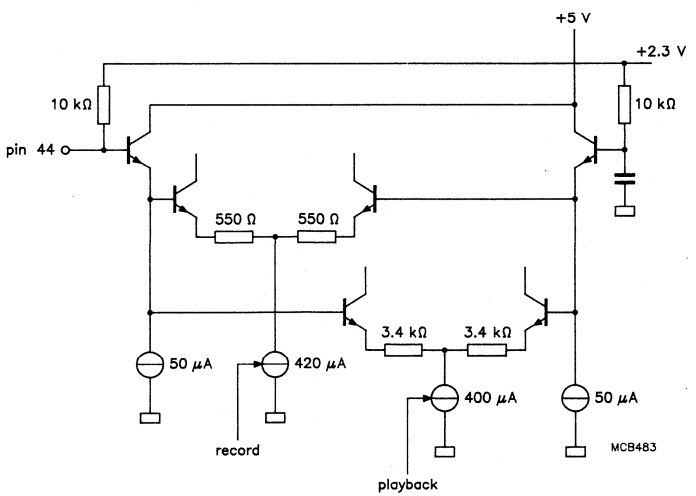


Fig.37 Chrominance AGC input.

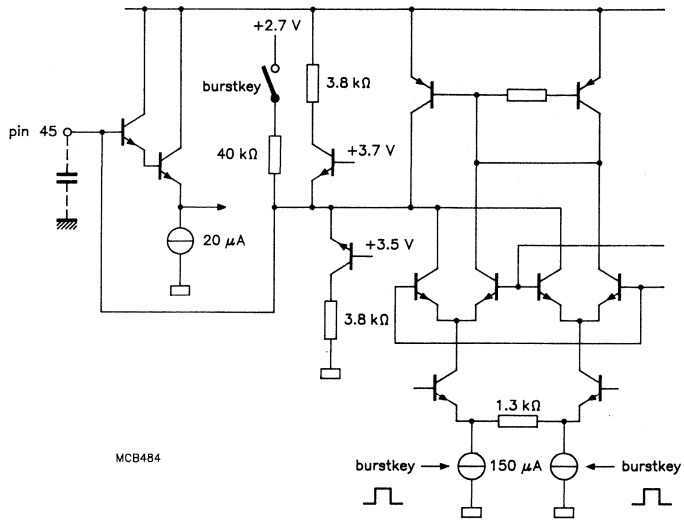


Fig.38 AGC control input.

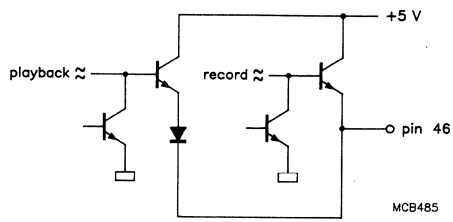


Fig.39 Chrominance output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

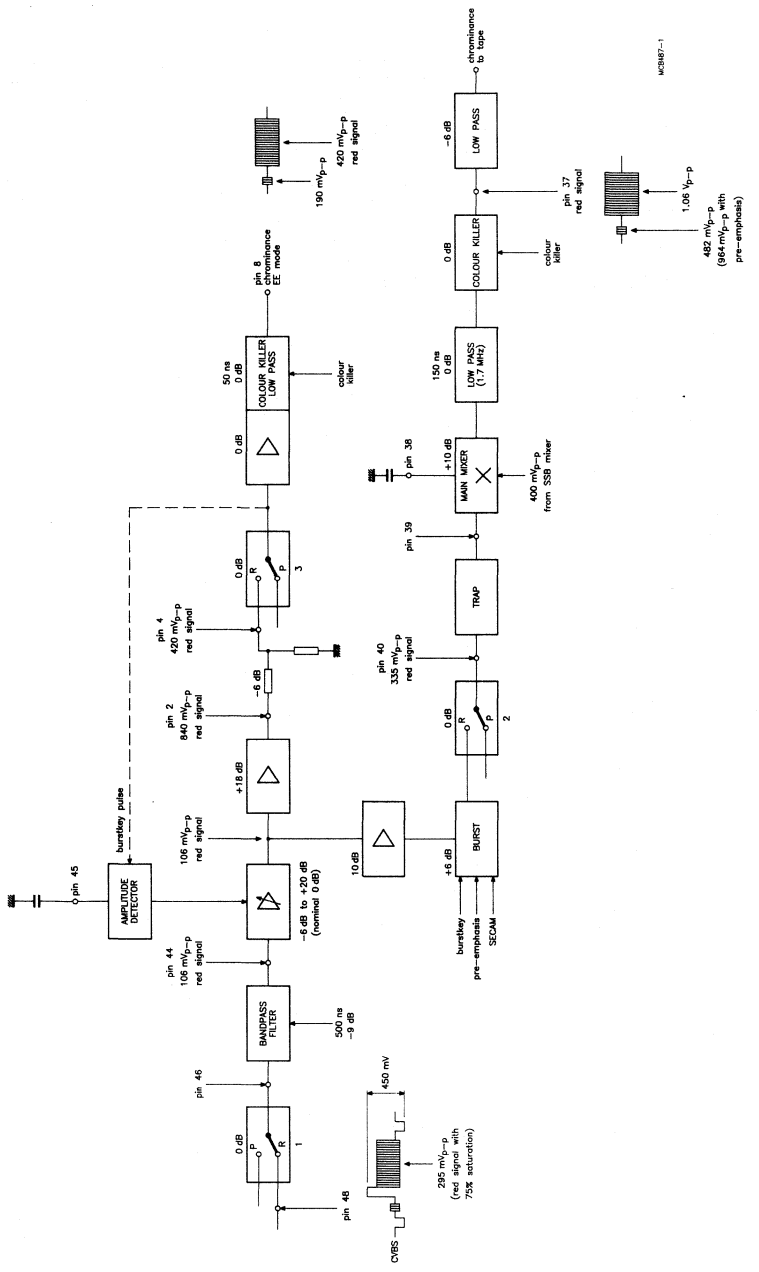


Fig.40 Signal path; record mode.

Where:

P = playback
R = record

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

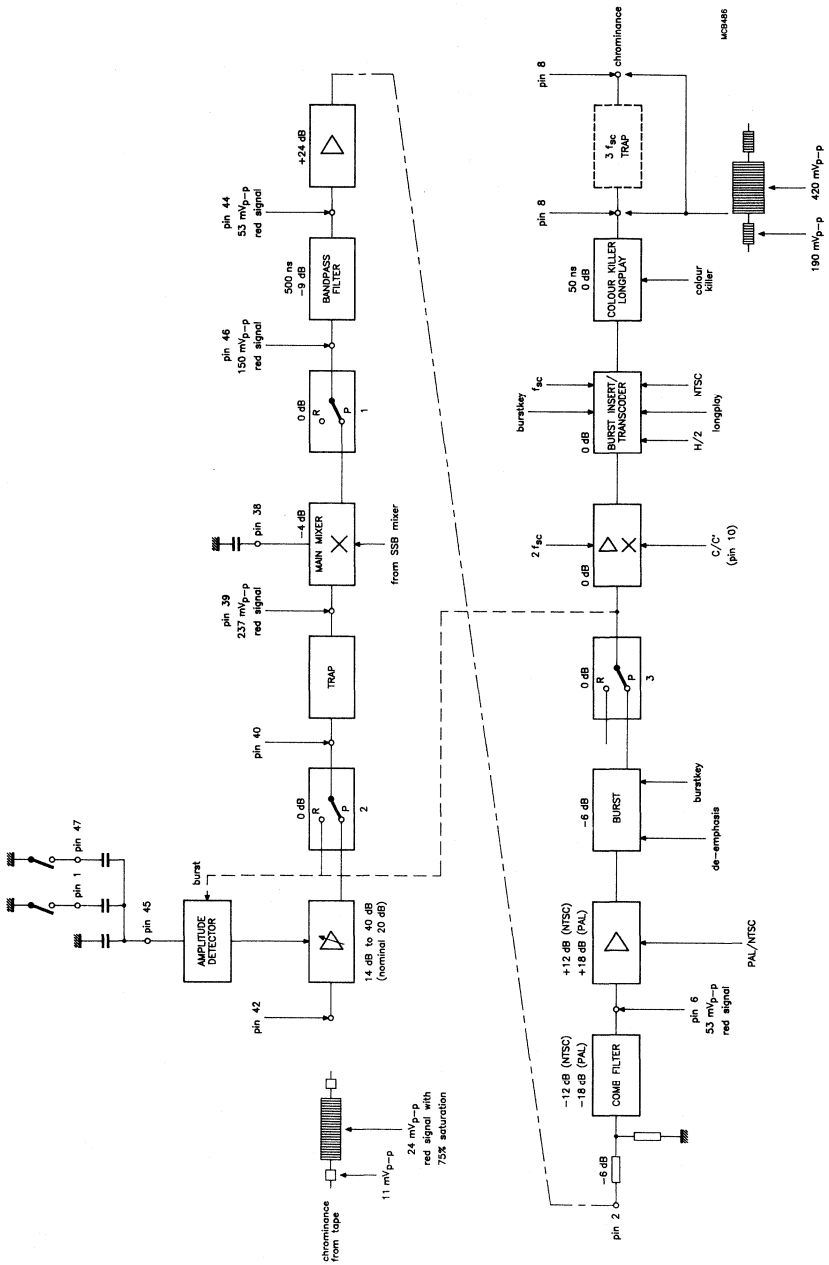


Fig.41 Signal path; playback mode.

Where:

P = playback
R = record

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

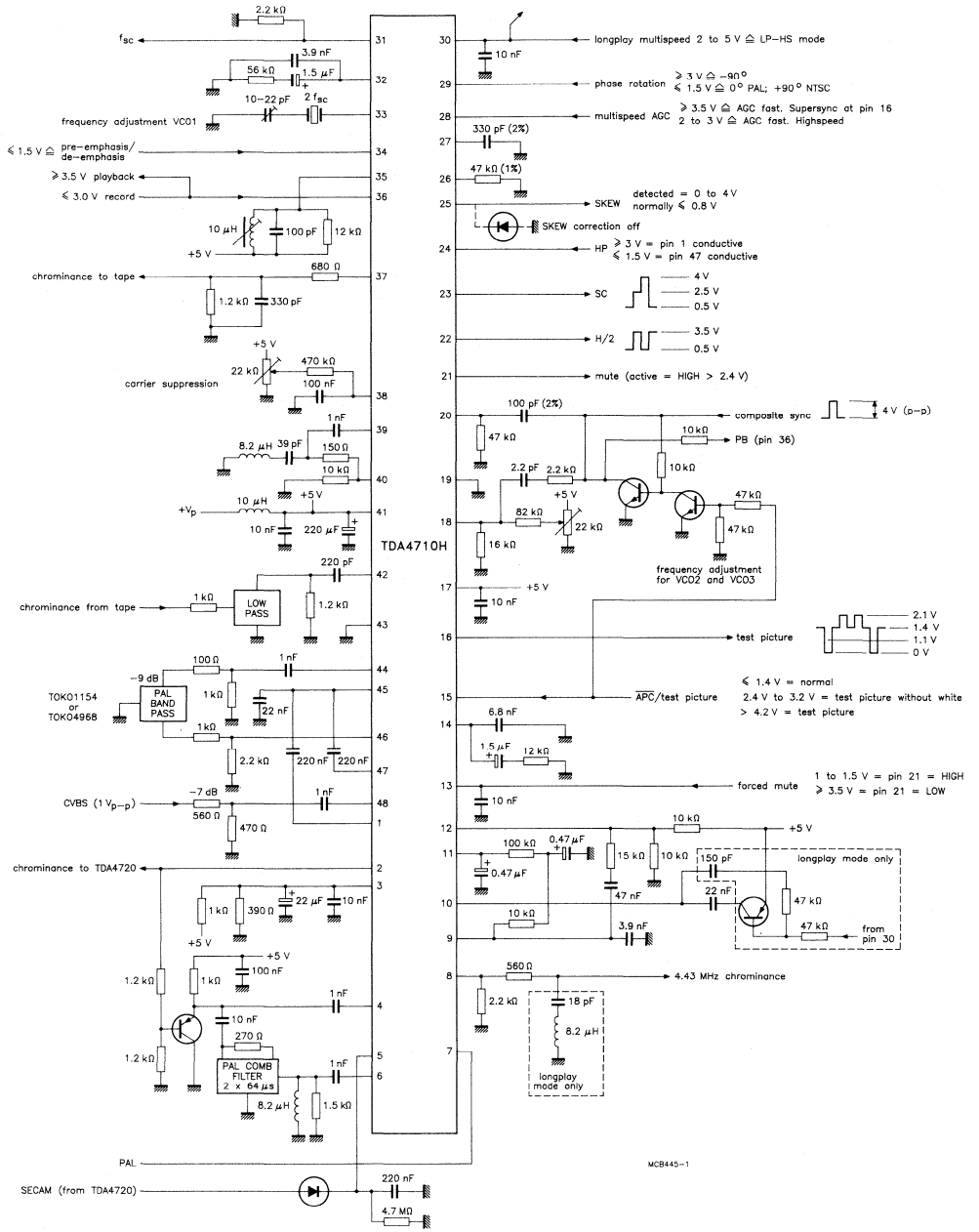


Fig.42 Application diagram (PAL).

Note to Fig.42

If not otherwise stated, the tolerance for external components is:
resistors ±5%
capacitors ±20%
inductors ±10%

SECAM IDENTIFICATION AND CHROMINANCE CORRECTION CIRCUIT

The TDA4720T is a monolithic integrated circuit for SECAM identification and chrominance signal correction in VHS video cassette recorders (VCR). It can be applied as a stand-alone SECAM identification circuit and, when used in conjunction with TDA4710, together they provide all the functions necessary for PAL/SECAM B, G chrominance processing in VHS VCRs.

Features

- Very reliable SECAM identification by means of chrominance burst amplitude, presence of both SECAM colour carriers and line alternation of both carriers
- Two identification outputs: SECAM YES/NO
- Internal phase correction of the demodulated burst
- Internal detection and switching for SECAM long-play VCR (for 'trick' modes)
- Internal buffers and switches for correction of the line-alternating colour carriers

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	4,5	5,0	5,5	V
Supply current	I_P	–	16	17	mA
Chrominance input signal to phase detector (peak-to-peak value)	$V_{14,15-4(p-p)}$	60	–	300	mV
Chrominance input signal to line correction circuit (peak-to-peak value)	$V_{5,12-4(p-p)}$	–	–	1	V
Chrominance output signal from line correction circuit (peak-to-peak value)	$V_{7-4(p-p)}$	–	–	1	V

PACKAGE OUTLINES

TDA4720: 16-lead DIL; plastic (SOT38).
TDA4720T: 16-lead mini-pack; plastic (SO16; SOT109A).

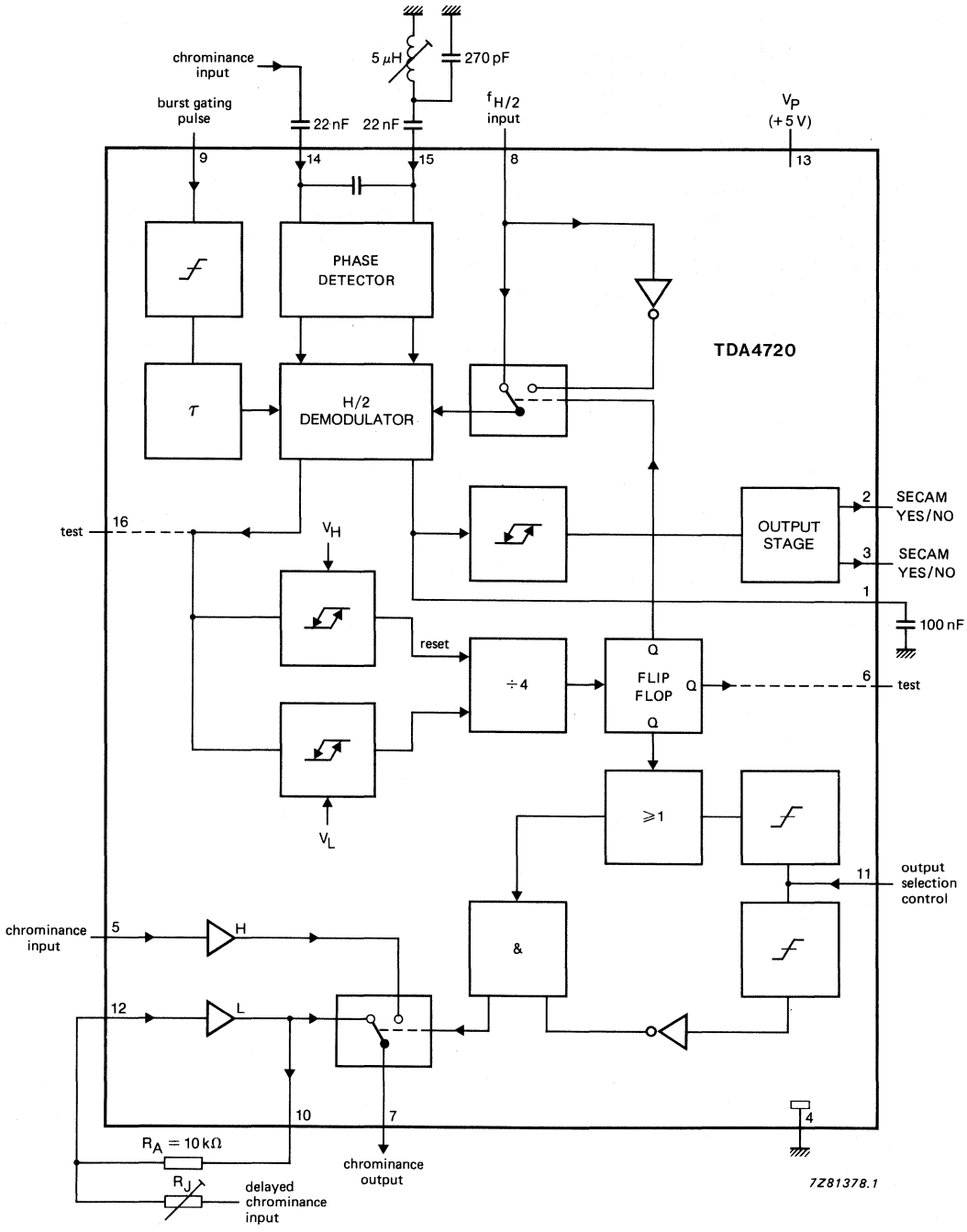


Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

PINNING

pin. no.	function
1	Integration of demodulated bursts.
2	Buffered output; SECAM YES/NO.
3	Buffered output; SECAM YES/NO.
4	Ground.
5	Chrominance input (only if line correction of SECAM carrier is used).
6	Test pin (internal connection).
7	Chrominance output (of line-corrected SECAM; only if line correction of SECAM carrier is used).
8	$f_{H/2}$ frequency input for chrominance burst demodulation.
9	Burst gating pulse input.
10	Feedback resistor for pin 12 signal path (only if line correction of SECAM carrier is used).
11	Output selection control (selects signal path to pin 7).
12	Delayed chrominance input (delayed by 1H; only if line correction of SECAM carrier is used).
13	Positive supply voltage (V_P = + 5 V).
14,15	The LC circuit at pin 15 has to be tuned to the centre frequency between the two chrominance carriers (at pin 14). The phase detector then provides a positive or negative output voltage depending on the first or second chrominance carrier.
16	Test pin (internal connection).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_P = V_{13-4}$	–	6,0	V
Voltage range on pins 6, 8, 9, 11, 12, 14 and 15	V_{n-4}	0	V_P	V
Maximum current at pins 1, 2, 3, 7, 15, 16 and 18	I_n	–	2	mA
Total power dissipation	P_{tot}	–	120	mW
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-4} = 5$ V; $T_{amb} = 25$ °C; test circuit as per Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_P	4,5	5,0	5,5	V
Supply current		I_{13}	–	16	17	mA
Identification						
AC input voltage (peak-to-peak value)		$V_{14,15-4}$	60	125	300	mV
Input resistance		$R_{14,15-4}$	14	18	22	kΩ
Charge capacitor		C_{1-4}	–	100	–	nF
Forced SECAM-ON voltage		V_{1-4}	3,8	–	–	V
Forced SECAM-OFF voltage		V_{1-4}	–	–	2	V
Sensitivity of phase detector	$V_{14,15-4(p-p)}$ = 125 mV	α	–	1,6	–	V/rad.
Output voltage						
in SECAM mode		$V_{2,3-4}$	4,3	–	–	V
in non-SECAM mode		$V_{2,3-4}$	–	–	0,8	V
Output current						
in SECAM mode		$I_{2,3}$	1	–	–	mA
in non-SECAM mode		$I_{2,3}$	–	–	0,3	μA
Burst gating						
Input resistance		R_{9-4}	20	25	–	kΩ
Threshold voltage HIGH (phase detector active)		V_{9-4}	3,0	3,25	3,5	V
H/2 demodulator						
Input resistance		R_{8-4}	20	25	–	kΩ
Threshold voltage for changing conditions of H/2 demodulator		V_{8-4}	3,0	3,25	3,5	V
Chrominance correction						
Chrominance input signal (peak-to-peak value)		$V_{5-4(p-p)}$	–	–	1	V
Input resistance		R_{5-4}	10	13	16	kΩ
Input capacitance		C_{5-4}	–	–	10	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Delayed chrominance input signal (peak-to-peak value)		$V_{12\text{-}4(p\text{-}p)}$	–	–	1	V
Input resistance		$R_{12\text{-}4}$	–	50	–	kΩ
Input capacitance		$C_{12\text{-}4}$	–	–	10	pF
Voltage gain		$\frac{V_{7\text{-}4}}{V_{12\text{-}4}}$	–	$\frac{R_A}{R_J}$	–	
Gain adjustment range		ΔG	19	–	–	dB
Gain bandwidth product		f_G	30	–	–	MHz
Output signal (peak-to-peak value)		$V_{7\text{-}4(p\text{-}p)}$	–	–	1	V
Output resistance		$R_{7\text{-}4}$	$\frac{V_T}{I_C}$	–	–	Ω
DC output voltage		$V_{7\text{-}4}$	–	–	2,5	V
Difference in DC output levels at pin 7 with pin 5/pin 12 switching		$\Delta V_{7\text{-}4}$	–	–	20	mV
Output selection control						
Input resistance		$R_{11\text{-}4}$	20	25	30	kΩ
Input voltage to select pin 5 signal for output		$V_{11\text{-}4}$	0	–	1,5	V
Input voltage to select pin 12 signal for output		$V_{11\text{-}4}$	2,75	–	5,0	V
Input voltage for automatic output switching*		$V_{11\text{-}4}$	2,0	–	2,6	V

DEVELOPMENT DATA

* This voltage is generated internally if pin 11 is not connected.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4725T

SECAM-L chrominance processor for VHS video recorders

FEATURES

- Forced recording or playback mode input
- SECAM identification circuit
- One circuit for Bell and anti-Bell filter (1.07 MHz)
- Fully ESD protected
- Low power consumption (170 mW)
- 5 V supply.

GENERAL DESCRIPTION

The TDA4725 is a bipolar integrated circuit for chrominance processing of SECAM-L signals in SECAM-L or Multistandard VHS video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{18\text{-}24,26}$	supply voltage		4.5	5.0	5.5	V
I_{18}	supply current		-	34	-	mA
$V_{25\text{-}24(p\text{-}p)}$ $V_{21\text{-}24(p\text{-}p)}$	chrominance input (peak-to-peak value)	record mode playback mode	- -	- 300	645 600	mV mV
$V_{15\text{-}24(p\text{-}p)}$ $V_{1\text{-}24(p\text{-}p)}$	chrominance output (peak-to-peak value)	record mode playback mode	560 -	630 -	700 1000	mV mV
T_{amb}	operating ambient temperature range		0	-	70	°C
T_{stg}	storage temperature range		–25	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4725	28	DIL28	plastic	SOT117
TDA4725T	28	SO28	plastic	SOT136A

SECAM-L chrominance processor for VHS video recorders

TDA4725T

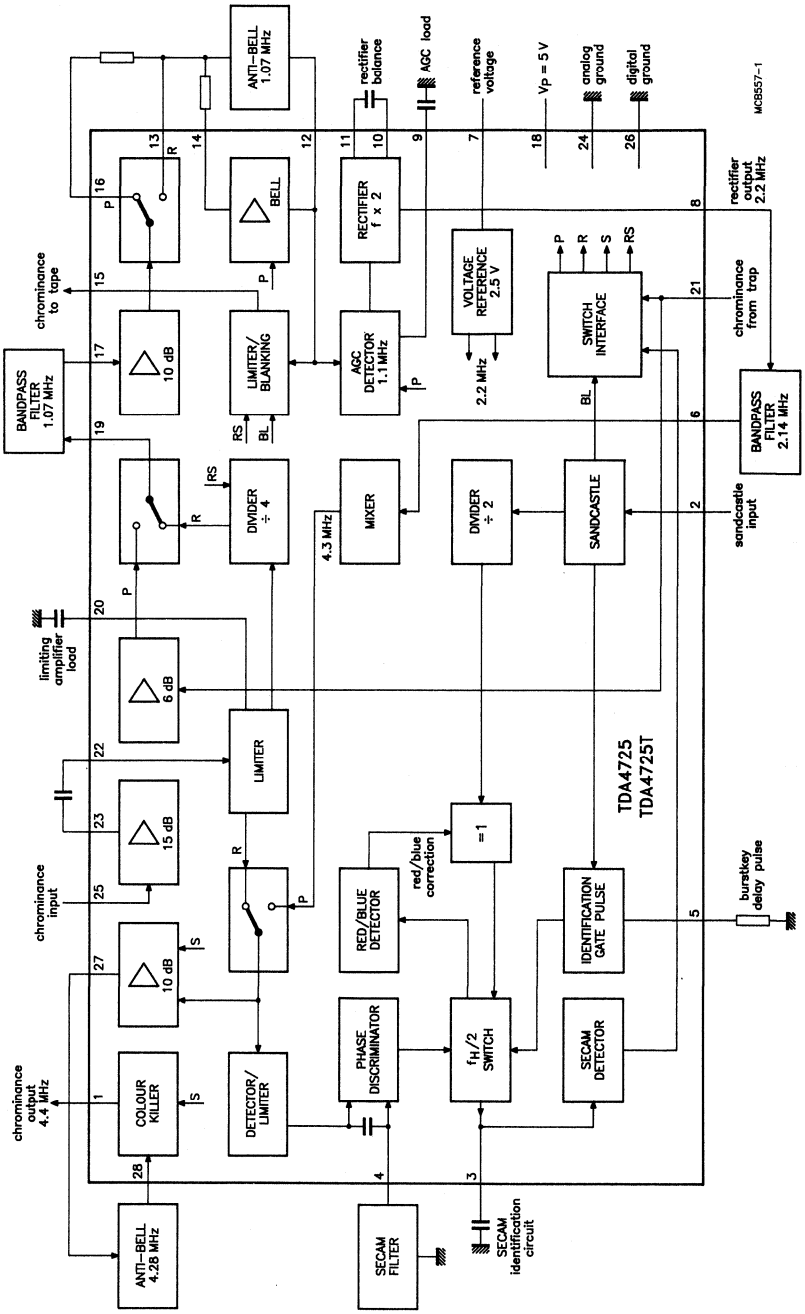


Fig.1 Block diagram.

SECAM-L chrominance processor for VHS video recorders

TDA4725T

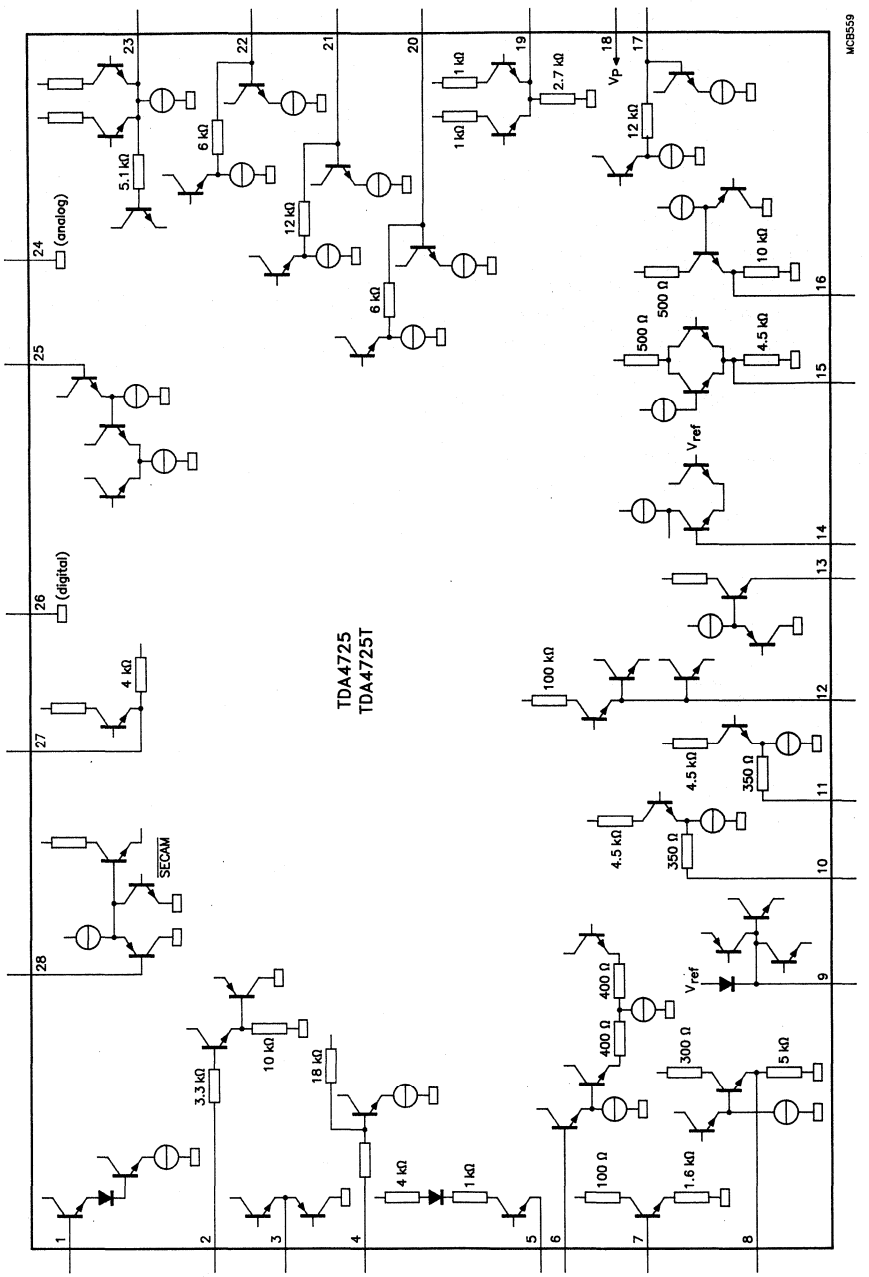


Fig.2 Internal pin configuration diagram.

SECAM-L chrominance processor for VHS video recorders

TDA4725T

PINNING

PIN	DESCRIPTION
1	chrominance output (4.4 MHz)
2	sandcastle pulse or composite synchronization pulse input
3	connection for external load capacitor for the SECAM identification circuit
4	connection for external resonance circuit for the phase discriminator circuit
5	connection for resistor required for internal delay of burstkey pulse
6	mixer input
7	reference voltage
8	rectifier circuit output (2.2 MHz)
9	connection for external load capacitor for the AGC
10	connection for external balancing capacitor for the rectifier circuit
11	connection for external balancing capacitor for the rectifier circuit
12	output to passive anti-Bell circuit and limiter circuit (record mode) or output to Bell circuit and AGC circuit (playback mode)
13	10 dB amplifier output to anti-Bell circuit (record mode only)
14	virtual ground
15	chrominance signal output to tape (1.1 MHz)
16	output 10 dB amplifier and input active Bell filter (playback mode only)
17	input to 10 dB amplifier
18	power supply
19	divider output (record mode) or 6 dB amplifier output (playback mode)
20	external capacitor for limiting amplifier
21	chrominance signal input from tape
22	limiting amplifier input
23	15 dB amplifier output
24	analog ground
25	15 dB amplifier input
26	digital ground
27	10 dB amplifier output
28	input for colour killer circuit

SECAM-L chrominance processor for VHS video recorders

TDA4725T

FUNCTIONAL DESCRIPTION (see Fig.1)

Recording mode

The chrominance signal is separated from the CVBS signal using an external bandpass filter and an external Bell circuit. The signal is applied to a divider (÷ 4) via a 15 dB amplifier (pin 25) and limiter (pin 22). Once divided the 1.1 MHz signal is fed via an external bandpass filter (pins 17 and 19), an internal 10 dB amplifier (via pin 17), an external anti-Bell filter (pins 12 and 13) and a limiter/blanking stage. The blanking stage is active during the sandcastle pulses.

E to E mode

The 4.4 MHz signal is obtained from a tap in the limiter circuit and is applied to the chrominance output (pin 1) via the 10 dB amplifier, the external anti-Bell circuit and the colour-killer stage

Playback mode

The 1.1 MHz signal from the tape is applied, via a trap, to an internal 6 dB amplifier (via pin 21). Once amplified the signal is applied via an external bandpass filter and 10 dB amplifier to an operational amplifier (pins 12 and 14). The operational amplifier has an external anti-Bell circuit connected in its feedback path and, consequently, performs as a Bell circuit. From the operational amplifier the signal is applied to the AGC stage. The output signal from the AGC stage is applied to a rectifier where the frequency is doubled. Unwanted harmonics are removed by an external bandpass filter (pins 6 and 8) and the frequency is again doubled by the mixer at pin 6. The resultant 4.4 MHz signal is applied to the output stage at pin 1 via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

NOTE: The 1.07 MHz bandpass filter (pins 17 and 19) and the anti-Bell circuit (pins 12 and 13) are used in both the record and playback mode.

SECAM identification

For SECAM identification the input signal is phase shifted by an external resonent circuit [$f_O = (f_b + f_r)/2$] and fed to the phase discriminator at pin 4. If the signal is a SECAM signal the positive- and negative-going pulses (with reference to the clamping voltage) are generated and rectified via the H/2 demodulator. The signal now consists of positive-going pulses only which are integrated via an external capacitor and applied to the SECAM detector at pin 3.

A non-SECAM signal (i.e. PAL) is removed from the phase discriminator having only positive-going pulses. After the H/2 demodulator, the signal has line-alternate positive- and negative-going pulses which compensate after integration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Ratings System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	-	6	V
P_{tot}	total power dissipation	-	250	mW
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

SECAM-L chrominance processor for VHS video recorders

TDA4725T

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 1						
$V_{1-24(p-p)}$	chrominance output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	-	1	V
V_{1-24}	DC level	SECAM signal non-SECAM signal	- -	V_{28-24} -	- 0.1	V V
R_{1-24}	output resistance		-	V_t/I_e	-	Ω
α_1	non-SECAM signal suppression		40	-	-	dB
Pin 2						
V_{2-24}	phase discriminator active voltage level		3.6	-	V_P	V
V_{2-24}	blanking active voltage level		2.0	2.5	3.0	V
V_{2-24}	blanking and phase discriminator inactive voltage level		-	-	1.5	V
R_{2-24}	input resistance		20	-	-	kΩ
Pin 4						
R_{4-24}	input resistance		14	18	22	kΩ
Pin 5						
R_{5-24}	required resistance to ground	for 1 μs	-	26	-	kΩ
Pin 6						
V_{6-24}	input signal	2.2 MHz sinusoidal signal	-	300	-	mV
V_{6-24}	DC level		-	V_{7-24}	-	V
R_{6-7}	input resistance		-	560	1200	Ω
C_{6-24}	input capacitance		-	-	5	pF
Pin 7						
V_{7-24}	DC level		2.4	2.5	2.6	V
$-I_7$	output current		-	-	5	mA
I_7	input current		1	-	-	mA
R_{7-24}	output resistance		-	-	1	Ω
Pin 8						
$V_{8-24(p-p)}$	output signal voltage (peak-to-peak)	2.2 MHz	-	600	-	mV
V_{8-24}	DC level		-	2.45	-	V
R_{8-24}	output resistance		-	V_t/I_e	-	Ω
α_8	1.1 MHz suppression		30	-	-	dB
α_8	3.3 MHz suppression		30	-	-	dB
α_8	4.4 MHz suppression		10	-	-	dB
Pin 12						
$V_{12-24(p-p)}$	input signal (peak-to-peak value)	playback mode	24	-	320	mV
V_{12-24}	DC level	record mode playback mode (closed loop)	- -	V_{13-24} V_{7-24}	- -	V V
B	gain bandwidth (operational amplifier)	playback mode	40	-	-	MHz
R_{12-24}	input resistance	record mode	100	-	-	kΩ
R_{12}	open-loop output resistance		-	V_t/I_e	-	Ω

SECAM-L chrominance processor for VHS video recorders

TDA4725T

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 13 V_{13-24}	DC level	record mode	-	V_{7-24}– 85 mV	-	V
G_{13-24}	signal gain	record mode	-	10	-	dB
R_{13-24}	output resistance	record mode	-	V_t/I_e	-	Ω
Pin 14 V_{14-24}	DC level	playback mode	-	V_{7-24}	-	V
Pin 15 $V_{15-24(p-p)}$	chrominance output (peak-to-peak value)		560	630	700	mV
V_{15-24}	DC level		-	V_{7-24}– 80 mV	-	V
R_{15-24}	output resistance		-	-	10	Ω
α_{15}	playback suppression		30	-	-	dB
α_{15}	non-SECAM suppression		40	-	-	dB
α_{15}	blanking suppression		30	-	-	dB
Pin 16 V_{16-24}	DC level	playback mode	-	V_{7-24}– 54 mV	-	V
G_{16-17}	signal gain	playback mode	-	10	-	dB
R_{16-24}	input resistance	record mode	-	10	-	kΩ
R_{16-24}	output resistance	playback mode	-	V_t/I_e	-	Ω
Pin 17 $V_{17-24(p-p)}$	input signal (peak-to-peak value)		-	400	-	mV
V_{17-24}	DC level		-	V_{7-24}– 30 mV	-	V
R_{17-24}	input resistance		8	12	16	kΩ
C_{17-24}	input capacitance		-	-	5	pF
Pin 19 V_{19-24}	DC level	record mode playback mode	- -	1.82 1.7	- -	V V
$V_{19-24(p-p)}$	AC level (peak-to-peak value)	sinusoidal	-	800	-	mV
		block	-	621	-	mV
G_{19-24}	signal gain	playback mode	-	6	-	dB
R_{19-24}	output resistance		-	V_t/I_e	-	Ω
Pin 21 $V_{21-24(p-p)}$	input signal (peak-to-peak)	playback mode	-	300	600	mV
V_{21-24}	DC level		-	3.25	-	V
V_{21-24}	record mode active voltage level		-	-	1.5	V
V_{21-24}	playback mode active voltage level		2.2	-	-	V
R_{21-24}	input resistance		8	12	16	kΩ
C_{21-24}	input capacitance		-	-	5	pF
Pin 25 $V_{25-24(p-p)}$	input signal (peak-to-peak value)		-	-	645	mV
V_{25-24}	DC level		-	V_{7-24}	-	V
R_{25-24}	input resistance		100	-	-	kΩ
C_{25-24}	input capacitance		-	-	5	pF

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 27 R_{27-24}	output resistance		-	-	10	Ω
RECORD MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 600 mV (p-p)	-	1175	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 300 mV (p-p)	-	1110	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 30 mV(p-p)	-	272	-	mV
V_{27-24}	DC level		-	1.65	-	V
PLAYBACK MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	1175	-	mV
V_{27-24}	DC level		-	3	-	V
G_{27-6}	signal gain		-	12	-	dB
α_{27}	2.2 MHz suppression		23	-	-	dB
α_{27}	6.6 MHz suppression		30	-	-	dB
α_{27}	8.8 MHz suppression		10	-	-	dB
Pin 28 $V_{28-24(p-p)}$	input signal (peak-to-peak)		-	-	1000	mV
V_{28-24}	DC level		-	V_{27-24}	-	V
R_{28-24}	input resistance		100	-	-	kΩ
C_{28-24}	input capacitance		-	-	5	pF

SECAM-L chrominance processor for VHS video recorders

TDA4725T

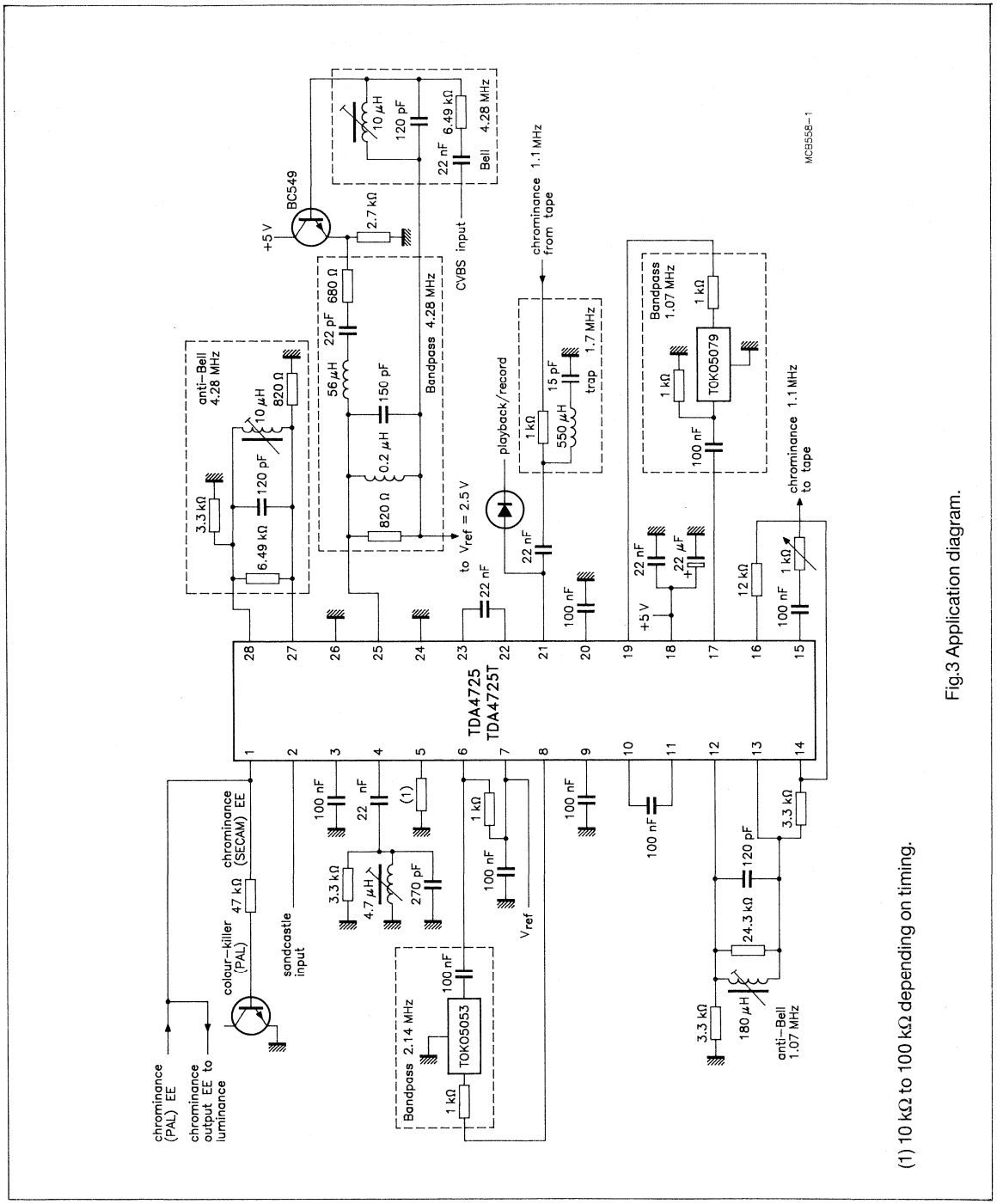


Fig.3 Application diagram.

(1) 10 kΩ to 100 kΩ depending on timing.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	June 1990

TDA4800

Vertical deflection circuit for monitor applications

FEATURES

- Fully integrated, few external components
- RC oscillator with wide sync range of 1:2 (e.g. 50 Hz to 100 Hz)
- Synchronization by positive or negative going sync pulse
- Blanking pulse duration is determined externally
- Dual frequency criterion for automatic amplitude switch-over (e.g. 50 Hz to 60 Hz)
- Guard circuit for screen protection
- Sawtooth generator with buffer stage supplied by external voltage
- Preamplifier
- Power output stage with thermal and SOAR protection
- Flyback generator
- Internal voltage stabilizer

GENERAL DESCRIPTION

The TDA4800 is a monolithic integrated circuit for vertical deflection primarily in monitors (and TV receivers). The complete circuit consists of 11 main functional blocks as shown in Fig.1.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_P	supply current (pins 6 and 10)	note 1	–	215	–	mA
I_{7M}	output peak current	note 1	–	800	–	mA
$I_{7(p-p)}$	output current (peak-to-peak value)	note 1	–	1500	–	mA
f_{sync}	picture frequency	note 1	–	–	90	Hz
V_3	positive sync input pulse		1.0	–	6.0	V
V_3	negative sync input pulse		–0.5	–	–0.7	V
T_{amb}	operating ambient temperature range	note 2	–20	–	+ 70	°C

Notes to the quick reference data

1. Measured in circuit Fig. 4.
2. P_{tot} = 3.6 W for $R_{th\ j\text{-}a}$ = 20 K/W.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4800	13	SBD	plastic	SOT141RGA

Vertical deflection circuit for monitor applications

TDA4800

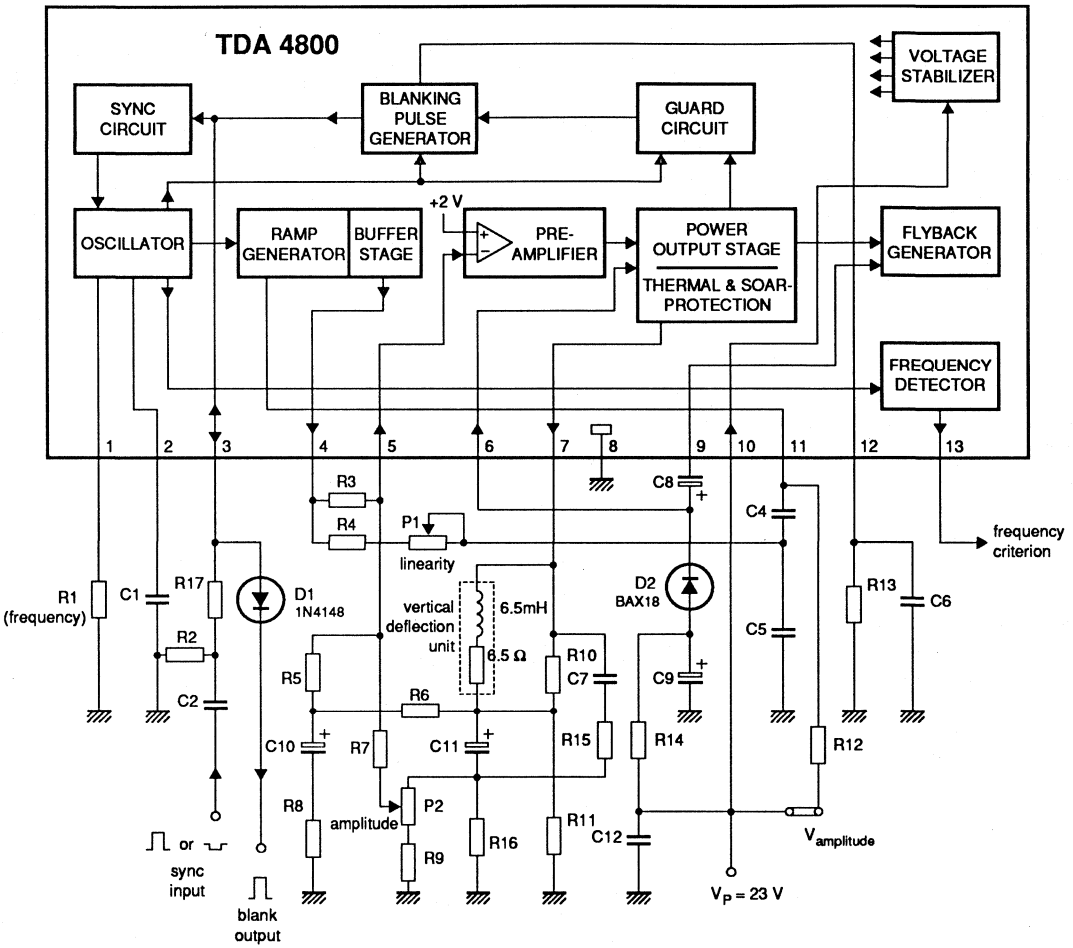


Fig.1 Block diagram.

Vertical deflection circuit for monitor applications

TDA4800

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. Oscillator
2. Synchronization circuit
3. Blanking pulse generator
4. Frequency detector and storage
5. Ramp generator
6. Buffer stage
7. Preamplifier
8. Power output stage
9. Flyback generator
10. Guard circuit
11. Voltage stabilizer

1. Oscillator (pins 1, 2)

The oscillator is an RC-oscillator with a threshold value switch, which ensures very good frequency stability.

The upper and lower threshold voltages are defined by an internal voltage divider.

An external capacitor C1 at pin 2 is charged by a constant current source. When the scan voltage of C1 reaches the upper threshold voltage, oscillator flyback starts. Capacitor C1 discharges via an internal resistor and transistor until the lower threshold is reached.

The constant charge current and free-running frequency f_o are adjusted by an external resistor R1 at pin 1:

$$f_o = \frac{1}{K \times R1 \times C1} \quad \text{with } K = 0.68$$

2. Synchronization circuit (pin 3)

A positive- or negative-going pulse fed to pin 3 synchronizes the oscillator by lowering the upper threshold voltage. The synchronizing range is f_o to 2 f_o. For example:

$f_o = 60$ Hz $\longrightarrow$ $f_{sync\ max} = 120$ Hz.

3. Blanking pulse generator (pin 3)

Also at pin 3 a blanking pulse is available. Diode D1 separates the synchronization pulse from the blanking pulse. During scanning, the external capacitor C6 at pin 12 is charged to an internal stabilized voltage V. The blanking pulse starts with the beginning of oscillator flyback; then capacitor C6 discharges via the external resistor R13 at pin 12. The blanking pulse stops when the capacitor voltage is V/2.

The blanking pulse duration is determined by the values of external components R13 and C6 at pin 12:

$$t_{bl} = R13 \times C6 \times Ln2$$

4. Frequency detector with storage (pin 13)

At the end of the scanning period a frequency detector detects the oscillator frequency (see *Note*). When this frequency is above the threshold a flip-flop is set to store this information. The output is an open collector output.

Note:

Frequency detector change-over at pin 13 from low (= low frequency) to high (= high frequency) is determined by f_o:

$$f_{threshold} = 1.23 \times f_o$$

5. Ramp generator (pin 11)

The ramp generator consists of two external series capacitors C4 and C5, external charge resistor R12 (connected to pin 11), and an internal differential amplifier which is synchronously-switched by the oscillator.

External capacitors C4 and C5 at pin 11 are charged by the charging current via the external charge resistor R12 until oscillator flyback starts. C4 and C5 are then discharged via pin 11 by an internal resistor and transistor. This generates a positive-going ramp voltage.

6. Buffer stage (pin 4)

The buffer stage consists of two emitter followers. The ramp voltage is fed via the buffer stage and is available at pin 4 with a low ohmic output impedance. With R4 and P1 it generates a ramp function, which, together with the feedback network of the deflection yoke, gives a high degree of linearity at the picture tube. The linearity can be adjusted by P1.

7. Preamplifier (pin 5)

The preamplifier is a differential amplifier. The non-inverting input is fixed at about 2 V by an internal voltage divider. The inverting input at pin 5 is connected to the ramp voltage via R3 and feedback network P2, R5 - R11, R15, R16, C7 , C10 and C11 .

8. Power output stage (pin 7)

The power output stage is an amplifier with a quasi-complementary class-B output. The output is connected to pin 7.

The power stage includes SOAR and thermal protection .

9. Flyback generator (pin 9)

The flyback generator has an external capacitor C8 at pin 9. During scanning, the internal circuit switches pin 9 almost to ground; thereby C8 is charged by the supply voltage via external components R14 and D2.

During the flyback time pin 9 is switched almost to the supply voltage, so that the supply voltage for the power output stage (pin 6) is nearly doubled. This high flyback voltage ensures a very short flyback time.

10. Guard circuit (pin 3)

When the vertical deflection current is absent (e.g. short circuit, or open circuit of the yoke) the guard circuit changes the blanking pulse at pin 3 into a DC signal which blanks the beam current to protect the screen.

Also an oscillator defect (C1 short-circuited or R1 disconnected from pin 1) switches on the guard circuit.

11. Voltage stabilizer

The voltage stabilizer circuit provides a stable operating voltage of about 7.5 V for several circuits of the TDA4800.

Vertical deflection circuit for monitor applications

TDA4800

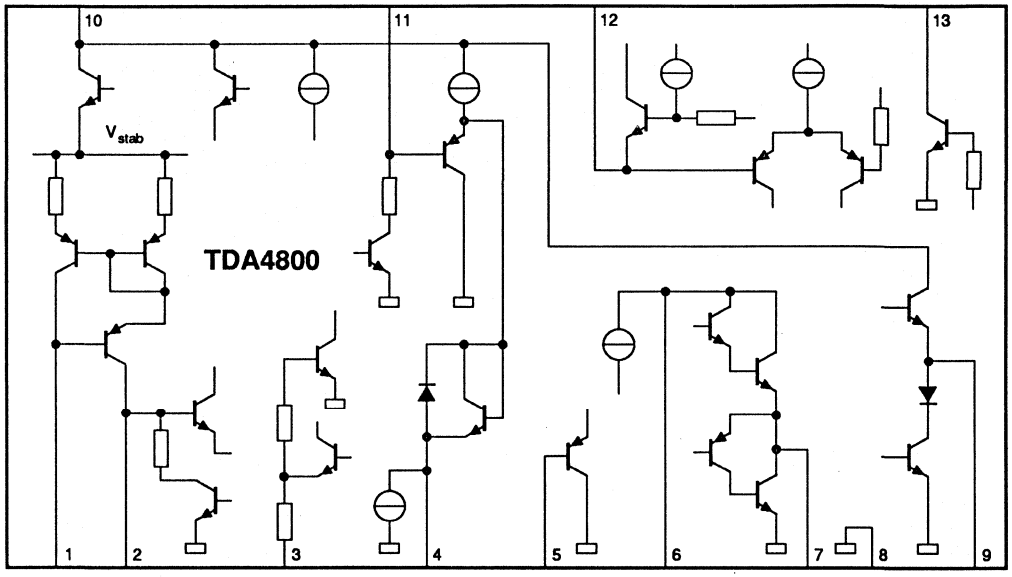


Fig.2 Internal circuits.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC_R	1	oscillator resistor
OSC_C	2	oscillator capacitor
SYB_O	3	sync. input, blanking pulse output
S_{OUT}	4	sawtooth output
PRE_I	5	preamplifier input
P_{SUP}	6	power supply
OUTP	7	deflection output
GND	8	ground
C_{FLY}	9	pin for the flyback generator capacitor
V_P	10	supply voltage
S_{GEN}	11	sawtooth generator
BP_{DU}	12	blanking pulse duration
FRQ_C	13	frequency criterion

PIN CONFIGURATION

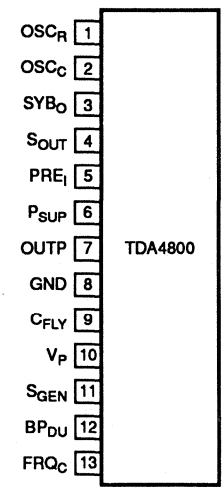


Fig. 3 Pin configuration.

Vertical deflection circuit for monitor applications

TDA4800

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_2	voltages		0	6	V
V_{11}			0	24	V
V_{12}			0	6	V
V_{13}			0	50	V
V_{10}	supply voltages (V_P)		0	50	V
V_9			0	50	V
V_7			0	60	V
V_6			0	60	V
V_5			0	6	V
V_4			0	24	V
V_3			−0.7	6	V
I_1	currents		0	−1	mA
I_3			+3	−10	mA
I_4			0	−5	mA
I_6, I_7, I_8		see note 1			
I_9			−1.2	+1.2	A
I_{11}			−0.1	+30	mA
T_{stg}	storage temperature range		−25	+150	°C
T_{amb}	operating ambient temperature range	see note 2	−20	+70	°C
$T_{j\ max}$	maximum junction temperature	see note 3	−	150	°C
P_{tot}	total power dissipation	see note 2	−	−	W
V_{ESD}	ESD sensitivity	see note 4	−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient free air	20	K/W
$R_{th\ j\text{-}mb}$	from junction to mounting base	5	K/W

Notes to the limiting values

1. I_6, I_7 and I_8 are limited by SOAR protection circuit that ensures that a short circuit between the output pin 7 and supply voltage or ground does not destroy the output stage. A short circuit may be soldered into the printed-circuit board or may sometimes (non-periodically) occur in the applied circuit.
2. The maximum value for the operating ambient temperature range and the power dissipation depends on the heatsink.
3. Internally limited by thermal protection: switching temperature point at T_j = 150 °C ± 8 °C.
4. Human body model: 1.5 kΩ, 100 pF, 5 pulses.

Vertical deflection circuit for monitor applications

TDA4800

CHARACTERISTICS

All voltages are measured to V_{GND} (pin 8); T_{amb} = 25 °C; V_P = 23 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_{10}	supply current	V_{10} = 25 V; V_5 = 3 V without load	–	10	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 1 V without load	–	20	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 3 V without load	–	5	–	mA
V_7	minimum output voltage	I_7 = 1 A	–	1.3	1.6	V
V_7	maximum output voltage	I_7 = –1 A	V_6 –2.2	V_6 –1.9	–	V
V_9	output voltage during flyback	I_9 = –1 A	–	V_{10} –2.2	–	V
I_7	output current		–	–	± 1.1	A
I_9	output current		–	–	± 1.1	A
I_5	preamplifier input current		–	–0.1	–	µA
V_1	stabilized voltage		6.1	6.8	7.3	V
V_3	blanking pulse output voltage		–	5.8	–	V
R_3	blanking pulse output resistance		–	410	–	Ω
I_3	blanking pulse output current		0	–	–3	mA
t_{bl}	blanking pulse duration	R = 100 kΩ; C = 10 nF (pin 12)	640	690	740	µs
V_{11}	output voltage ramp generator		0.3	–	20	V
I_{11}	output current ramp generator		–2	–	15×10^3	µA
V_{13}	output voltage frequency detector	lower frequency I_{13} = 1mA	–	1.0	–	V
I_{13}	leakage current frequency detector	higher frequency V_{13} = 50 V	–	1.0	–	µA
V_4	output voltage buffer stage		0	–	20	V
I_4	output current buffer stage		–	–	–4.0	mA
V_3	synchronizing input voltage	positive sync	1.0	–	6.0	V
V_3	synchronizing input voltage	negative sync	–0.5	–	–0.7	V
	tolerance of free running oscillator	without sync	–3.0	–	+ 3.0	%
$\Delta f/f / \Delta T_C$	oscillator temperature dependency	T_{case} = 20 °C to 100 °C	–	10^{-4}	–	K^{-1}
$\Delta f/f / \Delta V_P$	oscillator voltage dependency	V_P = 10 V to 30 V	–	4×10^{-4}	–	K^{-1}
	synchronizing range		f_o	–	$2f_o$	Hz

Vertical deflection circuit for monitor applications

TDA4800

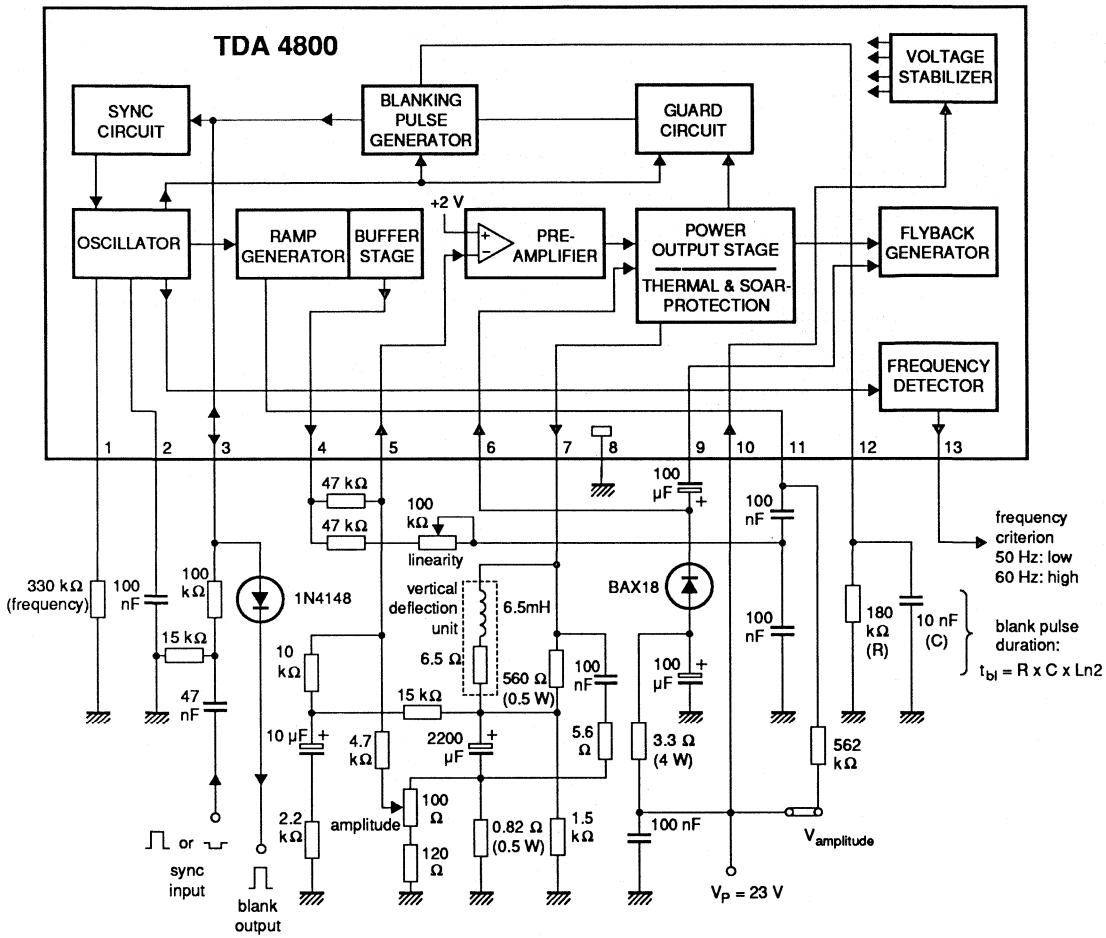


Fig.4 Test and application circuit.

Vertical deflection circuit for monitor applications

TDA4800

TDA4800 IN THE TEST AND APPLICATION CIRCUIT (see Fig.4)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
V_P	supply voltage		23	V
I_P	supply current		215	mA
V_7	DC output voltage		11.8	V
V_{7M}	peak output voltage		45	V
I_7	output current		0.8	A
$I_{Y(p-p)}$	vertical deflection current (peak to peak)		1.5	A
t_{fb}	flyback time		0.3	ms
t_{bl}	blanking pulse duration		1.25	ms
P_{tot}	total power dissipation		3.3	W
f_{osc}	free running oscillator frequency	without sync	45	Hz

Philips Components

Data sheet	
status	Preliminary specification
date of issue	June 1990

TDA4820T
Sync separation circuit for video applications

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7} = 1$ mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A

Sync separation circuit for video applications

TDA4820T

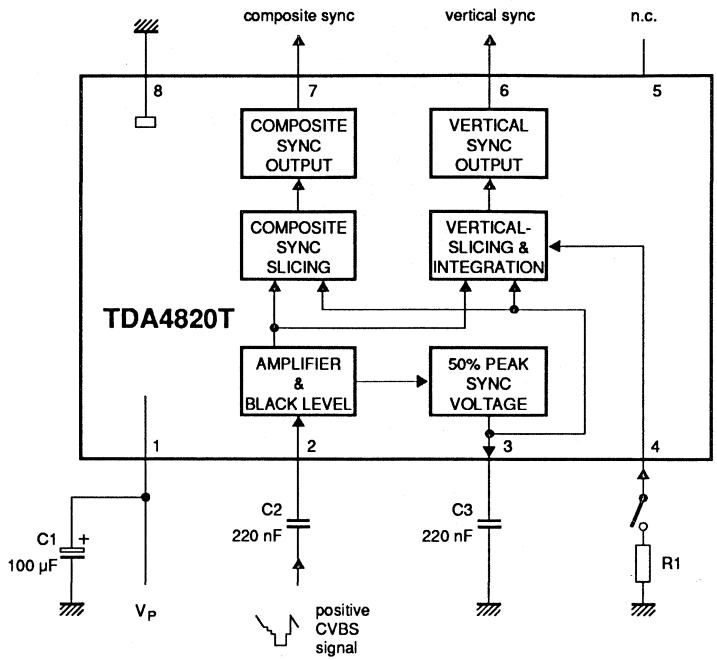


Fig. 1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

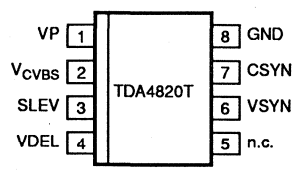


Fig. 2 Pin configuration.

Sync separation circuit for video applications

TDA4820T

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.

The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3.
A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.
With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.
The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded). Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be $\geq$ 3.3 kΩ. In this case t_{dV} is typically $\geq$ 23 µs.

Vertical sync output
Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

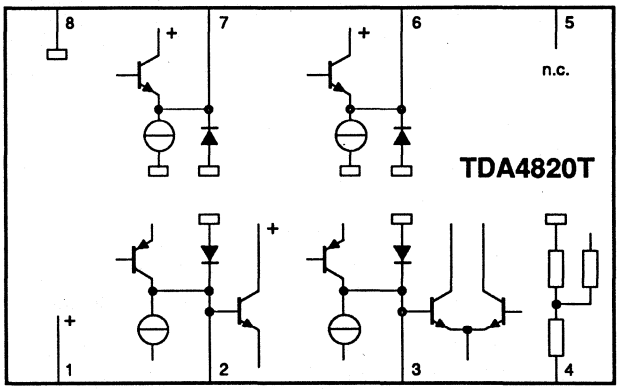


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	–0.5	6	V
I_o	output current (pin 6 and pin 7)	3	–10	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	–	150	°C
P_{tot}	total power dissipation	–	500	mW

Sync separation circuit for video applications

TDA4820T

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for 0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	50	300	500	mV
Z_s	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	µA
	charge currents of C2	sync below slicing level	–	–40	–	µA
		sync above slicing level	–	–25	–	µA
		during black level	–	–20	–	µA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	µA
	maximum charge current of C3		–	–345	–	µA
	reduced charge current of C3	during vertical sync	–	–255	–	µA
	charge current of C3	during sync pulse	–	–160	–	µA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: C_L ≤ 5 pF; R_L ≥ 100 kΩ	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	µs
		pin 4 grounded	11	18	25	µs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	I_6 = –1 mA	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	I_7 = –3 mA	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7}$ = 1 mA	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	µs

Sync separation circuit for video applications

TDA4820T

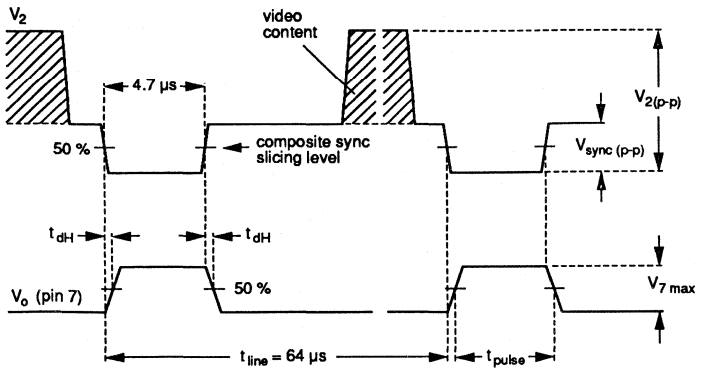
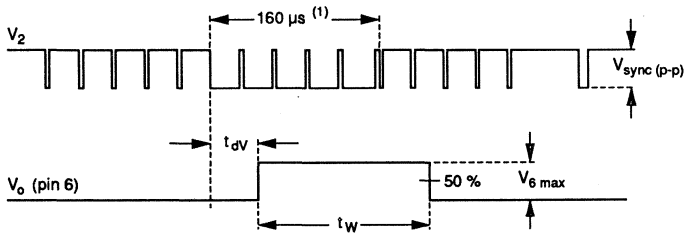


Fig.4 Typical horizontal sync signal.



(1) due to 625 line standard

Fig.5 Typical vertical sync signal.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL, plastic (SOT102).

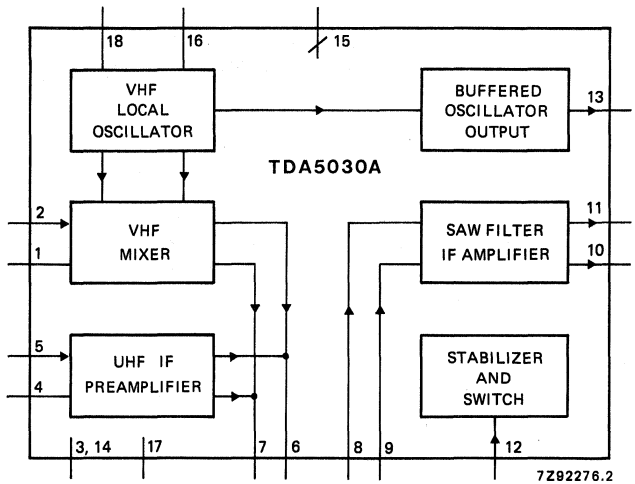


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15-3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	$V_{15}+0,3$	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	55	K/W

CHARACTERISTICS

Measured in circuit of Fig. 2, $V_P = V_{15-3} = 12$ V, $T_{amb} = 25$ °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	V_{15-3}	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	$V_{15}+0,3$	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-14}	100	–	–	dBμV
Voltage gain		A_v	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Yc_{2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			−63	−112	−134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

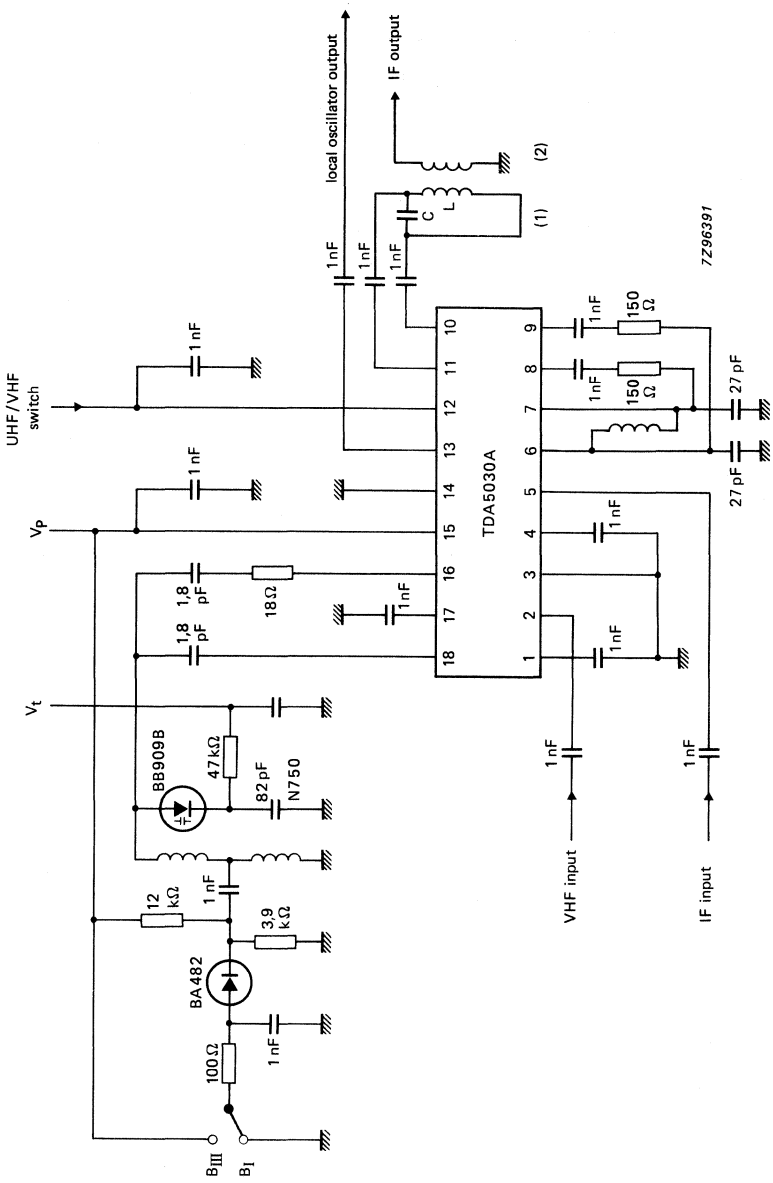


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.

(2) Turns ratio = 7 : 1, load = 50 Ω.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030AT provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 11, 12, 13 and 14

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	25	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	–55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	–	+ 80	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

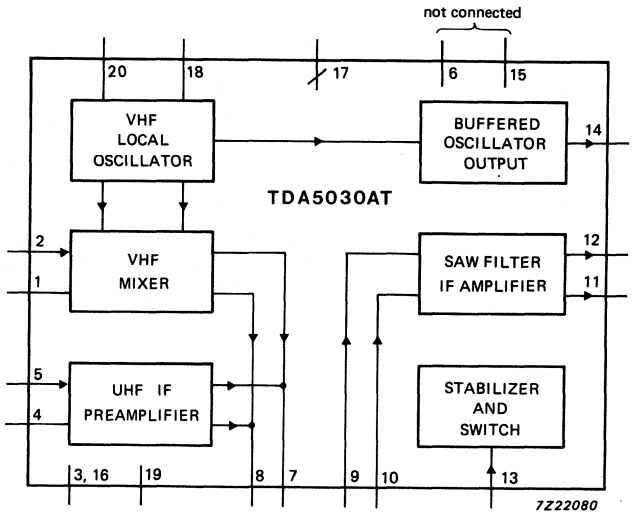


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-3}$	–	14	V
Input voltage (pins 1, 2, 4 and 5)	V_i	0	5	V
VHF switching voltage (pin 13)	V_{13}	0	V_P+0,3	V
Output current (pins 11, 12 or 14)	$-I_{11,12,14}$	–	10	mA
Short-circuit time on outputs (pins 11, 12 and 14)	t_{sc}	–	10	s
Storage temperature range	T_{stg}	–55	+125	°C
Operating ambient temperature range	T_{amb}	–25	+ 80	°C
Junction temperature range	T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

$V_P = V_{17-3} = 12$ V; $T_{amb} = 25$ °C; measured in circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 17)		V_{17-3}	10	–	13,2	V
Supply current		I_{17}	–	42	55	mA
Switch voltage level for VHF (pin 13)		V_{13}	0	–	2,5	V
Switch voltage level for UHF (pin 13)		V_{13}	9,5	–	V_P+0,3	V
Switch current	UHF selected	I_{13}	–0,05	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor (pin 2)	f = 50 MHz	NF	–	7,5	9	dB
	f = 225 MHz	NF	–	9	10	dB
	f = 300 MHz	NF	–	10	12	dB
	f = 470 MHz	NF	–	11	13	dB
Optimum source conductance (pin 2)	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
	f = 470 MHz	G	–	1,9	–	mS
Input conductance (pin 2)	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
	f = 470 MHz	G_i	–	1,45	–	mS
Input capacitance (pin 2)	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	96	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-16}	100	–	–	dBμV
Input voltage for 100 kHz pulling	f = 470 MHz	V_{2-3}	73	–	–	dBμV
Voltage gain		A_v	23	25	27	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance (pin 5)		G_i	–	0,3	–	mS
Input capacitance (pin 5)		C_i	–	3,0	–	pF
Noise factor (pin 5)		NF	–	5	6	dB
Optimum source conductance (pin 5)		G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		V_{5-16}	88	90	–	dBμV
Voltage gain		A_v	32	34	36	dB
VHF mixer						
Conversion transadmittance (pins 2 to 7, 8)		$Yc_{2-7,8}$	–	5,7	–	mS
Output impedance (pins 7 and 8)		Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{11,12}$ = 2 kΩ; f = 36 MHz	$Z_{9,10}$	–	300+ j100	–	Ω
Transimpedance		$Z_{9,10-11,12}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage (pin 14)	R_L = 75 Ω					
	f < 100 MHz	V_{14}	14	20	–	mV
	f > 100 MHz	V_{14}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{14}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

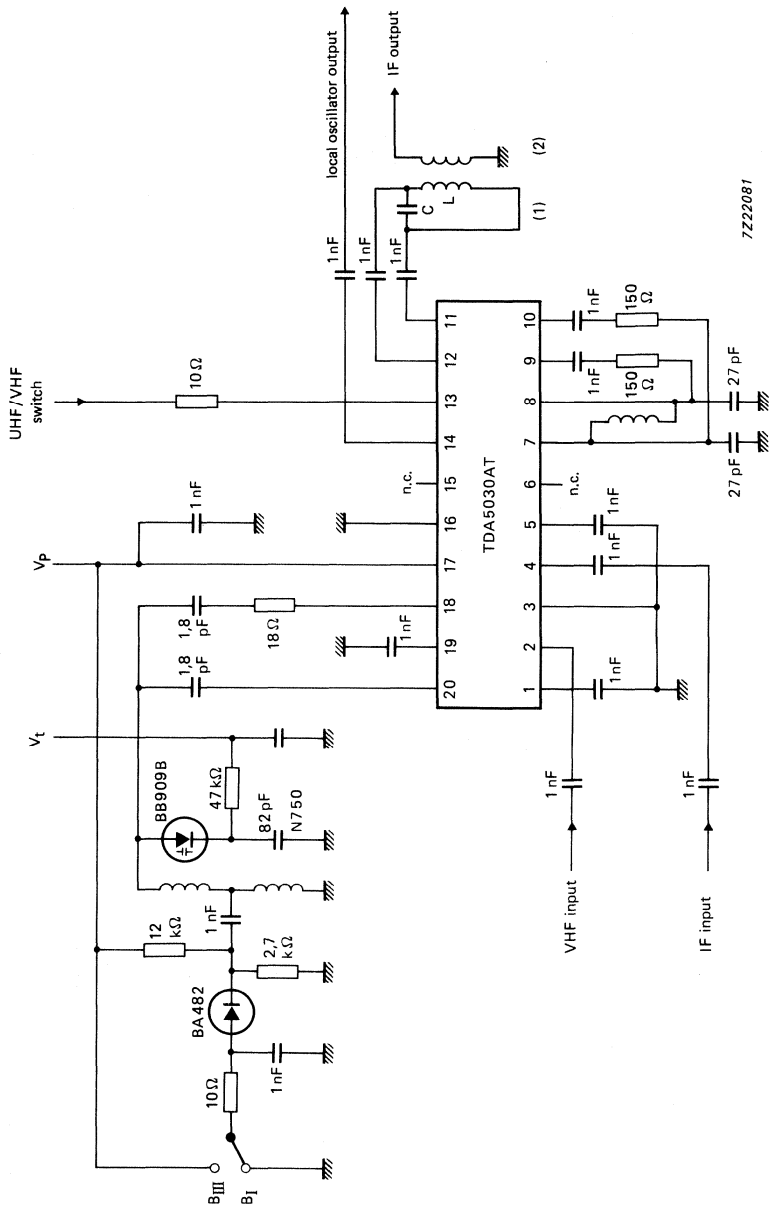


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

BRUSHLESS DC MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The TDA5140 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a VHS video casette recorder motor.

Features

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuit
- Three push-pull outputs:
  - 0.6 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range	note 1	V_P	4	–	18	V
Supply current range	note 2	I_P	–	3.3	4.5	mA
Input voltage to the output driver stages	see Fig.1	V_{VMOT}	0	–	16	V
Driver output voltage range	I_O = 0 mA	V_O	0.2	–	V_{VMOT}–0.9	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.

PACKAGE OUTLINE

TDA5140P: 18-lead DIL; plastic with internal heatspreader (SOT102).
TDA5140T: 20-lead mini-pack; plastic (SO20; SOT163A).

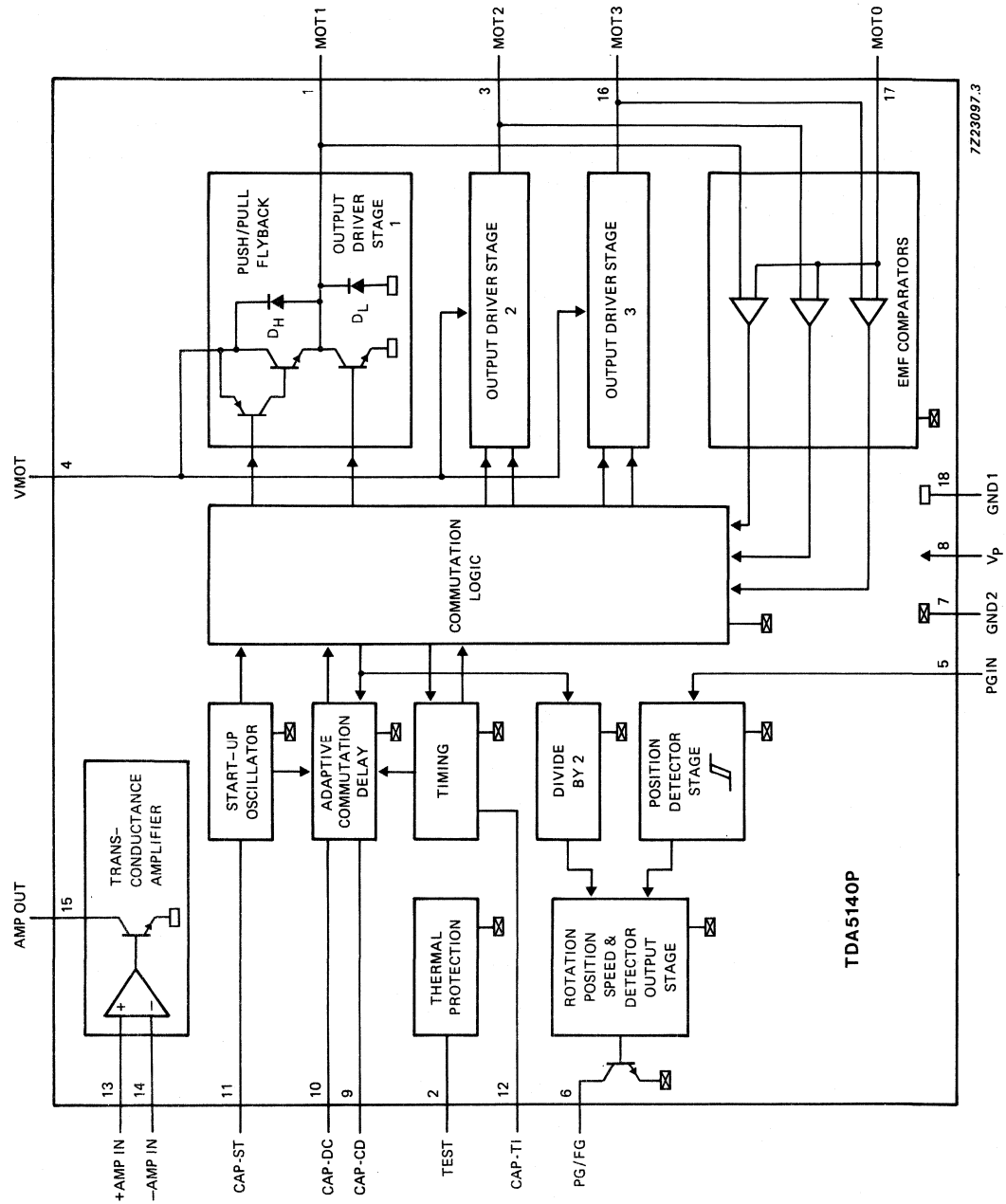


Fig.1 Block diagram; SOT102 (DIL 18).

PINNING

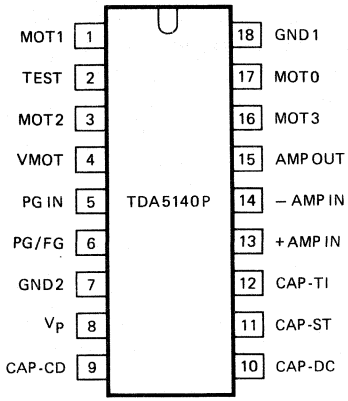


Fig.2(a) Pinning diagram; SOT102 (DIL 18).

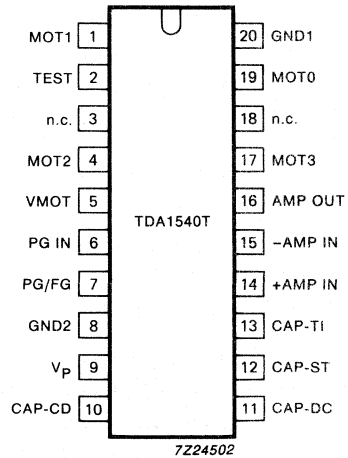


Fig.2(b) Pinning diagram; SOT163A (SO20).

DEVELOPMENT DATA

SOT102	SO20	signal	function
1	1	MOT1	driver output 1
2	2	TEST	test input/output
	3	n.c.	not connected
3	4	MOT2	driver output 2
4	5	VMOT	input voltage for the output driver stages
5	6	PG IN	position generator: input from the position detector sensor to the position detector stage (optional). Only if an external position coil is used.
6	7	PG/FG	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
7	8	GND2	ground supply return for control circuits
8	9	V_P	positive supply voltage
9	10	CAP-CD	external capacitor connection for adaptive commutation delay timing
10	11	CAP-DC	external capacitor connection for adaptive commutation delay timing copy
11	12	CAP-ST	external capacitor connection for start-up oscillator
12	13	CAP-TI	external capacitor connection for timing
13	14	+AMP IN	non-inverting input of the transconductance amplifier
14	15	–AMP IN	inverting input of the transconductance amplifier
15	16	AMP OUT	transconductance amplifier output (open collector)
16	17	MOT3	driver output 3
17	19	MOT0	input from the start point of the motor coils
	18	n.c.	not connected
18	20	GND1	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5140 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (0.6 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal
- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Additional uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Input voltage; all pins except VMOT	$V_I < 18$ V	V_I	−0.3	$V_P + 0.5$	V
VMOT input voltage		V_{VMOT}	−0.5	17	V
Output voltage; AMP OUT and PG/FG		V_O	GND	V_P	V
Output voltage; MOT0, MOT1, MOT2 and MOT3		V_O	−1	$V_{VMOT} + V_D$	V
Input voltage; CAP-ST, CAP-TI, CAP-CD and CAP-DC		V_I	–	2.5	V
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	0	70	°C
Total power dissipation		P_{tot}		see Fig. 3	
Electrostatic voltage; handling*		V_{es}	–	500	V

THERMAL RESISTANCE

Junction average to ambient, on a vertically mounted printed-circuit board	$R_{th\ j\text{-}a}$	=	50 K/W
Junction (peak) to ambient, on a printed-circuit board	$R_{th\ j\text{-}p}$	=	75 K/W
Junction average to ambient (SO20; copper lead frame)	$R_{th\ j\text{-}a}$	=	90 K/W

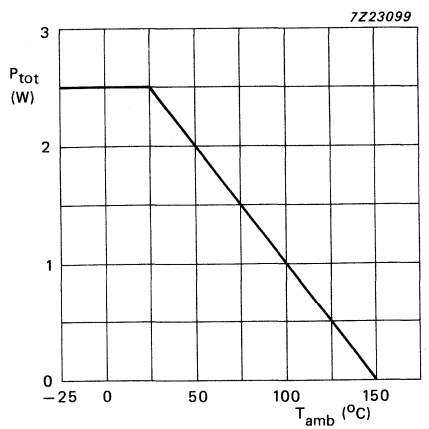


Fig.3(a) Power derating curve; SOT102 (DIL 18).

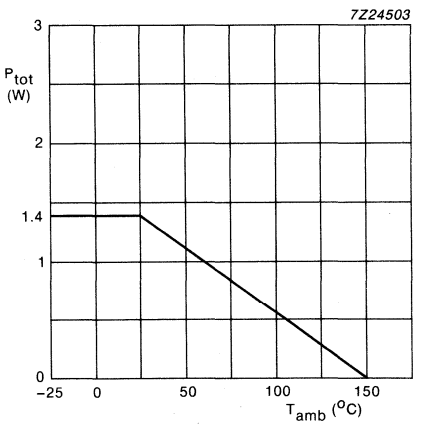


Fig.3(b) Power derating curve; SO20.

* Equivalent to discharging a 100 pF capacitor through a 0 Ω resistor.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	4	–	18	V
Input current range	note 2	I_P	–	3.3	4.5	mA
Input voltage to the driver output stages	see Fig.1	V_{VMOT}	0	–	16	V
Thermal protection						
Local temperature at temperature sensor causing shut-down		T_{SD}	130	140	150	°C
Reduction in temperature before switch-on	after shut-down	ΔT	–	T_{SD}–30	–	°C
MOT0						
Input voltage range		V_I	–0.5	–	V_{VMOT}	V
Input bias current	0.5 V < V_I < VMOT–1.5 V	I_I	–10	–	0	μA
Comparator switching level	note 3	± V_{CSW}	–	25	–	mV
Variations in comparator switching levels		ΔV_{CS}	–	0	–	mV
Comparator input hysteresis		V_H	–	75	–	μV
MOT1, MOT2 and MOT3	driver active					
Driver output voltage range	I_O = 100 mA	V_O	*	–	*	V
	I_O = 500 mA or 400 mA at T_{amb} = +70 °C	V_O	0.6	–	V_{VMOT}–1.5	V
Variation in saturation voltage lower transistors	I_O = 100 mA	ΔV_{OL}	–	–	180	mV
Variation in saturation voltage upper transistors	I_O = –100 mA	ΔV_{OH}	–	–	180	mV
Current limiting	lower transistor V_{CE} = 6 V	I_{LIM}	600	850	1000	mA
Diode forward voltage (D_H)	notes 4 and 5; see Fig.1; I_O = –500 mA	V_{DHF}	–	–	1.5	V
Diode forward voltage (D_L)	notes 4 and 5; see Fig.1; I_O = 500 mA	V_{DLF}	–1.5	–	–	V
Peak diode current	note 5	I_{DM}	–	–	1	A

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
VMOT						
Input voltage range		V_{MOT}	0	–	16	V
+AMP IN and –AMP IN						
Input voltage range		V_{IAMP}	–0.3	–	V_P–1.7	V
Differential mode voltage without 'latch-up'		$\pm V_{IAMP}$	–	–	V_P	V
Input bias current		I_{LI}	–	–	500	nA
Input capacitance		C_I	–	4	–	pF
Input offset voltage		V_{OFFSET}	–	–	3	mV
AMP OUT						
Output sink current		I_I	40	–	–	mA
Saturation voltage	I_I = 40 mA	V_{SAT}	–	–	*	V
Maximum output voltage		V_{Omax}	18	1.5	–	V
Slew rate	R_L = 330 Ω; C_L = 50 pF	SR	40	–	–	mA/μs
Transfer gain		G_{TRAN}	0.3	–	–	S
PG IN						
Input voltage		V_I	–0.3	–	V_P–1.7	V
Input bias current		I_b	–	–	500	nA
Input resistance		R_I	9	20	45	kΩ
Comparator switching level		V_{CSW}	–	80	–	mV
Comparator input hysteresis		$\pm V_H$	–	8	–	mV
PG/FG						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Maximum output voltage HIGH		V_{OHmax}	V_P	–	–	V
Transition time	HIGH-to-LOW; C_L = 50 pF; R_L = 10 kΩ	t_{THL}	–	0.5	–	μs
Ratio of PG/FG frequency and commutation frequency			–	1 : 2	–	
Duty factor		δ	–	50	–	%
Pulse width LOW	after a PG IN pulse	t_{PL}	–	10	–	μs

* Value to be fixed.

CHARACTERISTICS (continued)

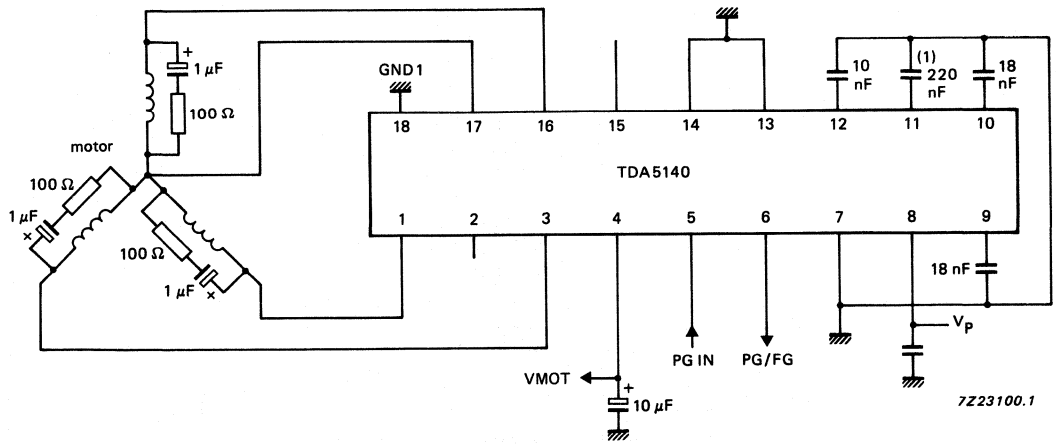
parameter	condition	symbol	min.	typ.	max.	unit
CAP-ST						
Output sink current		I_I	1.5	2.0	2.5	μA
Output source current		I_O	−2.5	−2.0	−1.5	μA
Lower switching level		V_{SWL}	–	0.20	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-TI						
Output sink current		I_I	–	28	–	μA
Output source current HIGH		I_{OH}	–	−60	–	μA
Output source current LOW		I_{OL}	–	−5	–	μA
Lower switching level		V_{SWL}	–	0.20	–	V
Middle switching level		V_{SWM}	–	0.30	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-CD						
Output sink current		I_I	*	17	*	μA
Output source current		I_O	*	−8.1	*	μA
Ratio of sink to source current		–	2	2.1	2.2	
Input voltage level LOW		V_{IL}	–	0.9	–	V
CAP-DC						
Output sink current		I_I	*	16	*	μA
Output source current		I_O	*	−16	*	μA
Ratio of sink to source current		I_I/I_O	0.95	1	1.05	

Notes to the characteristics

1. An unstabilized supply can be used.
2. VMOT = V_P, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in high impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

* Value to be fixed.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA).

DEVELOPMENT DATA

Introduction

Refer to Fig.5. Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

APPLICATION INFORMATION (continued)

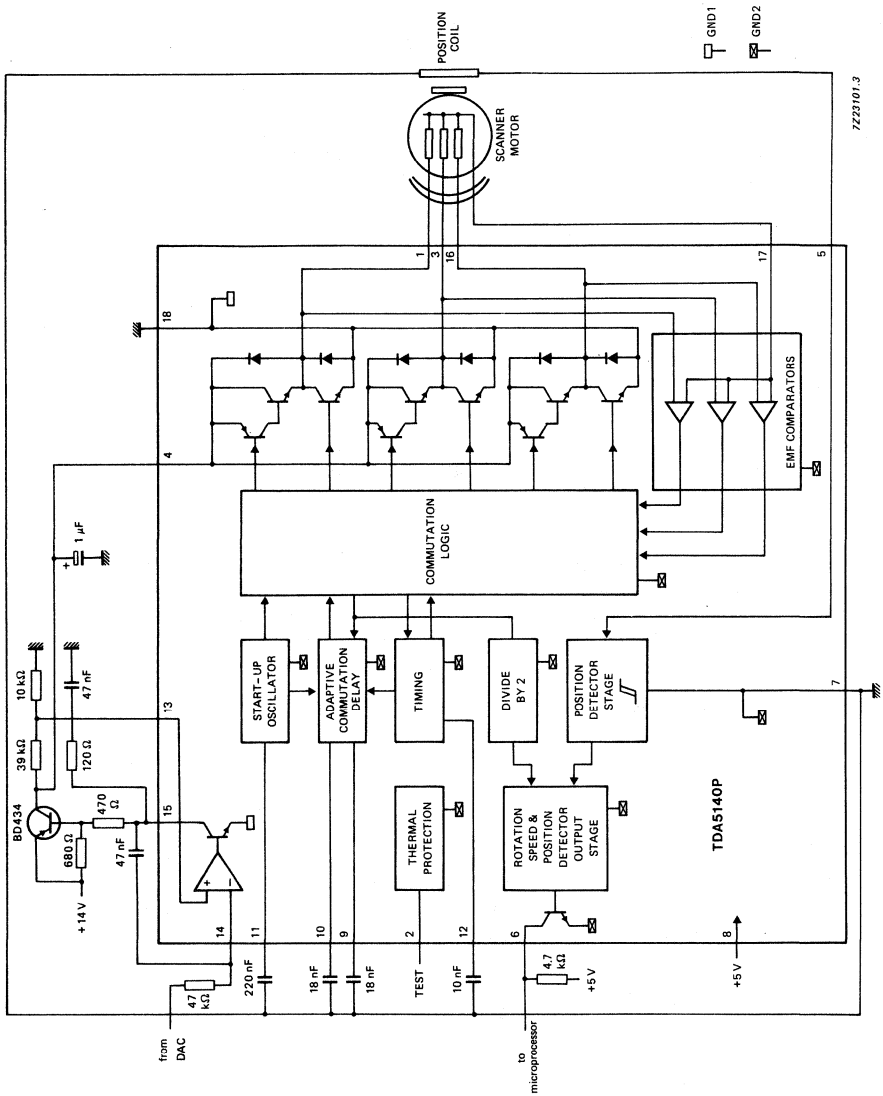


Fig.5 Typical application of the TDA5140 as a scanner driver, with use of OTA.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patent pending), possibility of using a pick-up coil without bias current.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit. These are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

DEVELOPMENT DATA

The Start Capacitor (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C)s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where: K_t = torque constant (N·m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J (kg/m^2)

Example: J = 72 x 10^{-6}kg/m^2, K = 25 x 10^{-3}N. m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The Adaptive Commutation Delay (CAP-CD and CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 10 μA and the discharging current 20 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{c1}:

$C = 7692/f_{c1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 20 μA.

maximum delay = (0.065 x C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 7692/400 = 19.2 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 6 illustrates typical voltage waveforms.

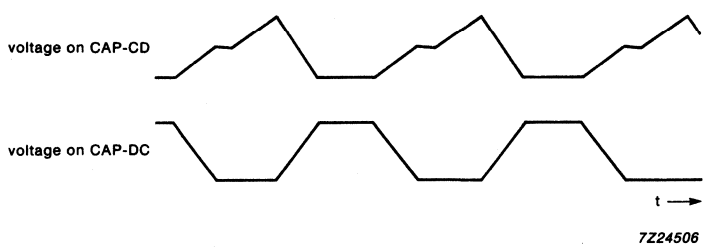


Fig.6 CAP-CD and CAP-DC voltage waveforms in normal running mode.

The Timing Capacitor (CAP-T1)

Capacitor CAP-T1 is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time. The EMF usually recovers within a short time if the motor is running normally ($<<$ ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer ($>>$ ms). A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 62 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 24 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-T1 is given by:

$$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.7.

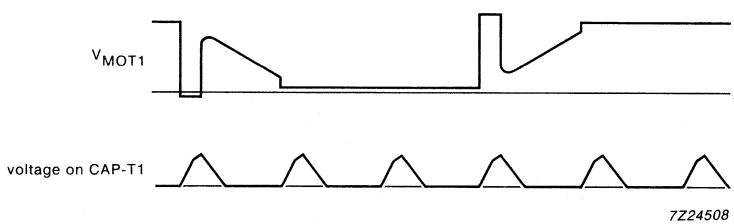


Fig.7 Typical CAP-T1 and V_{MOT1} voltage waveforms in normal running mode.

Note

If the chosen value of CAP-T1 is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The External Damping Components

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5140. This distortion may influence the correct functioning of the TDA5140, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 μs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 μs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp-8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 μF (use 1 μF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 μs. Eddy currents will also contribute to this phase shift. A shift of 20 μs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or, 0.1 mm on a VHS scanner drum.

Other Design Aspects

There are other design aspects concerning the application of the TDA5140 besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG Signal

The FG signal is generated in the TDA5140 by using the zero-crossings of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG Signal

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PGIN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 15 μs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.8).

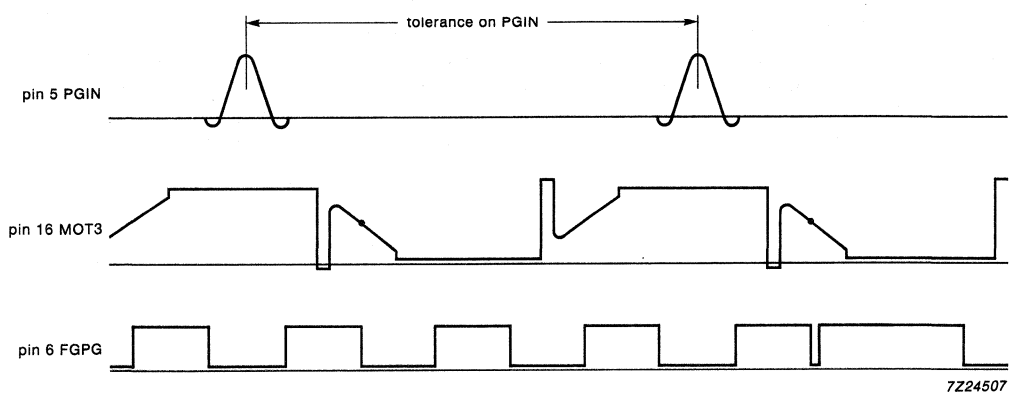


Fig.8 Timing of the FG and PGIN signals.

APPLICATION INFORMATION (continued)

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PGIN on pin 5) must sense a positive going edge (> 80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.8).

The voltage requirements of the PGIN input are such that a cheap pick-up coil can be used as a sensor (see Fig.9).

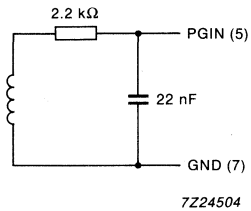


Fig.9 Pick-up coil as PG sensor.

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PGIN input must be grounded, this will result in a 50% duty factor FG signal.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P - 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analogue control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analogue or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analogue control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.5).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.10).

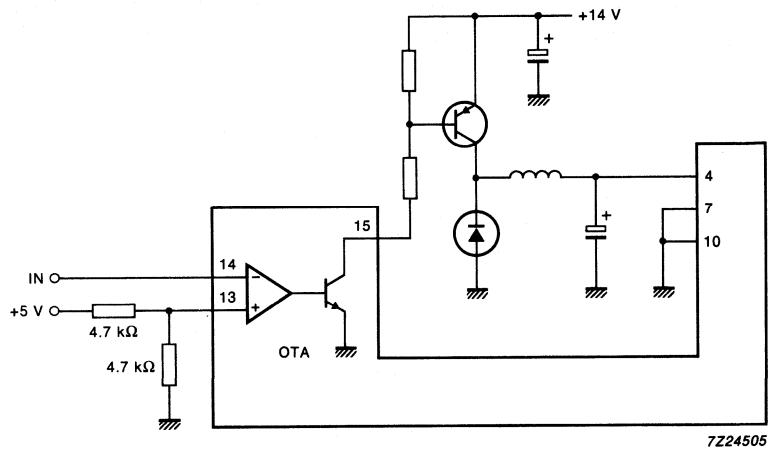


Fig.10 PWM drive of the output stages, OTA used as a level converter.

A further aspect of motor control is current or voltage control; the TDA5140 is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pin 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.5 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5140 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 4 then the motor will generate a braking torque that is proportional to the current.

APPLICATION INFORMATION (continued)

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+ 15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 4) may cause higher currents than allowed (> 1 A). These currents must be limited externally.

BRUSHLESS DC MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a VHS video casette recorder motor.

Features

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuit
- Three push-pull outputs:
  - 0.6 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range	note 1	V_P	4	–	18	V
Supply current range	note 2	I_P	–	3.7	5.0	mA
Input voltage to the output driver stages	see Fig.1	V_{VMOT}	3	–	16	V
Driver output voltage range	I_O = 0 mA	V_O	0.2	–	V_{VMOT}–0.9	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

PACKAGE OUTLINES

TDA5140A: 18-lead DIL; plastic with internal heatspreader (SOT102).
TDA 5140AT: 20-lead mini-pack; plastic (SO20; SOT163A).

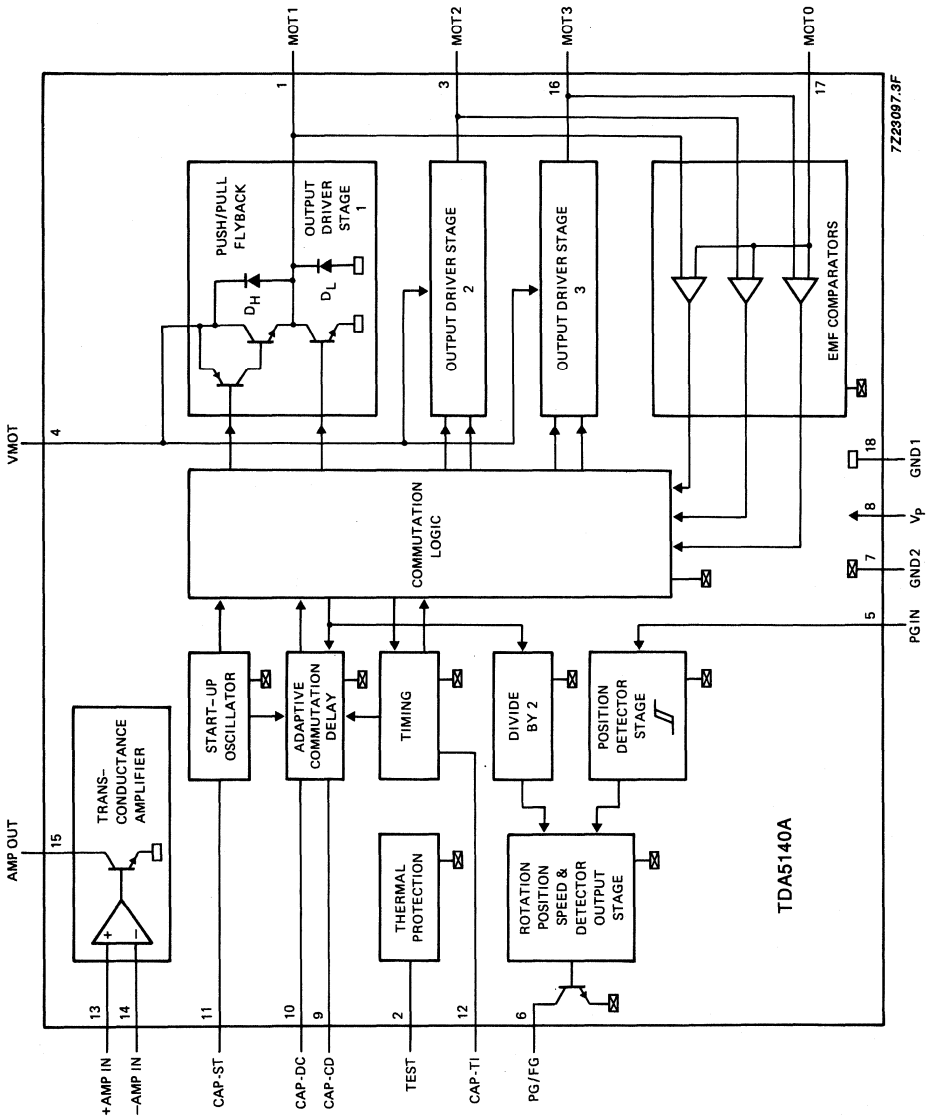


Fig.1 Block diagram; SOT102 (DIL 18).

PINNING

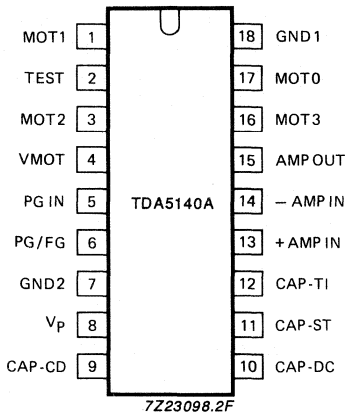


Fig.2(a) Pinning diagram; SOT102 (DIL 18).

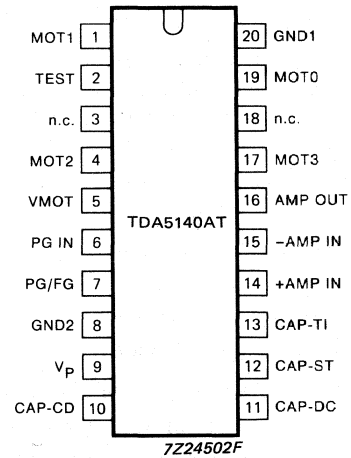


Fig.2(b) Pinning diagram; SOT163A (SO20).

SOT102	SO20	signal	function
1	1	MOT1	driver output 1
2	2	TEST	test input/output
	3	n.c.	not connected
3	4	MOT2	driver output 2
4	5	VMOT	input voltage for the output driver stages
5	6	PG IN	position generator: input from the position detector sensor to the position detector stage (optional). Only if an external position coil is used.
6	7	PG/FG	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
7	8	GND2	ground supply return for control circuits
8	9	V_P	positive supply voltage
9	10	CAP-CD	external capacitor connection for adaptive commutation delay timing
10	11	CAP-DC	external capacitor connection for adaptive commutation delay timing copy
11	12	CAP-ST	external capacitor connection for start-up oscillator
12	13	CAP-TI	external capacitor connection for timing
13	14	+AMP IN	non-inverting input of the transconductance amplifier
14	15	–AMP IN	inverting input of the transconductance amplifier
15	16	AMP OUT	transconductance amplifier output (open collector)
16	17	MOT3	driver output 3
17	19	MOT0	input from the start point of the motor coils
	18	n.c.	not connected
18	20	GND1	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (0.6 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal
- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Additional uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Input voltage; all pins except VMOT	$V_I < 18$ V	V_I	−0.3	$V_P + 0.5$	V
VMOT input voltage		V_{VMOT}	−0.5	17	V
Output voltage; AMP OUT and PG/FG		V_O	GND	V_P	V
Output voltage; MOT0, MOT1, MOT2 and MOT3		V_O	−1	$V_{VMOT} + V_D$	V
Input voltage; CAP-ST, CAP-TI, CAP-CD and CAP-DC		V_I	–	2.5	V
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−10	70	°C
Total power dissipation		P_{tot}	see Fig.3		
Electrostatic voltage; handling		V_{es}	–	500	V

ESD

In accordance with MIL STD883C – Method 3015 (HMB 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin as a function of ground. Class 1.

THERMAL RESISTANCE

Junction average to ambient, on a vertically mounted printed-circuit board	$R_{th\ j\text{-}a}$	=	50 K/W
Junction (peak) to ambient, on a printed-circuit board	$R_{th\ j\text{-}p}$	=	75 K/W
Junction average to ambient (SO20; copper lead frame)	$R_{th\ j\text{-}a}$	=	90 K/W

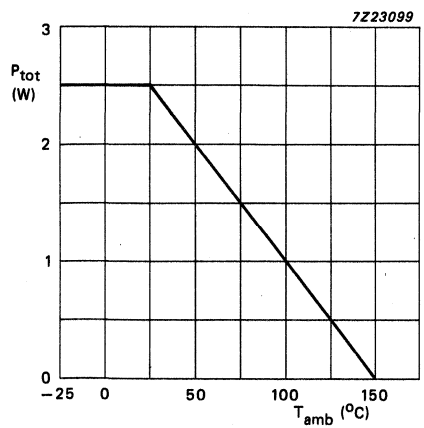


Fig.3(a) Power derating curve; SOT102 (DIL 18).

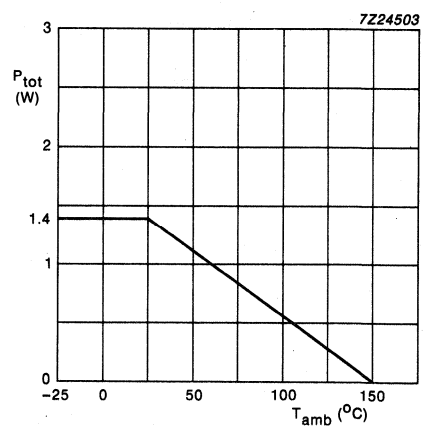


Fig.3(b) Power derating curve; SO20.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	4	–	18	V
Input current range	note 2	I_P	–	3.7	5.0	mA
Input voltage to the driver output stages	see Fig.1	V_{VMOT}	3	–	16	V
Thermal protection						
Local temperature at temperature sensor causing shut-down		T_{SD}	130	140	150	°C
Reduction in temperature before switch-on	after shut-down	ΔT	–	$T_{SD}-30$	–	°C
MOT0						
Input voltage range		V_I	−0.5	–	V_{VMOT}	V
Input bias current	0.5 V < V_I < VMOT−1.5 V	I_I	−10	–	–	μA
Comparator switching level	note 3	$\pm V_{CSW}$	20	30	40	mV
Variations in comparator switching levels		ΔV_{CS}	−3	0	+3	mV
Comparator input hysteresis		V_H	–	75	–	μV
MOT1, MOT2 and MOT3	driver active					
Driver output voltage range	I_O = 100 mA	V_O	0.4	–	$V_{VMOT}-1.2$	V
	I_O = 500 mA or 400 mA at T_{amb} = +70 °C	V_O	0.6	–	$V_{VMOT}-1.5$	V
Variation in saturation voltage lower transistors	I_O = 100 mA	ΔV_{OL}	–	–	180	mV
Variation in saturation voltage upper transistors	I_O = −100 mA	ΔV_{OH}	–	–	180	mV
Current limiting	lower transistor V_{CE} = 6 V; T_{amb} = −10 to +70 °C	I_{LIM}	600	850	1000	mA
Diode forward voltage (D_H)	notes 4 and 5; see Fig.1; I_O = −500 mA	V_{DHF}	–	–	1.5	V
Diode forward voltage (D_L)	notes 4 and 5; see Fig.1; I_O = 500 mA	V_{DLF}	−1.5	–	–	V
Peak diode current	note 5	I_{DM}	–	–	1	A

parameter	condition	symbol	min.	typ.	max.	unit
VMOT						
Input voltage range		V_{MOT}	3	–	16	V
+AMP IN and –AMP IN						
Input voltage range		V_{IAMP}	–0.3	–	V_P–1.7	V
Differential mode voltage without 'latch-up'		$\pm V_{IAMP}$	–	–	V_P	V
Input bias current		I_{LI}	–	–	650	nA
Input capacitance		C_I	–	4	–	pF
Input offset voltage		V_{OFFSET}	–	–	5	mV
AMP OUT						
Output sink current		I_I	40	–	–	mA
Saturation voltage	I_I = 40 mA	V_{SAT}	–	1.5	2.1	V
Maximum output voltage		V_{Omax}	18	–	–	V
Slew rate	R_L = 330 Ω; C_L = 50 pF	SR	–	60	–	mA/μs
Transfer gain		G_{TRAN}	0.3	–	–	S
PG IN						
Input voltage		V_I	–0.3	–	5	V
Input bias current		I_b	–	–	650	nA
Input resistance	T_{amb} = –10 to +70 °C	R_I	5	–	25	kΩ
Comparator switching level		V_{CSW}	86	–	107	mV
Comparator input hysteresis		$\pm V_H$	–	8	–	mV
PG/FG						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Maximum output voltage HIGH		V_{OHmax}	V_P	–	–	V
Transition time	HIGH-to-LOW; C_L = 50 pF; R_L = 10 kΩ	t_{THL}	–	0.5	–	μs
Ratio of PG/FG frequency and commutation frequency			–	1 : 2	–	
Duty factor		δ	–	50	–	%
Pulse width LOW	after a PG IN pulse	t_{PL}	5	–	18	μs

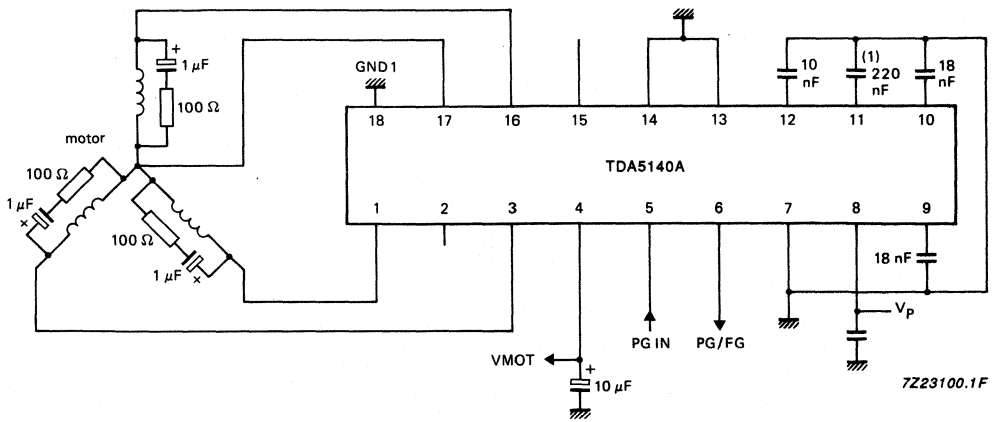
CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
CAP-ST						
Output sink current		I_I	1.5	2.0	2.5	μA
Output source current		I_O	−2.5	−2.0	−1.5	μA
Lower switching level		V_{SWL}	–	0.20	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-TI						
Output sink current		I_I	–	28	–	μA
Output source current HIGH		I_{OH}	–	−57	–	μA
Output source current LOW		I_{OL}	–	−5	–	μA
Lower switching level		V_{SWL}	–	0.20	–	V
Middle switching level		V_{SWM}	–	0.30	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-CD						
Output sink current		I_I	10.6	16.2	22	μA
Output source current		I_O	−5.3	−8.1	−11	μA
Ratio of sink to source current		I_I/I_O	1.85	2.05	2.25	
Input voltage level LOW		V_{IL}	0.85	0.875	0.90	V
Input voltage level HIGH		V_{IH}	2.3	2.4	2.5	V
CAP-DC						
Output sink current		I_I	10.1	15.5	20.9	μA
Output source current		I_O	-20.9	−15.5	−10.1	μA
Ratio of sink to source current		I_I/I_O	0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. VMOT = V_P, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in high impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction

Refer to Fig.5. Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

APPLICATION INFORMATION (continued)

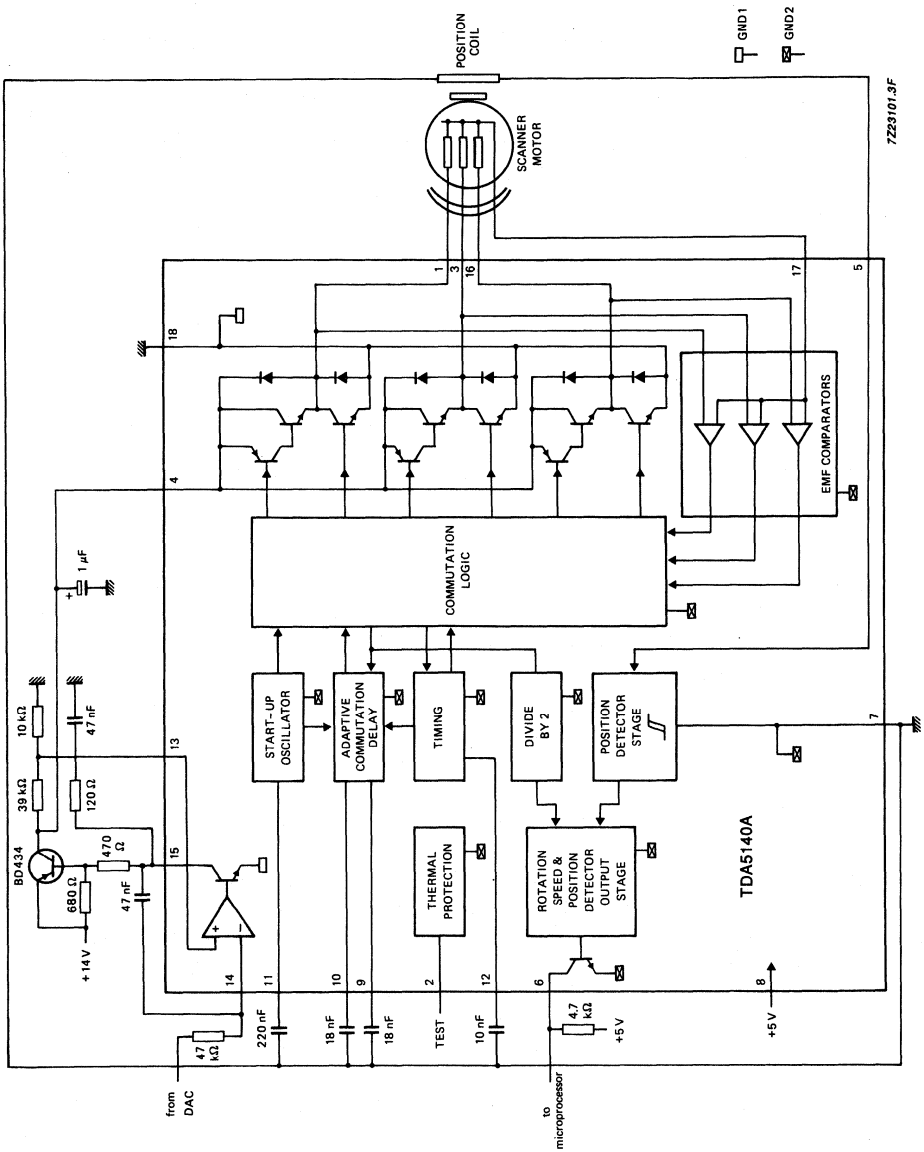


Fig. 5 Typical application of the TDA5140A as a scanner driver, with use of OTA.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140A also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140A is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patent pending), possibility of using a pick-up coil without bias current.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit. These are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

The Start Capacitor (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$t_{start} = (2.15 \times C)s$ (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140A will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where: K_t = torque constant (N·m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ kg.m^2, $K = 25 \times 10^{-3}$N. m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The Adaptive Commutation Delay (CAP-CD and CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{c1}:

$C = 6231/f_{c1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 x C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 6 illustrates typical voltage waveforms.

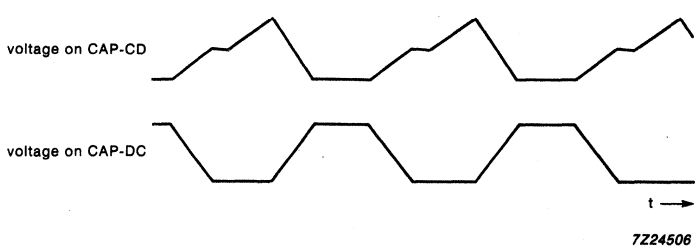


Fig.6 CAP-CD and CAP-DC voltage waveforms in normal running mode.

The Timing Capacitor (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time. The EMF usually recovers within a short time if the motor is running normally ($<<$ ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer ($>>$ ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-T1 is given by:

$$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.7.

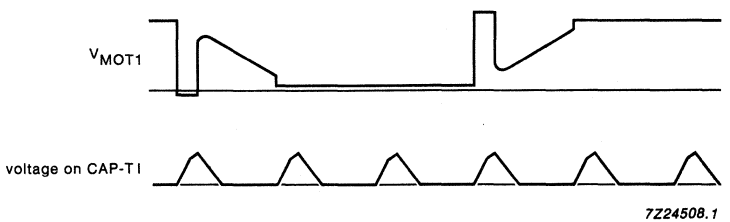


Fig.7 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Note

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The External Damping Components

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5140A. This distortion may influence the correct functioning of the TDA5140A, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 μs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 μs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp-8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 μF (use 1 μF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 μs. Eddy currents will also contribute to this phase shift. A shift of 20 μs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or, 0.1 mm on a VHS scanner drum.

Other Design Aspects

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG Signal

The FG signal is generated in the TDA5140A by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG Signal

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PGIN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 15 μs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.8).

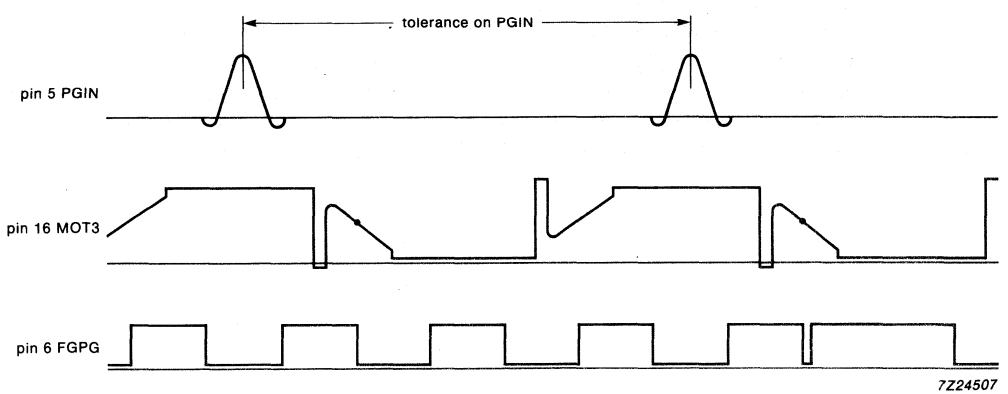


Fig.8 Timing of the FG and PGIN signals.

APPLICATION INFORMATION (continued)

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PGIN on pin 5) must sense a positive going edge (> 80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.8).

The voltage requirements of the PGIN input are such that a cheap pick-up coil can be used as a sensor (see Fig.9).

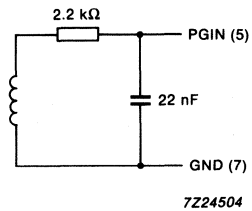


Fig.9 Pick-up coil as PG sensor.

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PGIN input must be grounded, this will result in a 50% duty factor FG signal.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P - 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.5).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.10).

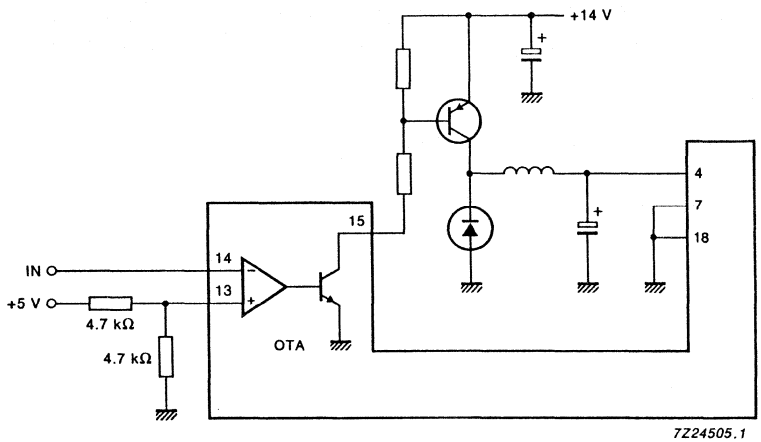


Fig.10 PWM drive of the output stages, OTA used as a level converter.

A further aspect of motor control is current or voltage control; the TDA5140A is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pin 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.5 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5140A with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 4 then the motor will generate a braking torque that is proportional to the current.

APPLICATION INFORMATION (continued)

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+ 15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 4) may cause higher currents than allowed (> 1 A). These currents must be limited externally.

BRUSHLESS DC MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The TDA5141 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

Features

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuit
- Three push-pull outputs:
  - 1.8 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range	note 1	V_P	4	–	18	V
Supply current range	note 2	I_P	–	4.9	6.5	mA
Input voltage to the output driver stages	see Fig.1	V_{VMOT}	3	–	16	V
Driver output voltage range	I_O = 0 mA	V_O	0.2	–	V_{VMOT}–0.9	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

PACKAGE OUTLINES

TDA5141: 18-lead DIL; plastic with internal heatspreader (SOT102).
TDA5141AT: 20-lead mini-pack; plastic (SO20; SOT163A).
TDA5141T: 28-lead mini-pack; plastic (SO28; SOT136A).

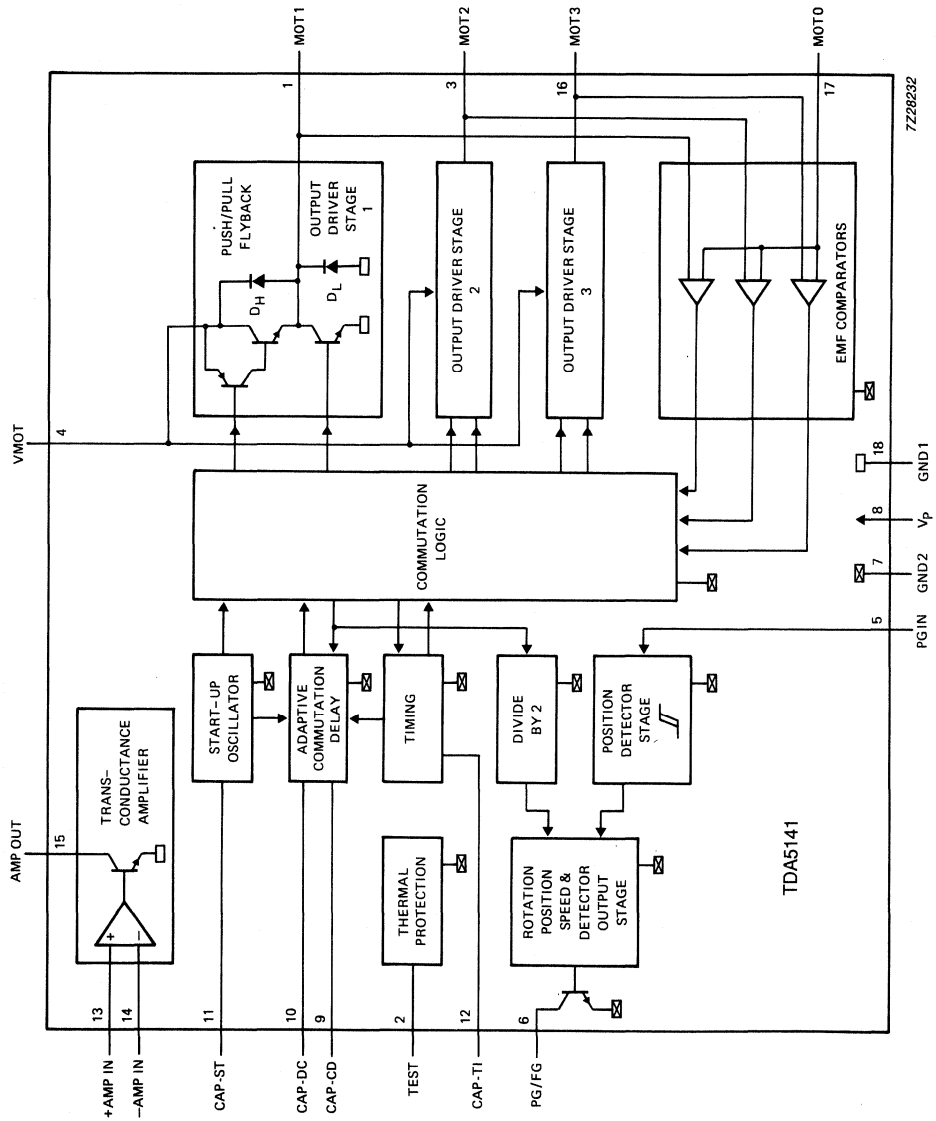


Fig.1 Block diagram; SOT102 (DIL 18).

PINNING

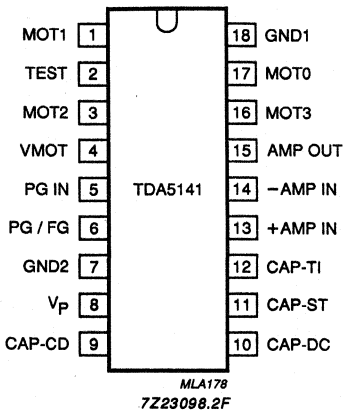


Fig.2(a) Pinning diagram; SOT102 (DIL 18).

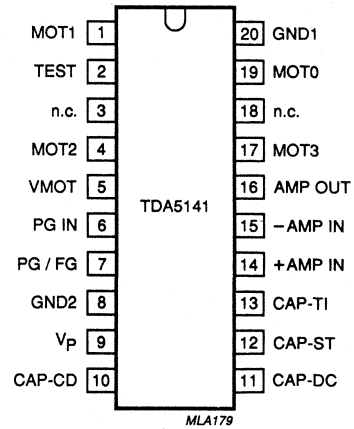


Fig.2(b) Pinning diagram; SOT163A (SO20).

DEVELOPMENT DATA

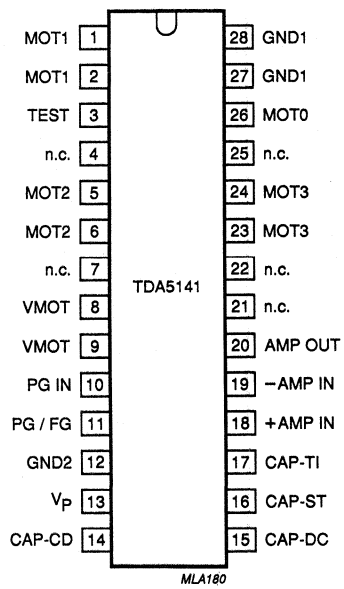


Fig.2(c) Pinning diagram; SOT136A (SO28).

PINNING (continued)

DIL18	SO20	SO28	signal	function
1	1	1,2	MOT1	driver output 1
2	2	3	TEST	test input/output
	3	4	n.c.	not connected
3	4	5, 6	MOT2	driver output 2
		7	n.c.	not connected
4	5	8, 9	VMOT	input voltage for the output driver stages
5	6	10	PG IN	position generator: input from the position detector sensor to the position detector stage (optional). Only if an external position coil is used.
6	7	11	PG/FG	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
7	8	12	GND2	ground supply return for control circuits
8	9	13	V_P	positive supply voltage
9	10	14	CAP-CD	external capacitor connection for adaptive commutation delay timing
10	11	15	CAP-DC	external capacitor connection for adaptive commutation delay timing copy
11	12	16	CAP-ST	external capacitor connection for start-up oscillator
12	13	17	CAP-TI	external capacitor connection for timing
13	14	18	+AMP IN	non-inverting input of the transconductance amplifier
14	15	19	−AMP IN	inverting input of the transconductance amplifier
15	16	20	AMP OUT	transconductance amplifier output (open collector)
		21,22	n.c.	not connected
16	17	23,24	MOT3	driver output 3
17	19	26	MOT0	input from the start point of the motor coils
	18	25	n.c.	not connected
18	20	27,28	GND1	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5141 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5141 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5141 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal
- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Additional uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Input voltage; all pins except VMOT	$V_I < 18$ V	V_I	−0.3	$V_P + 0.5$	V
VMOT input voltage		V_{VMOT}	−0.5	17	V
Output voltage; AMP OUT and PG/FG		V_O	GND	V_P	V
Output voltage; MOT0, MOT1, MOT2 and MOT3		V_O	−1	$V_{VMOT} + V_D$	V
Input voltage; CAP-ST, CAP-TI, CAP-CD and CAP-DC		V_I	–	2.5	V
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	0	70	°C
Total power dissipation		P_{tot}		see Fig. 3	
Electrostatic voltage; handling*		V_{es}	–	500	V

THERMAL RESISTANCE

Junction average to ambient, on a vertically mounted printed-circuit board (DIL18)	$R_{th\ j\text{-}a}$	=	50	K/W
Junction (peak) to ambient, on a printed-circuit board (DIL18)	$R_{th\ j\text{-}p}$	=	75	K/W
Junction average to ambient (SO20; copper lead frame)	$R_{th\ j\text{-}a}$	=	90	K/W
Junction average to ambient (SO28; copper lead frame)	$R_{th\ j\text{-}a}$	=	70	K/W

* Equivalent to discharging a 100 pF capacitor through a 0 Ω resistor.

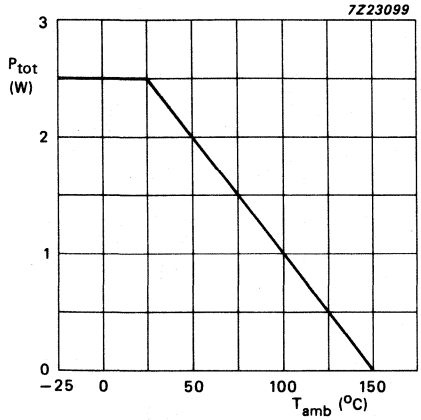


Fig.3(a) Power derating curve; SOT102 (DIL 18).

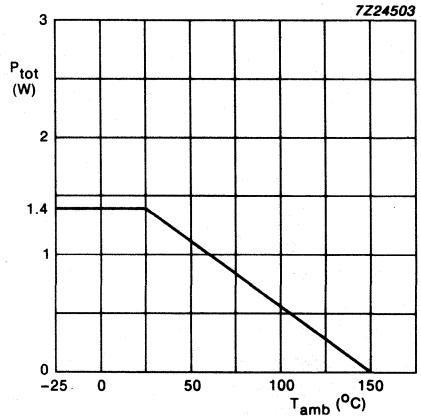


Fig.3(b) Power derating curve; SO20.

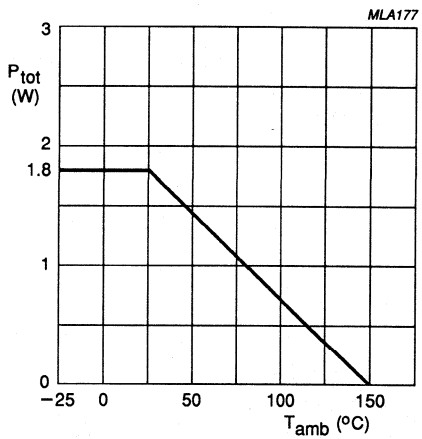


Fig.3(c) Power derating curve; SO28.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	4	–	18	V
Input current range	note 2	I_P	–	4.9	6.5	mA
Input voltage to the driver output stages	see Fig.1	V_{VMOT}	0	–	16	V
Thermal protection						
Local temperature at temperature sensor causing shut-down		T_{SD}	130	140	150	°C
Reduction in temperature before switch-on	after shut-down	ΔT	–	$T_{SD}-30$	–	°C
MOT0						
Input voltage range		V_I	−0.5	–	V_{VMOT}	V
Input bias current	0.5 V < V_I < VMOT−1.5 V	I_I	−10	–	0	μA
Comparator switching level	note 3	$\pm V_{CSW}$	–	25	–	mV
Variations in comparator switching levels		ΔV_{CS}	−3	0	+3	mV
Comparator input hysteresis		V_H	–	75	–	μV
MOT1, MOT2 and MOT3	driver active					
Driver output voltage range	I_O = 100 mA	V_O	0.4	–	$V_{VMOT}-1.2$	V
	I_O = 1200 mA or 1000 mA at T_{amb} = +70 °C	V_O	0.8	–	$V_{VMOT}-1.8$	V
Variation in saturation voltage lower transistors	I_O = 100 mA	ΔV_{OL}	–	–	180	mV
Variation in saturation voltage upper transistors	I_O = −100 mA	ΔV_{OH}	–	–	180	mV
Current limiting	lower transistor V_{CE} = 6 V	I_{LIM}	*	1.8	*	A
Diode forward voltage (D_H)	notes 4 and 5; see Fig.1; I_O = −500 mA	V_{DHF}	–	–	1.5	V
Diode forward voltage (D_L)	notes 4 and 5; see Fig.1; I_O = 500 mA	V_{DLF}	−1.5	–	–	V
Peak diode current	note 5	I_{DM}	–	–	1	A

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
VMOT						
Input voltage range		V_{MOT}	3	–	16	V
+AMP IN and –AMP IN						
Input voltage range		V_{IAMP}	–0.3	–	V_P–1.7	V
Differential mode voltage without 'latch-up'		$\pm V_{IAMP}$	–	–	V_P	V
Input bias current		I_{LI}	–	–	500	nA
Input capacitance		C_I	–	4	–	pF
Input offset voltage		V_{OFFSET}	–	–	3	mV
AMP OUT						
Output sink current		I_I	40	–	–	mA
Saturation voltage	I_I = 40 mA	V_{SAT}	–	1.5	*	V
Maximum output voltage		V_{Omax}	18	–	–	V
Slew rate	R_L = 330 Ω; C_L = 50 pF	SR	–	60	–	mA/μs
Transfer gain		G_{TRAN}	0.3	–	–	S
PG IN						
Input voltage		V_I	–0.3	–	V_P–1.7	V
Input bias current		I_b	–	–	500	nA
Input resistance		R_I	5	–	25	kΩ
Comparator switching level		V_{CSW}	57	82	107	mV
Comparator input hysteresis		$\pm V_H$	–	8	–	mV
PG/FG						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Maximum output voltage HIGH		V_{OHmax}	V_P	–	–	V
Transition time	HIGH-to-LOW; C_L = 50 pF; R_L = 10 kΩ	t_{THL}	–	0.5	–	μs
Ratio of PG/FG frequency and commutation frequency			–	1 : 2	–	
Duty factor		δ	–	50	–	%
Pulse width LOW	after a PG IN pulse	t_{PL}	5	7	9	μs

* Value to be fixed.

CHARACTERISTICS (continued)

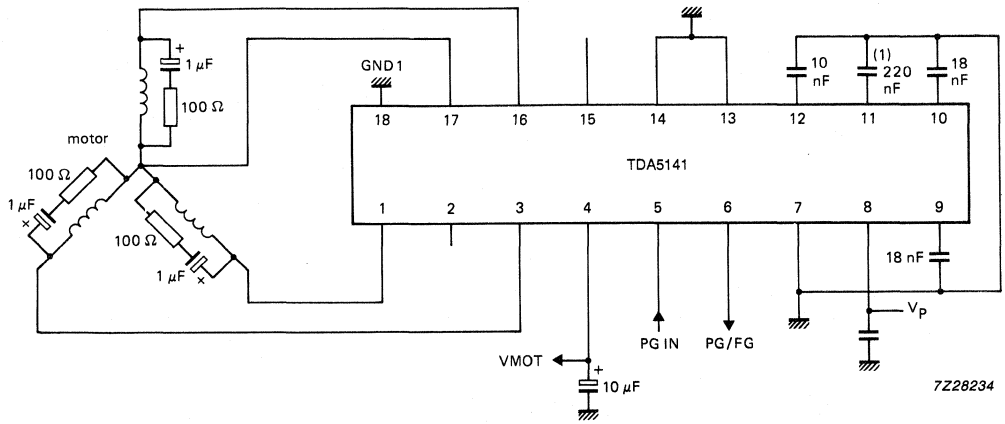
parameter	condition	symbol	min.	typ.	max.	unit
CAP-ST						
Output sink current		I_I	1.5	2.0	2.5	μA
Output source current		I_O	−2.5	−2.0	−1.5	μA
Lower switching level		V_{SWL}	–	0.20	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-TI						
Output sink current		I_I	–	28	–	μA
Output source current HIGH		I_{OH}	–	−57	–	μA
Output source current LOW		I_{OL}	–	−5	–	μA
Lower switching level		V_{SWL}	–	50	–	mV
Middle switching level		V_{SWM}	–	0.30	–	V
Upper switching level		V_{SWH}	–	2.20	–	V
CAP-CD						
Output sink current		I_I	*	16.2	*	μA
Output source current		I_O	*	−8.1	*	μA
Ratio of sink to source current		–	1.9	2.0	2.1	
Input voltage level LOW		V_{IL}	850	–	900	mV
Input voltage level HIGH		V_{IH}	2.3	–	2.5	V
CAP-DC						
Output sink current		I_I	*	15.5	*	μA
Output source current		I_O	*	−15.5	*	μA
Ratio of sink to source current		I_I/I_O	0.95	1	1.05	

Notes to the characteristics

1. An unstabilized supply can be used.
2. VMOT = V_P, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in high impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

* Value to be fixed.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA).

DEVELOPMENT DATA

Introduction

Refer to Fig.5. Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

APPLICATION INFORMATION (continued)

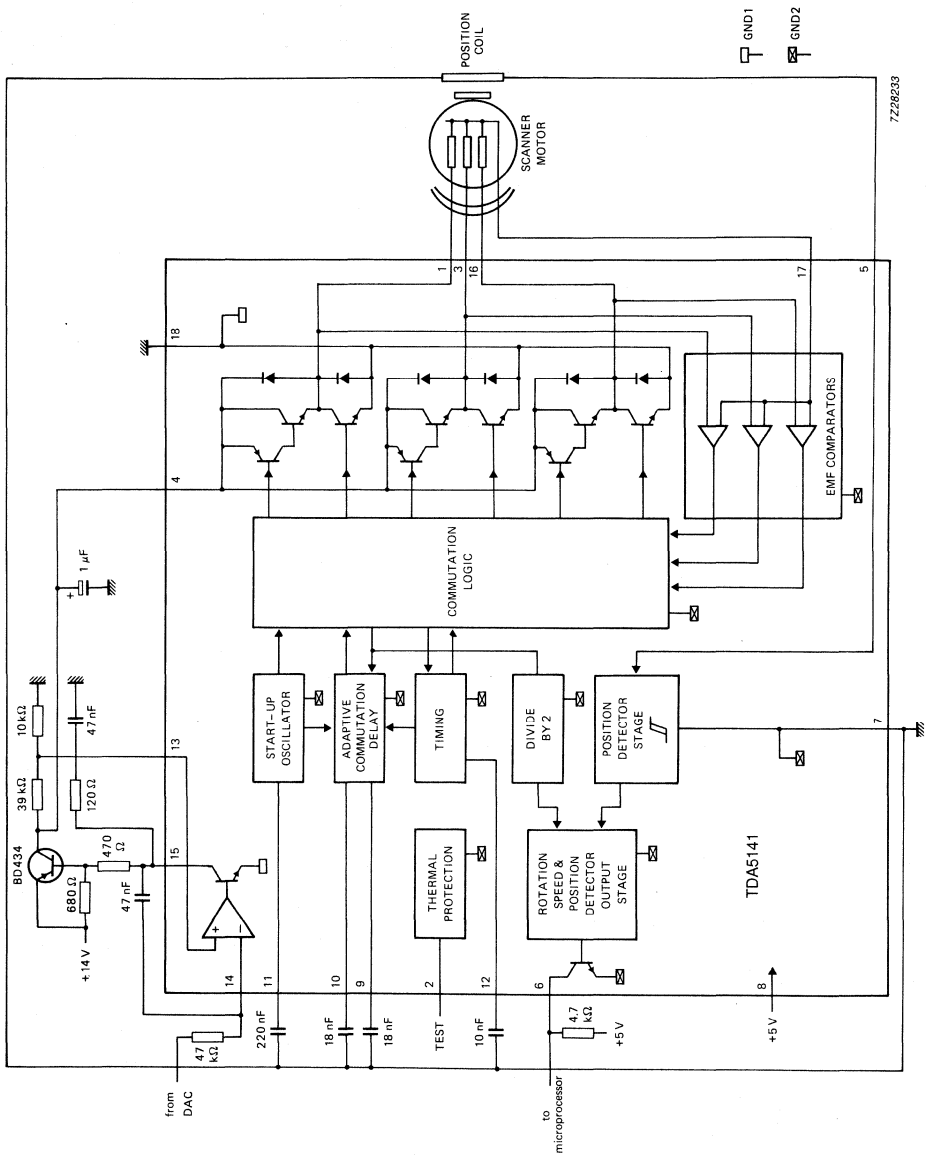


Fig.5 Typical application of the TDA5141 as a scanner driver, with use of OTA.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5141 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5141 designed for systems with low current consumption uses I^2L logic and adaptive base drive for the output transistors (patent pending), possibility of using a pick-up coil without bias current.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit. These are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

The Start Capacitor (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$$t_{start} = (2.15 \times C)s \text{ (with C in } \mu F)$$

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5141 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where: K_t = torque constant (N·m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N. m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The Adaptive Commutation Delay (CAP-CD and CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{c1}:

$C = 6231/f_{c1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.080 x C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 6 illustrates typical voltage waveforms.

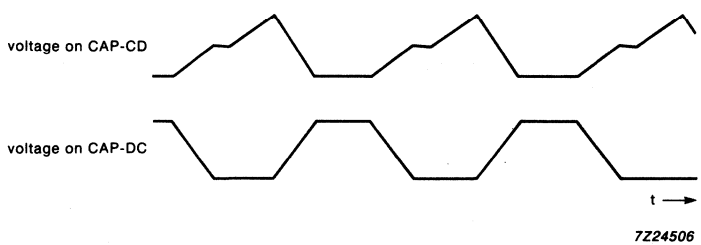


Fig.6 CAP-CD and CAP-DC voltage waveforms in normal running mode.

The Timing Capacitor (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time. The EMF usually recovers within a short time if the motor is running normally ($<<$ ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer ($>>$ ms). A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 50 mV to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$$C = 5 \times 10^{-6} \times t_m / 1.9 = 2.63\ t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.7.

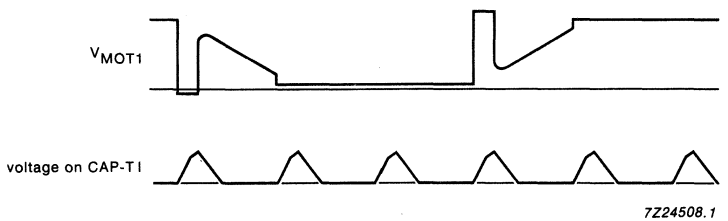


Fig.7 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Note

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The External Damping Components

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5141. This distortion may influence the correct functioning of the TDA5141, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 μs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 μs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp-8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 μF (use 1 μF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 μs. Eddy currents will also contribute to this phase shift. A shift of 20 μs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or, 0.1 mm on a VHS scanner drum.

Other Design Aspects

There are other design aspects concerning the application of the TDA5141 besides the communication function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG Signal

The FG signal is generated in the TDA5141 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG Signal

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PGIN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 15 μs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.8).

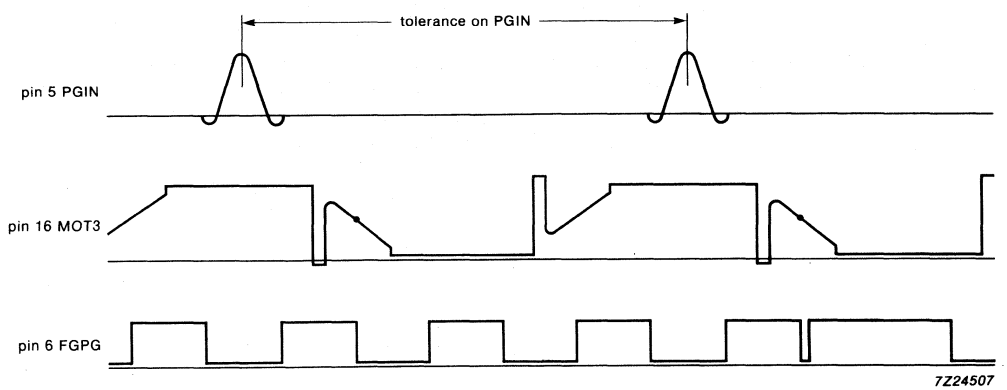


Fig.8 Timing of the FG and PGIN signals.

APPLICATION INFORMATION (continued)

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PGIN on pin 5) must sense a positive going edge (> 80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.8).

The voltage requirements of the PGIN input are such that a cheap pick-up coil can be used as a sensor (see Fig.9).

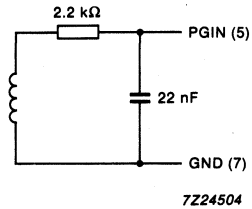


Fig.9 Pick-up coil as PG sensor.

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PGIN input must be grounded, this will result in a 50% duty factor FG signal.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P - 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analogue control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analogue or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analogue control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.5).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.10).

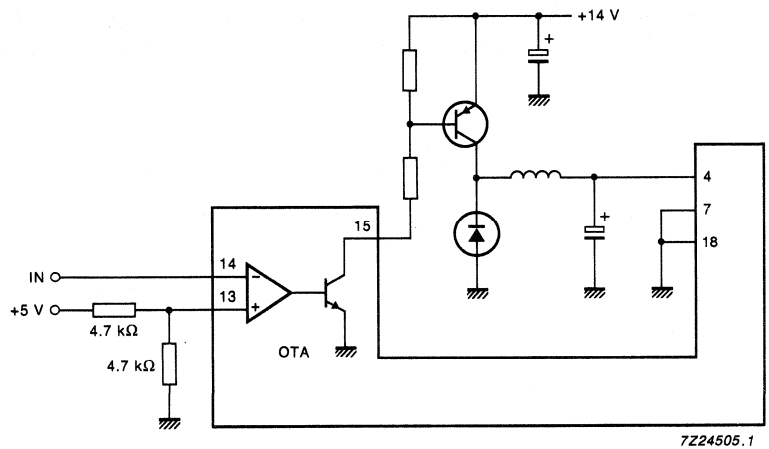


Fig.10 PWM drive of the output stages, OTA used as a level converter.

A further aspect of motor control is current or voltage control; the TDA5141 is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pin 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.5 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5141 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 4 then the motor will generate a braking torque that is proportional to the current.

APPLICATION INFORMATION (continued)

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+ 15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 4) may cause higher currents than allowed (> 1 A). These currents must be limited externally.

BRUSHLESS DC MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The TDA5142T is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for power-drum motors (hard-disk drives, tape drives, fan motors).

Features

- Full-wave commutation without position sensors
- Built-in start-up circuit
- Six outputs that can drive three external transistor pairs
  - 0.15 A output current
  - low saturation voltage
  - built-in current limiters
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range	note 1	V_P	4	–	18	V
Supply current range	note 2	I_P	–	*	*	mA
Input voltage to the output driver stages	see Fig.1	V_{VMOT}	3	–	18	V
Driver output voltage range	I_O = 0 mA	V_O	0.2	–	–	V
OUT– NA, NB, NC			–	–	V_{VMOT}–0.9	V
OUT– PA, PB, PC			–	–	V_{VMOT}–0.2	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.

* Value to be fixed.

PACKAGE OUTLINE

24-lead mini-pack; plastic (SO24; SOT137A).

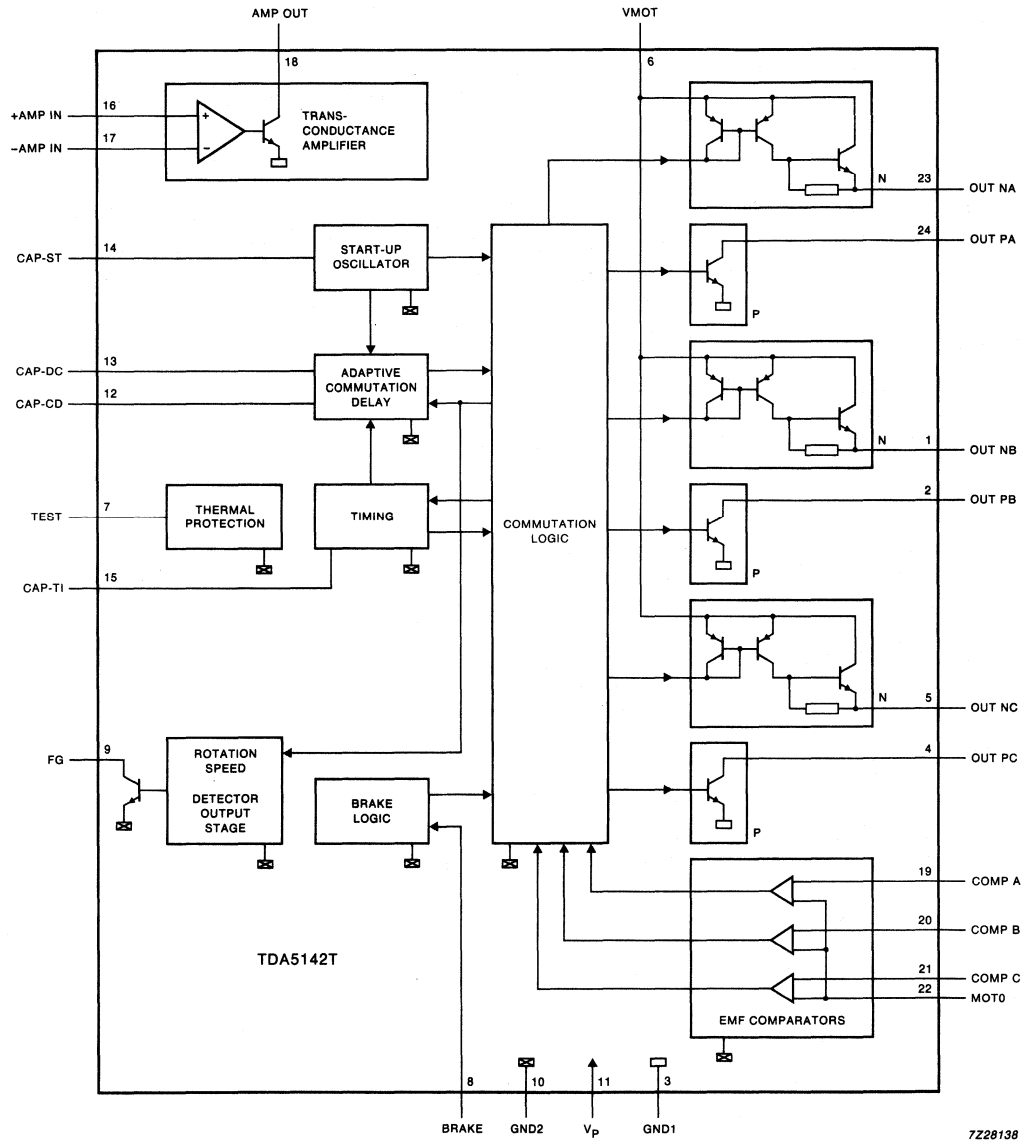


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

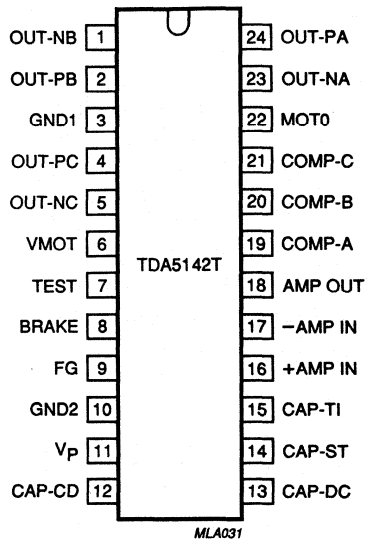


Fig.2 Pinning diagram.

pin number	signal	function
1	OUT-NB	driver output for driving the n-channel power FET or power NPN
2	OUT-PB	driver output for driving the p-channel power FET or power PNP
3	GND1	ground (0 V) motor supply return for output stages
4	OUT-PC	driver output for driving the p-channel power FET or power PNP
5	OUT-NC	driver output for driving the n-channel power FET or power NPN
6	VMOT	input voltage for the output driver stages
7	TEST	test input/output
8	BRAKE	brake input command
9	FG	output of the rotation speed position detector stage
10	GND2	ground supply return for control circuits
11	V_P	positive supply voltage
12	CAP-CD	external capacitor connection for adaptive commutation delay timing
13	CAP-DC	external capacitor connection for adaptive commutation delay timing copy
14	CAP-ST	external capacitor connection for start-up oscillator
15	CAP-TI	external capacitor connection for timing

PINNING (continued)

pin number	signal	function
16	+AMP IN	non-inverting input of the transconductance amplifier
17	–AMP IN	inverting input of the transconductance amplifier
18	AMP OUT	transconductance amplifier output (open collector)
19	COMP-A	input of comparator corresponding to output A
20	COMP-B	input of comparator corresponding to output B
21	COMP-C	input of comparator corresponding to output C
22	MOT0	input from the star point of the motor coils
23	OUT-NA	driver output for driving the n-channel power FET or power NPN
24	OUT-PA	driver output for driving the p-channel power FET or power PNP

FUNCTIONAL DESCRIPTION

The TDA5142T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5142T offers protected outputs capable of driving external power FETs or power bipolar transistors. It can easily be adapted for different motors and applications. The TDA5142T offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Six output drivers
- Maximum output current (0.15 A)
- Outputs protected by current limiting and thermal protection
- Low current consumption
- Accurate frequency generator (FG) by using the motor EMF
- Brake function
- Additional uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Input voltage					
all pins except VMOT	$V_I < 18$ V	V_I	−0.3	$V_P + 0.5$	V
VMOT input voltage		V_{VMOT}	–	18	V
Output voltage					
FG		V_O	GND	V_P	V
AMP OUT		V_O	–	18	V
Output voltage					
OUT– NA, NB, NC		V_O	0.2	$V_{VMOT}-0.9$	V
OUT– PA, PB, PC		V_O	0.2	$V_{VMOT}-0.2$	V
Input voltage					
CAP-ST, CAP-TI, CAP-CD and CAP-DC		V_I	–	2.5	V
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	0	70	°C
Total power dissipation		P_{tot}		see Fig.3	
Electrostatic voltage; handling*		V_{es}	–	500	V

THERMAL RESISTANCE

Junction average to ambient (SO24; copper lead frame) $R_{th\,j\text{-}a}$ = 75 K/W

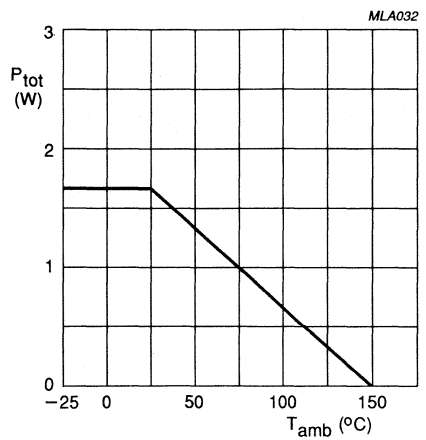


Fig.3 Power derating curve.

* Equivalent to discharging a 100 pF capacitor through a 0 Ω resistor.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	4	–	18	V
Input current range	note 2	I_P	–	*	*	mA
Input voltage to the driver output stages	see Fig.1	V_{VMOT}	0	–	18	V
Thermal protection						
Local temperature at temperature sensor causing shut-down		T_{SD}	130	140	150	°C
Reduction in temperature before switch-on	after shut-down	ΔT	–	$T_{SD}-30$	–	°C
MOT0						
Input voltage range		V_I	−0.5	–	V_{VMOT}	V
Input bias current	$0.5\ V < V_I < VMOT-1.5\ V$	I_I	−10	–	0	μA
Comparator switching level	note 3	$\pm V_{CSW}$	–	25	–	mV
Variations in comparator switching levels		ΔV_{CS}	−3	0	+ 3	mV
Comparator input hysteresis		V_H	–	75	–	μV
OUT– A, B and C	driver active					
Driver output voltage range	I_O = 100 mA	V_O	*	–	*	V
Variation in saturation voltage lower transistors	I_O = 100 mA	ΔV_{OL}	–	–	180	mV
Variation in saturation voltage upper transistors	I_O = −100 mA	ΔV_{OH}	–	–	180	mV
Current limiting	lower transistor	I_{LIM}	–	150	–	mA

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
VMOT						
Input voltage range		V_{MOT}	3	–	18	V
+AMP IN and –AMP IN						
Input voltage range		V_{IAMP}	–0.3	–	V_P–1.7	V
Differential mode voltage without 'latch-up'		$\pm V_{IAMP}$	–	–	V_P	V
Input bias current		I_{LI}	–	–	500	nA
Input capacitance		C_I	–	4	–	pF
Input offset voltage		V_{OFFSET}	–	–	3	mV
AMP OUT						
Output sink current		I_I	40	–	–	mA
Saturation voltage	I_I = 40 mA	V_{SAT}	–	–	*	V
Maximum output voltage		V_{Omax}	18	1.5	–	V
Slew rate	R_L = 330 Ω; C_L = 50 pF	SR	40	–	–	mA/μs
Transfer gain		G_{TRAN}	0.3	–	–	S
BRAKE						
Brake-mode voltage on pin 8	$4 < V_P < 18$ V	BMV	–	–	2.3	V
Brake current on pin 8		BC	–	–20	–	μA
Normal-mode current on pin 8		NMC	–	0	–	μA
FG						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Maximum output voltage HIGH		V_{OHmax}	V_P	–	–	V
Transition time	HIGH-to-LOW; C_L = 50 pF; R_L = 10 kΩ	t_{THL}	–	0.5	–	μs
Ratio of FG frequency and commutation frequency			–	1	–	
Duty factor		δ	–	50	–	%

* Value to be fixed.

CHARACTERISTICS (continued)

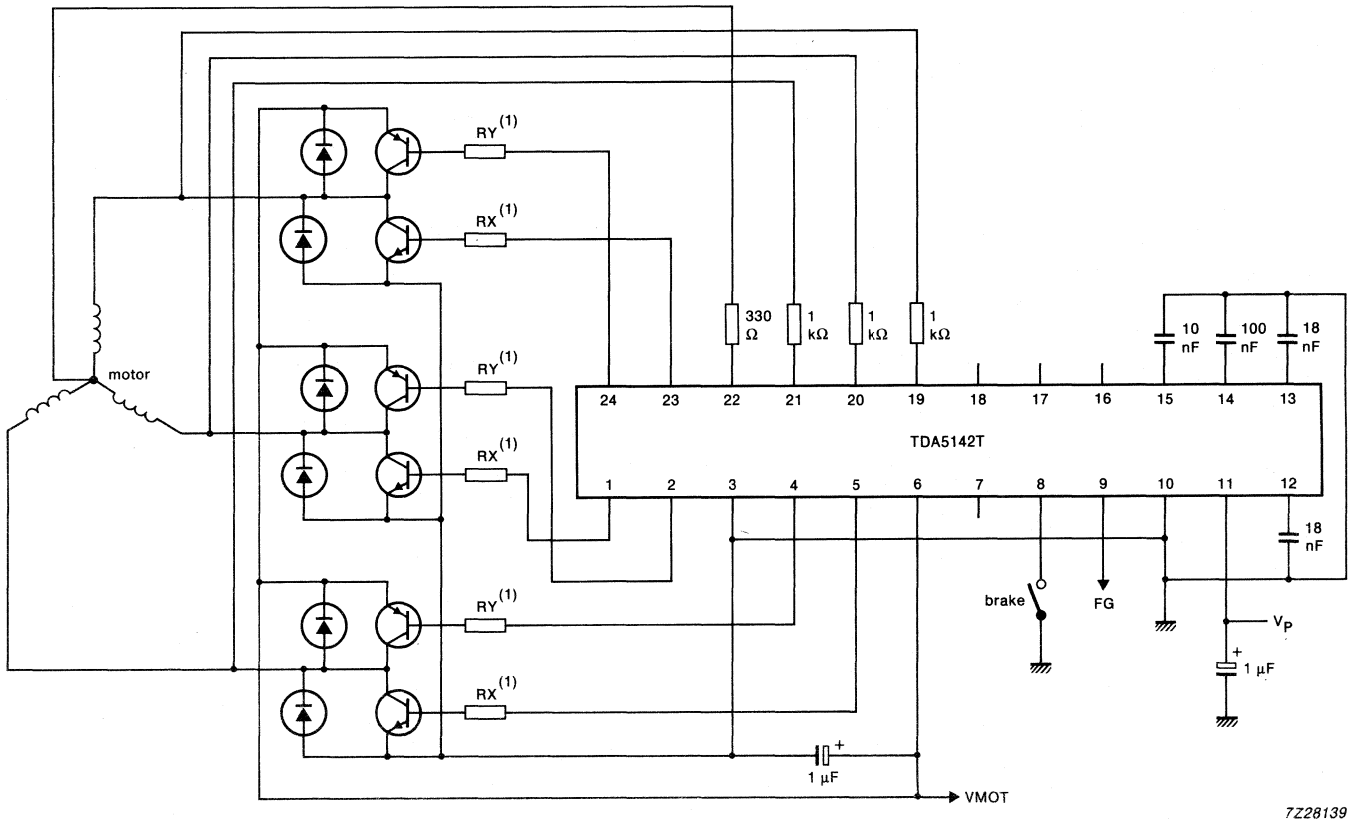
parameter	condition	symbol	min.	typ.	max.	unit
CAP-ST						
Output sink current		I_I	1.5	2.0	2.5	μA
Output source current		I_O	−2.5	−2.0	−1.5	μA
Lower switching level		V_{SWL}	−	0.20	−	V
Upper switching level		V_{SWH}	−	2.20	−	V
CAP-TI						
Output sink current		I_I	−	28	−	μA
Output source current HIGH		I_{OH}	−	−57	−	μA
Output source current LOW		I_{OL}	−	−5	−	μA
Lower switching level		V_{SWL}	−	0.20	−	V
Middle switching level		V_{SWM}	−	0.30	−	V
Upper switching level		V_{SWH}	−	2.20	−	V
CAP-CD						
Output sink current		I_I	*	16.2	*	μA
Output source current		I_O	*	−8.1	*	μA
Ratio of sink to source current		I_I/I_O	1.9	−	2.1	
Input voltage level LOW		V_{IL}	0.85	−	0.9	V
Input voltage level HIGH		V_{IH}	2.37	−	2.45	V
CAP-DC						
Output sink current		I_I	*	16	*	μA
Output source current		I_O	*	−16	*	μA
Ratio of sink to source current		I_I/I_O	0.95	1	1.05	

Notes to the characteristics

1. An unstabilized supply can be used.
2. VMOT = V_P, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to driver outputs OUT− NA, NB, NC and OUT− PA, PB, PC.

* Value to be fixed.

APPLICATION INFORMATION



(1) RX = RY > 8 (VMOT−1.5).

Fig.4(a) Application diagram without use of the operational transconductance amplifier (OTA) with bipolar power transistors.

APPLICATION INFORMATION (continued)

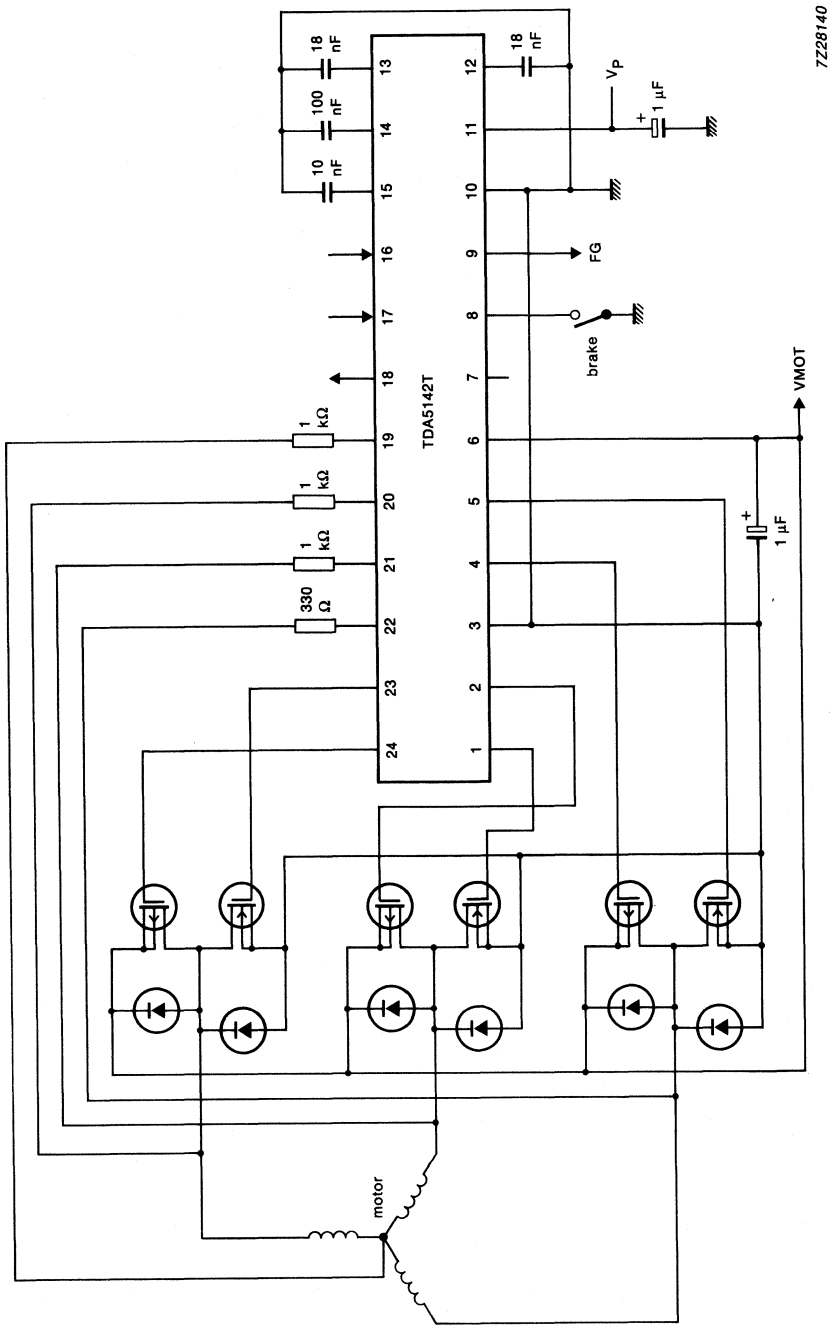


Fig.4(b) Application diagram without use of the operational transconductance amplifier (OTA) with MOS power transistors.

Introduction

Refer to Fig.5. Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

The driver output stages are also protected by a current limiting circuit and by thermal protection.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

APPLICATION INFORMATION (continued)

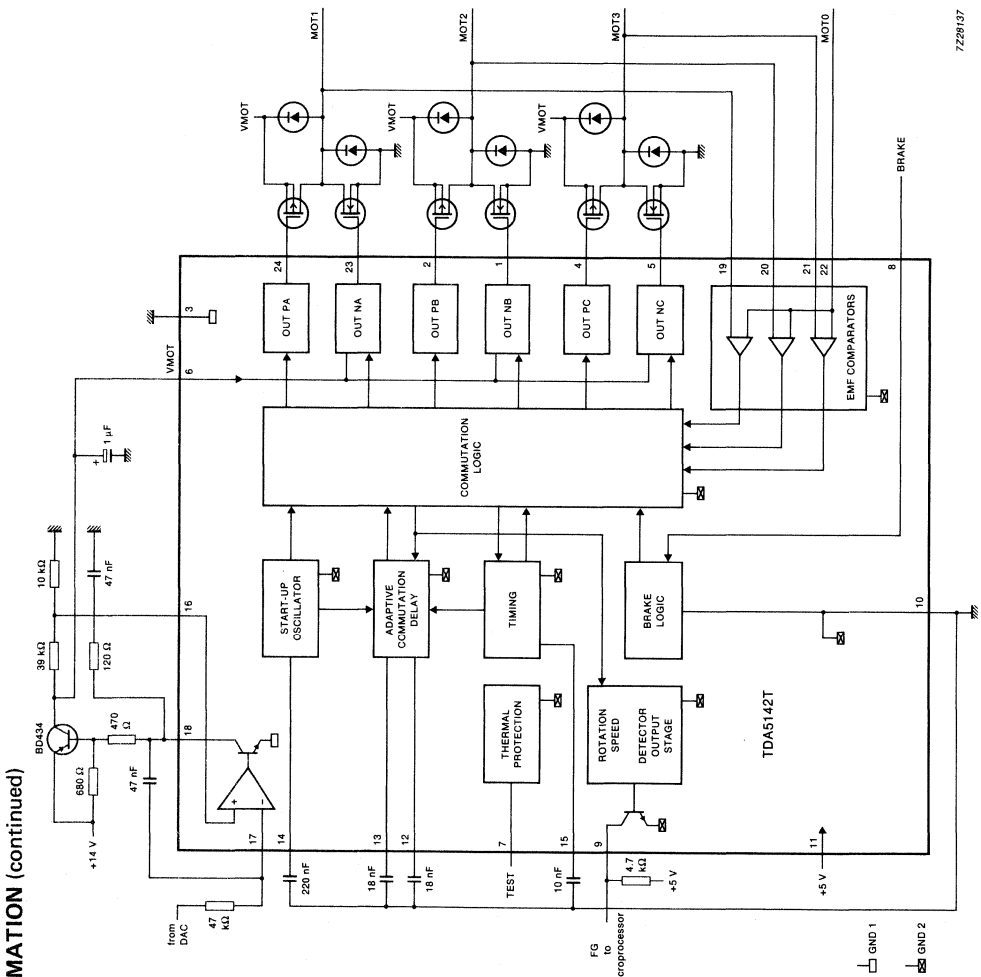


Fig. 5 Typical application of the TDA5142T as a scanner driver, with use of OTA.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5142T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5142T designed for systems with low current consumption uses I^2L logic and adaptive base drive for the output transistors (patent pending).

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit. These are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

The Start Capacitor (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C)s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5142T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where: K_t = torque constant (N·m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6} kg.m^2$, $K = 25 \times 10^{-3}$ N. m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The Adaptive Commutation Delay (CAP-CD and CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 10 μA and the discharging current 20 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{c1}:

$C = 7692/f_{c1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 20 μA.

maximum delay = (0.065 x C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 7692/400 = 19.2 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 6 illustrates typical voltage waveforms.

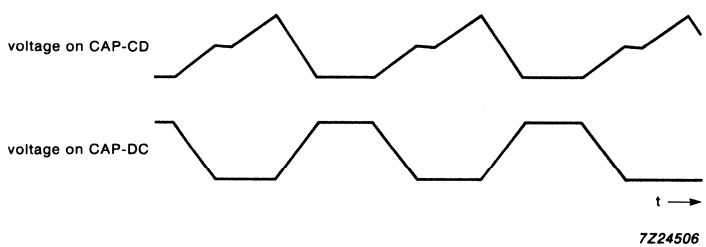


Fig.6 CAP-CD and CAP-DC voltage waveforms in normal running mode.

The Timing Capacitor (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time. The EMF usually recovers within a short time if the motor is running normally ($<<$ ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer ($>>$ ms). A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 50 mV to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-T1 is given by:

$$C = 5 \times 10^{-6} \times t_m / 1.9 = 2.63\ t_m \quad (C \text{ in nF; } t \text{ in ms})$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.7.

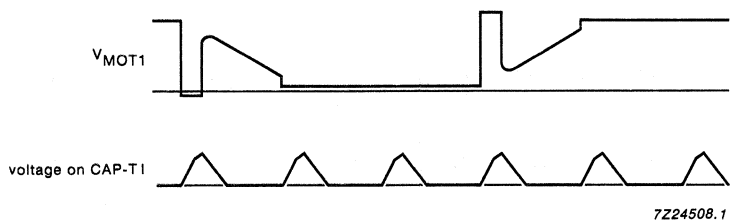


Fig.7 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Note

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

APPLICATION INFORMATION (continued)

Adjustments (continued)

The External Damping Components

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5140A. This distortion may influence the correct functioning of the TDA5140A, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 μs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 μs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp-8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 μF (use 1 μF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 μs. Eddy currents will also contribute to this phase shift. A shift of 20 μs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or, 0.1 mm on a VHS scanner drum.

Other Design Aspects

There are other design aspects concerning the application of the TDA5142T besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG Signal

The FG signal is generated in the TDA5142T by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero crossings and LOW-to-HIGH on all commutations.

Output FG can source typically 75 μA and sink more than 3 mA.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 900 Hz.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P - 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analogue control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 18) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 16) is positive with respect to the inverting input (pin 17). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analogue or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analogue control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.5).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.8).

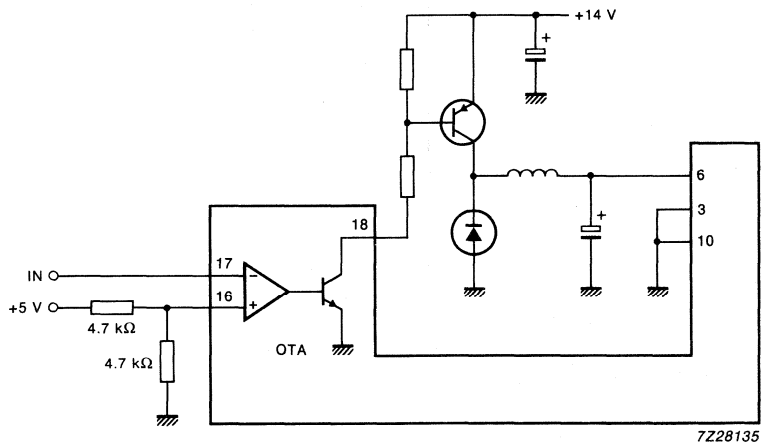


Fig.8 PWM drive of the output stages, OTA used as a level converter.

A further aspect of motor control is current or voltage control; the TDA5142T is intended for voltage control applications. Both ground pins (3 and 10) must be connected externally. However the current from pin 10 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 3, 10 and ground can be used for current control. Care must be taken that the voltage on pin 3, 10 does not disturb the (digital) FG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.5 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5142T with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FG signal is read by a microprocessor that runs the servo control program.

APPLICATION INFORMATION (continued)

Other Design Aspects (continued)

A final aspect of motor control is braking; decreasing the speed to zero. Provisions have been made for this function:

- If the voltage on pin 8 is less than 2.3 V the motor brakes
- If pin 8 is floating or if the voltage on pin 8 is greater than 2.7 V the motor runs normally

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+ 15%). This means that the current to and from the output stages is limited.
- Thermal protection is achieved:
  The transistors are switched off when the local temperature becomes too high.

VHF, UHF AND HYPERBAND MIXER/OSCILLATOR FOR TV AND VCR 3-BAND TUNERS

GENERAL DESCRIPTION

The TDA5330T is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small 3-band tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B and C
- Balanced oscillator for band B and C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with an output impedance of 100 Ω
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19-2, 26}$	–	12	–	V
Band A frequency range		f_A	48	–	180	MHz
Band B frequency range		f_B	160	–	470	MHz
Band C frequency range		f_C	430	–	860	MHz
Conversion noise		F	7	–	11	dB
Band A input voltage	1% cross-modulation	V_{24-26}	–	100	–	dBμV
Band B and C input power	1% cross-modulation	P_I	–	–21	–	dBm
Band A voltage gain		G_v	–	24	–	dB
Band B voltage gain		G_v	–	37	–	dB
Band C voltage gain		G_v	–	36	–	dB

PACKAGE OUTLINE

28-lead mini-pack, plastic (SO20; SOT163A).

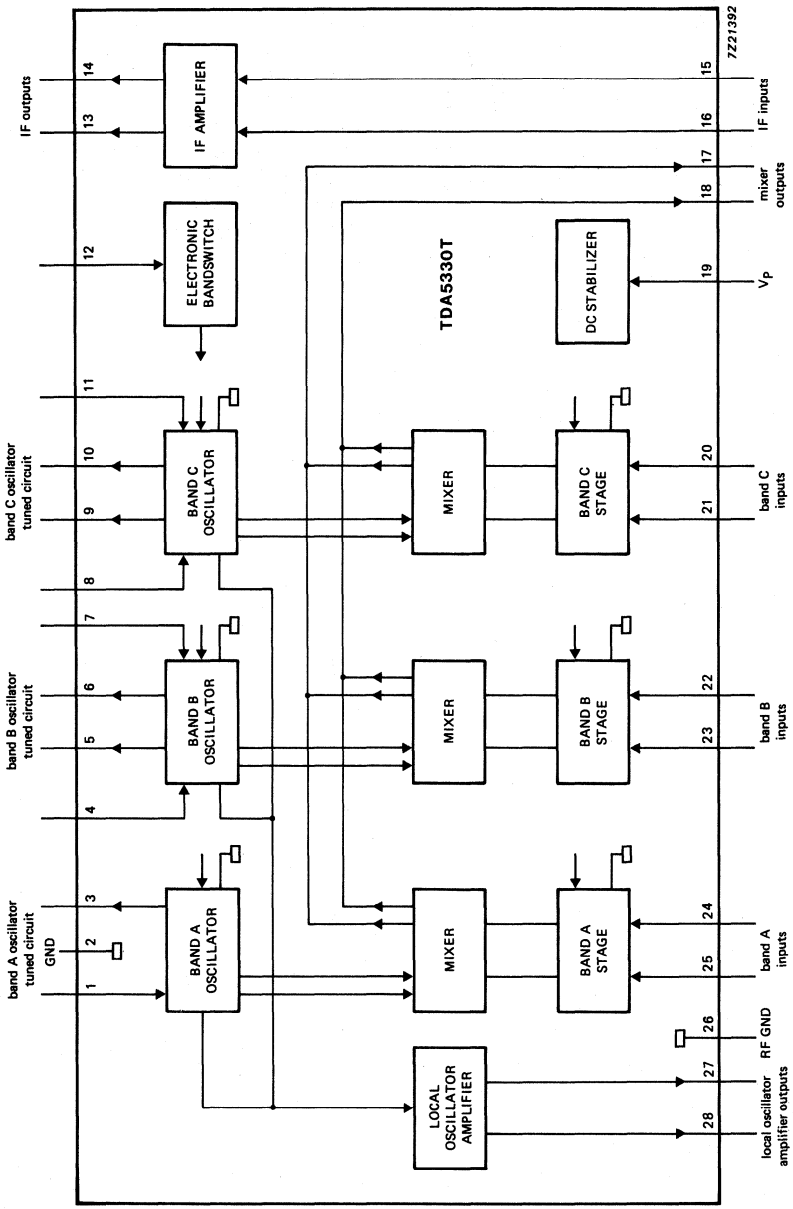


Fig. 1 Block diagram.

DEVELOPMENT DATA

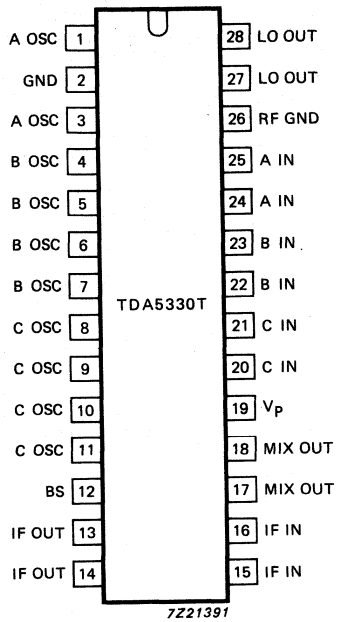


Fig. 2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	C OSC	band C oscillator input
9	C OSC	band C oscillator output
10	C OSC	band C oscillator output
11	C OSC	band C oscillator input
12	BS	electronic bandswitch
13	IF OUT	IF amplifier output
14	IF OUT	IF amplifier output
15	IF IN	IF amplifier input
16	IF IN	IF amplifier input
17	MIX OUT	mixer output
18	MIX OUT	mixer output
19	V_P	positive supply voltage
20	C IN	band C input
21	C IN	band C input
22	B IN	band B input
23	B IN	band B input
24	A IN	band A input
25	A IN	band A input
26	RF GND	ground for RF inputs
27	LO OUT	local oscillator amplifier output
28	LO OUT	local oscillator amplifier output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_{19-2, 26}$	−0.3	14	V
Switching voltage		V_{12}	0	14	V
Output current of each pin to ground		I_O	−	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	−	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	typ. 75 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	10	–	13.2	V
Supply current		I_{19}	–	42	55	mA
Switching voltage;						
band A		V_{12}	0	–	1.1	V
band B		V_{12}	1.6	–	2.4	V
band C		V_{12}	3.0	–	5.0	V
Switching current;						
band C		I_{12}	–	–	50	μA
Band A Mixer (including IF amplifier)	measured using circuit shown in Fig. 9					
Frequency range		f_A	48	–	180	MHz
Noise figure	note 1;					
	50 MHz	NF	–	7.5	9	dB
	180 MHz	NF	–	9	10	dB
Optimum source conductance	50 MHz	$G_{24\text{-}26}$	–	0.5	–	mS
	180 MHz	$G_{24\text{-}26}$	–	1.1	–	mS
Input admittance	see Fig. 9					
Input capacitance	50 - 180 MHz	$C_{24\text{-}26}$	–	2	–	pF
Input voltage	1% cross-modulation; in channel	$V_{24\text{-}26}$	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel	$V_{24\text{-}26}$	100	108	–	dBμV
Voltage gain	20 log ($V_{13\text{-}14}/V_{24}$)	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$Sc = I_{17}/V_{24}$ $= -I_{18}/V_{24}$	$Sc_{24\text{-}17,\ 18}$	–	3.5	–	mS
Mixer output admittance	pins 15 and 16		–	0.1	–	mS
Mixer output capacitance		$C_{17\text{-}18}$	–	2	–	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Band A oscillator						
Frequency range		f_A	80	–	216	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2					
Frequency range		f_B	160	–	470	MHz
Noise figure	pins 22 and 23;					
	200 MHz	NF	–	8	10	dB
	470 MHz	NF	–	8	10	dB
Input admittance	see Fig. 5					
Available input power	1% cross-modulation; in channel; pins 22 and 23;					
	200 MHz	P_{AI}	–24	–21	–	dBm
	470 MHz	P_{AI}	–24	–21	–	dBm
10 kHz pulling	pins 22 and 23; in channel;					
	470 MHz		–	–11	–	dBm
N+5 – 1 MHz pulling	note 3;					
	430 MHz		–	–11	–	dBm
Voltage gain	note 4;					
	200 MHz	G_V	33	36	39	dB
	470 MHz	G_V	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	500	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	500	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.		max.	unit
Band C mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2						
Frequency range		f_C	430	–		860	MHz
Noise figure	pins 20 and 21;						
	430 MHz	NF	–	9		11	dB
	860 MHz	NF	–	9		11	dB
Input admittance	see Fig. 6						
Available input power	1% cross-modulation in channel; pins 20 and 21;						
	430 MHz	P_{AI}	–25	–21		–	dBm
	860 MHz	P_{AI}	–25	–21		–	dBm
10 kHz pulling	pins 20 and 21; in channel;						
	860 MHz		–	–20		–	dBm
N+5 – 1 MHz pulling	note 3;						
	820 MHz		–42	–35		–	dBm
Voltage gain	note 4;						
	430 MHz	G_v	33	36		39	dB
	860 MHz	G_v	33	36		39	dB
Band C oscillator							
Frequency range		f_C	470	–		900	MHz
Frequency shift	$\Delta V_b = 10\%$	Δf	–	–		400	kHz
Frequency drift	$\Delta T = 25\ ^oC$	Δf	–	–		800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–		200	kHz
				mod.	phase		
IF Amplifier	note 5; differentially measured at 36 MHz; see Fig. 7						
Input reflection coefficient		S_{11}	–	–0,5	–2.0	–	dB/deg
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/deg
Forward transmission coefficient		S_{21}	–	12	160	–	dB/deg
Output reflection coefficient	see Fig. 8	S_{22}	–	–9	10	–	dB/deg

parameter	conditions	symbol	min.	typ.	max.	unit
LO output						
Output voltage into 50 Ω resistor		V_{27-28}	14	35	100	mV
Spurious signal on LO output with respect to LO output signal	note 6	SRF	–	–	−10	dB
LO signal harmonics with respect to LO signal	measured at 50 Ω	SHD	–	–	−10	dB

Notes to the characteristics

1. Measured with an input circuit for optimum noise. (See Fig. 3).

DEVELOPMENT DATA

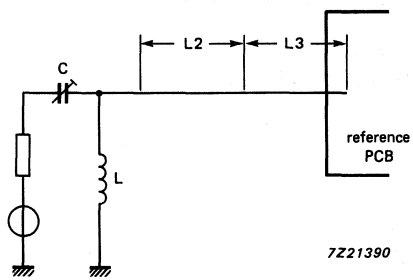


Fig. 3 Input circuit for optimum noise.

Table 1 Component values

component	f = 50 MHz	f = 180 MHz
L	13 t, ϕ 5.5 mm, wire 0.7 mm	*
L2	rigid cable, 2.9 cm	*
L3	rigid cable, 4 cm	*
C	9.6 pF	*

* Value to be fixed.

Notes to the characteristics (continued)

Table 2 Electrical parameters of the circuit (for appropriate impedance and selectivity)

parameter	f = 50 MHz	f = 180 MHz	unit
Insertion loss	0.3	*	dB
Bandwidth	8	*	MHz
Image suppression	15	*	dB
Output impedance (source for IC)	2	*	kΩ

2. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
3. The input level of a N+5 − 1 MHz signal (just visible).
4. The gain is defined as the transducer gain (measured in Fig. 9) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
5. All S parameters are referred to a 50 Ω system.
6. Measured with 50 Ω output impedance on pins 26 and 27 and a RF input signal level of:
   RF level = 1 V at $f < 180$ MHz
   RF power = 0.5 dBm at 100 MHz $< f <$ 225 MHz
   RF power = −10 dBm at 225 MHz $< f <$ 860 MHz

* Value to be fixed.

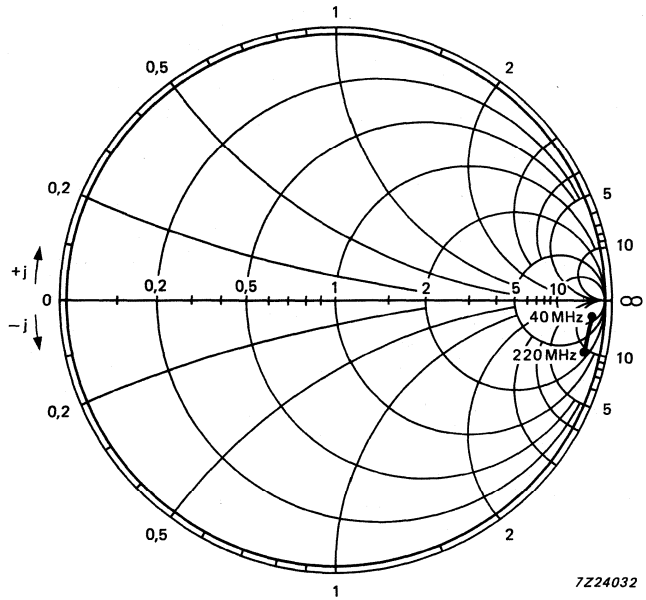


Fig. 4 S11 of the band A mixer input (40 to 220 MHz).

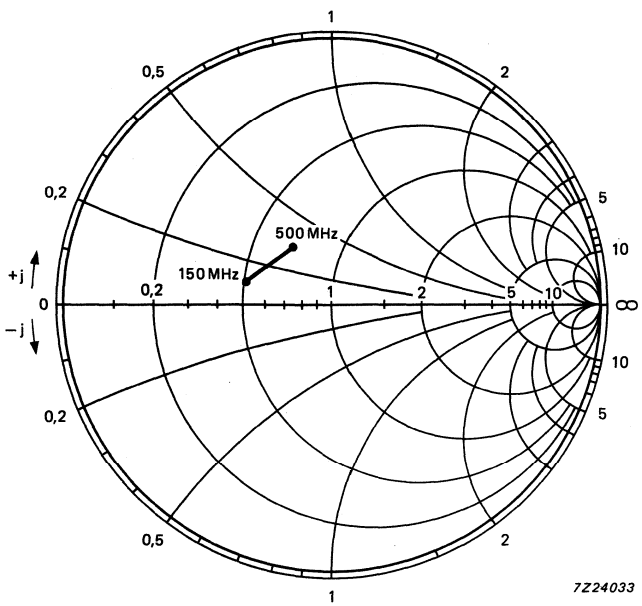


Fig. 5 S11 of the band B mixer input (150 to 500 MHz).

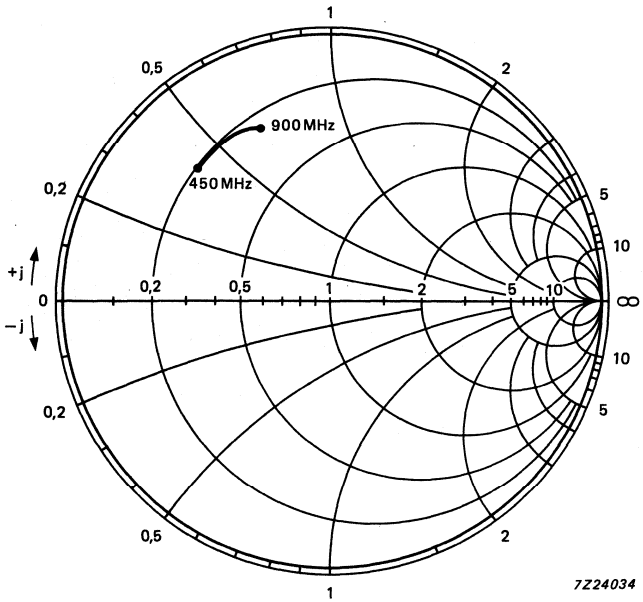


Fig. 6 S11 of the band C mixer input (450 to 900 MHz).

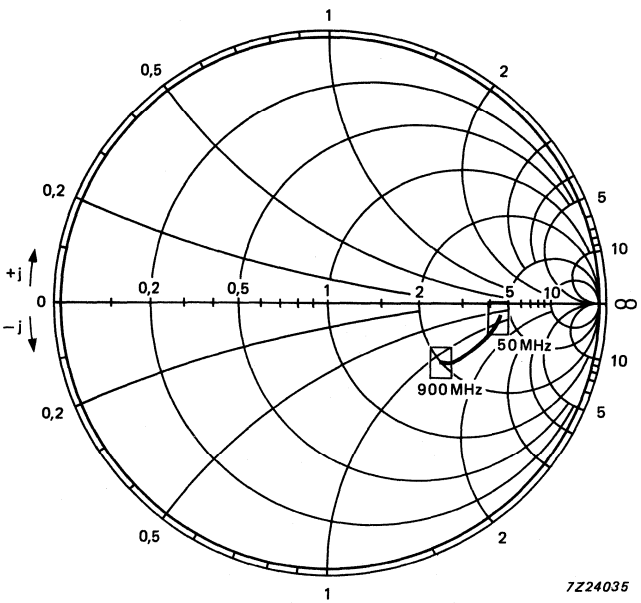


Fig. 7 S11 of the LO output (50 to 900 MHz).

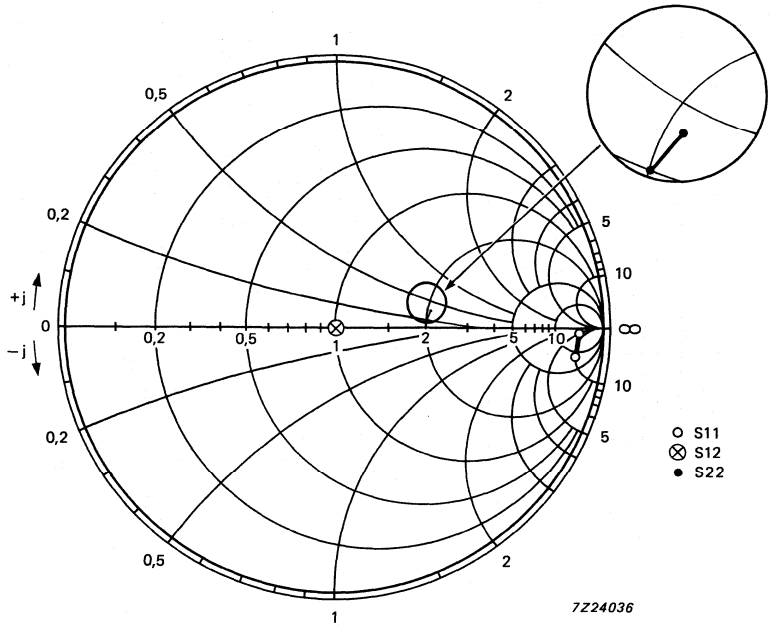


Fig. 8 S11, S12 and S22 of the IF amplifier (30 to 60 MHz).

DEVELOPMENT DATA

APPLICATION INFORMATION

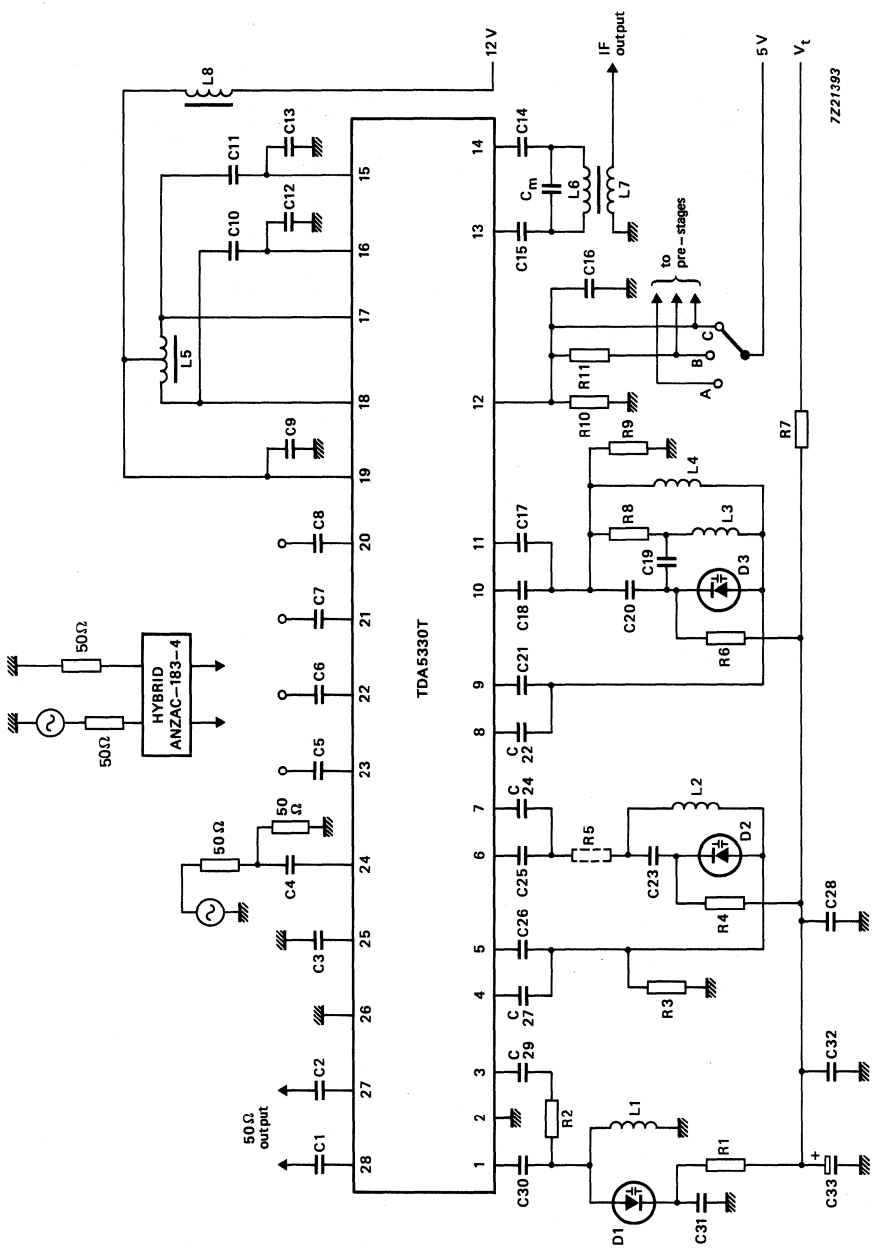


Fig. 9 Test circuit diagram.

Component values of the test circuit

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 22 kΩ	R4 = 22 kΩ
R5 = 22 Ω (SMD)	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 22 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 1 nF
C9 = 1 nF	C10 = 1 nF	C11 = 1 nF	C12 = 15 pF (N750)
C13 = 15 pF (N750)	C14 = 1 nF	C15 = 1 nF	C16 = 1 nF
C17 = 0.68 pF (SMD)	C18 = 1 pF (SMD)	C19 = 100 pF (SMD)	C20 = 5.6 pF (SMD)
C21 = 1 pF	C22 = 0.68 pF (SMD)	C23 = 150 pF (N750)	C24 = 1.8 pF (N750)
C25 = 3.3 pF (SMD)	C26 = 3.3 pF (SMD)	C27 = 1.8 pF (SMD)	C28 = 1 nF
C29 = 1 pF (NPO)	C30 = 1 pF (NPO)	C31 = 82 pF (N750)	C32 = 1 nF
C33 = 1 μF (40 V)	Cm = 18 pF (N750)		

diodes and IC

D1 = BB911	D2 = BB909B	D3 = BB405B
IC = TDA5330T		

coils

L1 = 6.5 t (ϕ3)	L2 = 1.5 t (ϕ3)	L3 = 1.5 t (ϕ3)	L4 = 1.5 t (ϕ3)
L5 = 2 x 6 t*	L6 = 12 t*	L7 = 2 t (mounted on L6)	L8 = 5 μH (choke coil)

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

DEVELOPMENT DATA

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

DOUBLE MIXER/OSCILLATOR FOR TV AND VCR TUNERS

GENERAL DESCRIPTION

The TDA5332T is an integrated circuit that performs the mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B
- Balanced oscillator for band B
- SAW filter preamplifier with an output impedance of 75 Ω in application
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	12	–	V
Band A frequency range	depending on application	f_A	45	–	470	MHz
Band B frequency range	depending on application	f_B	160	–	860	MHz
Band A noise factor	50 MHz	NF_A	–	7.5	–	dB
Band B noise factor	860 MHz	NF_B	–	9	–	dB
Band A input voltage	1% cross-modulation	V_{18-20}	–	100	–	dBμV
Band B input power	1% cross-modulation note 5	P_I	–	–21	–	dBm
Band A voltage gain		G_{VA}	–	25	–	dB
Band B voltage gain		G_{VB}	–	36	–	dB

PACKAGE OUTLINE

20-lead mini-pack, plastic (SO20L; SOT163A).

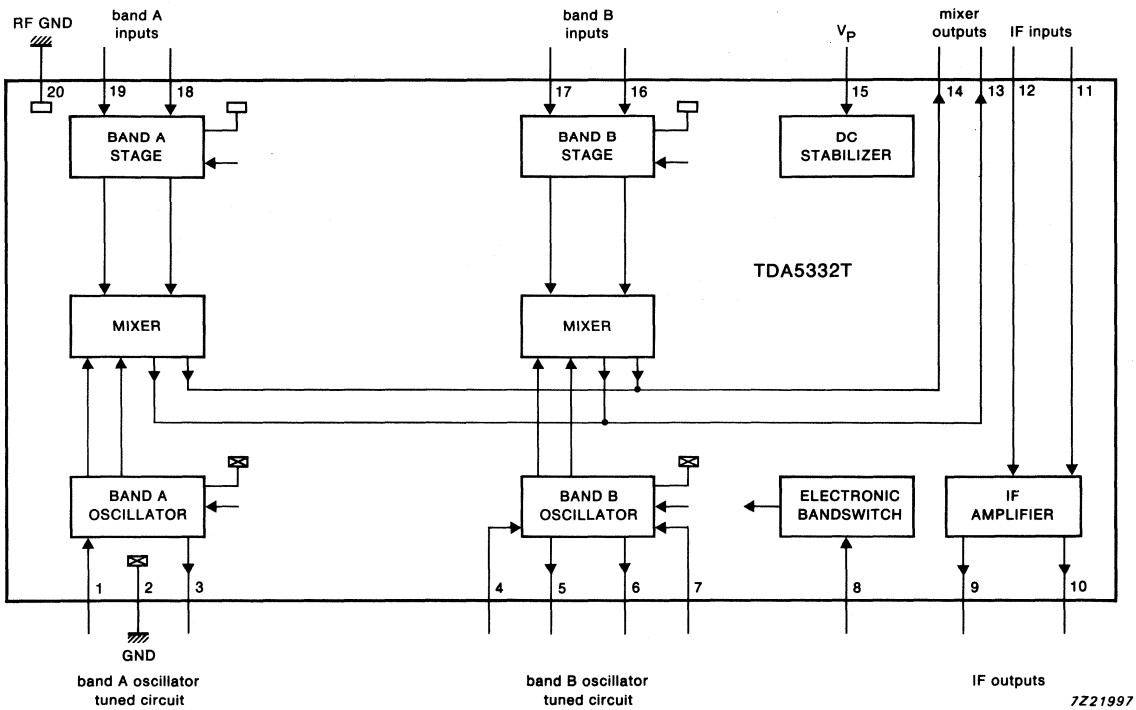


Fig.1 Block diagram.

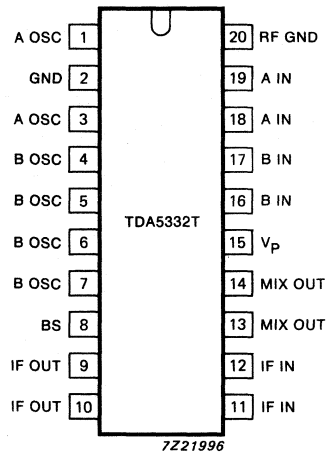


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	BS	electronic bandswitch
9	IF OUT	IF amplifier output
10	IF OUT	IF amplifier output
11	IF IN	IF amplifier input
12	IF IN	IF amplifier input
13	MIX OUT	mixer output
14	MIX OUT	mixer output
15	V_P	positive supply voltage
16	B IN	band B input
17	B IN	band B input
18	A IN	band A input
19	A IN	band A input
20	RF GND	ground for RF inputs

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	−0.3	14	V
Switching voltage		V_8	0	14	V
Output current of each pin to ground		I_O	–	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	–	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C
Junction temperature		T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 100 K/W

HANDLING

Pins 8, 9 and 10 withstand the ESD test in accordance with MIL-STD-883C category B (2000 V).

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pins 2 and 20); measured in Fig.3; unless otherwise specified.

parameter	conditions	symbol	min.	typ.		max.	unit
Supply voltage		V_{15}	10	–		13.2	V
Supply current		I_{15}	–	42		55	mA
Switching voltage;							
band A		V_{SA}	0	–		1.1	V
band B		V_{SB}	3	–		5	V
Switching current							
band A		I_{SA}	–	–		10	μA
band B		I_{SB}	–	–		50	μA
IF Amplifier	differentially measured at 36 MHz			mod.	phase		
Input reflection coefficient	note 4	S_{11}	–	–0.5	–2	–	dB/°
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/°
Forward transmission coefficient		S_{21}	–	12	160	–	dB/°
Output reflection coefficient		S_{22}	–	–9	10	–	dB/°
Input admittance in application		Y_I	–	–	1.4	–	mS
					0.9	–	pF
Output admittance in application		Z_O	–	–	55	–	Ω
					230	–	nH
Band A mixer (including IF amplifier)	measured using circuit shown in Fig.3						
Frequency range		f_A	45	–		470	MHz
Noise factor	50 MHz	NF	–	7.5		9	dB
	225 MHz	NF	–	9		11	dB
	300 MHz	NF	–	10		12	dB
	470 MHz	NF	–	11		13	dB
Optimum source conductance	50 MHz	$G_{18\text{-}20}$	–	0.5		–	mS
	225 MHz	$G_{18\text{-}20}$	–	1.1		–	mS
	300 MHz	$G_{18\text{-}20}$	–	1.2		–	mS
	470 MHz	$G_{18\text{-}20}$	–	1.9		–	mS

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	50 - 470 MHz	C_{18-20}	–	2.5	–	pF
Input voltage	1% cross-modulation; in channel	V_{18-20}	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel; f < 300 MHz	V_{18-20}	100	108	–	dBμV
Voltage gain	20 log (V_{9-10}/V_{18})	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$I_{13}/V_{18} = -I_{14}/V_{18}$	C_t	–	3.5	–	mS
Mixer output admittance	pins 13 and 14		–	0.1	–	mS
Mixer output capacitance		C_{13-14}	–	2	–	pF
Band A oscillator						
Frequency range		f_A	80	–	520	MHz
Frequency shift	ΔV_P = 10% note 6; f = 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C note 7; f = 330 MHz	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on; f = 330 MHz	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig.3; measurements using hybrid; note 1					
Frequency range		f_B	160	–	860	MHz
Noise factor not corrected for image	pins 16 and 17					
	160 MHz	NF_B	–	9	11	dB
	860 MHz	NF_B	–	9	11	dB
Available input power	note 5; 1% cross-modulation; in channel; pins 16 and 17;					
	160 MHz	P_{IB}	–25	–21	–	dBm
	860 MHz	P_{IB}	–25	–21	–	dBm
10 kHz pulling	note 5; pins 16 and 17; in channel;					
	860 MHz		–	–20	–	dBm

DEVELOPMENT DATA

CHARACTERISTICS (continued)

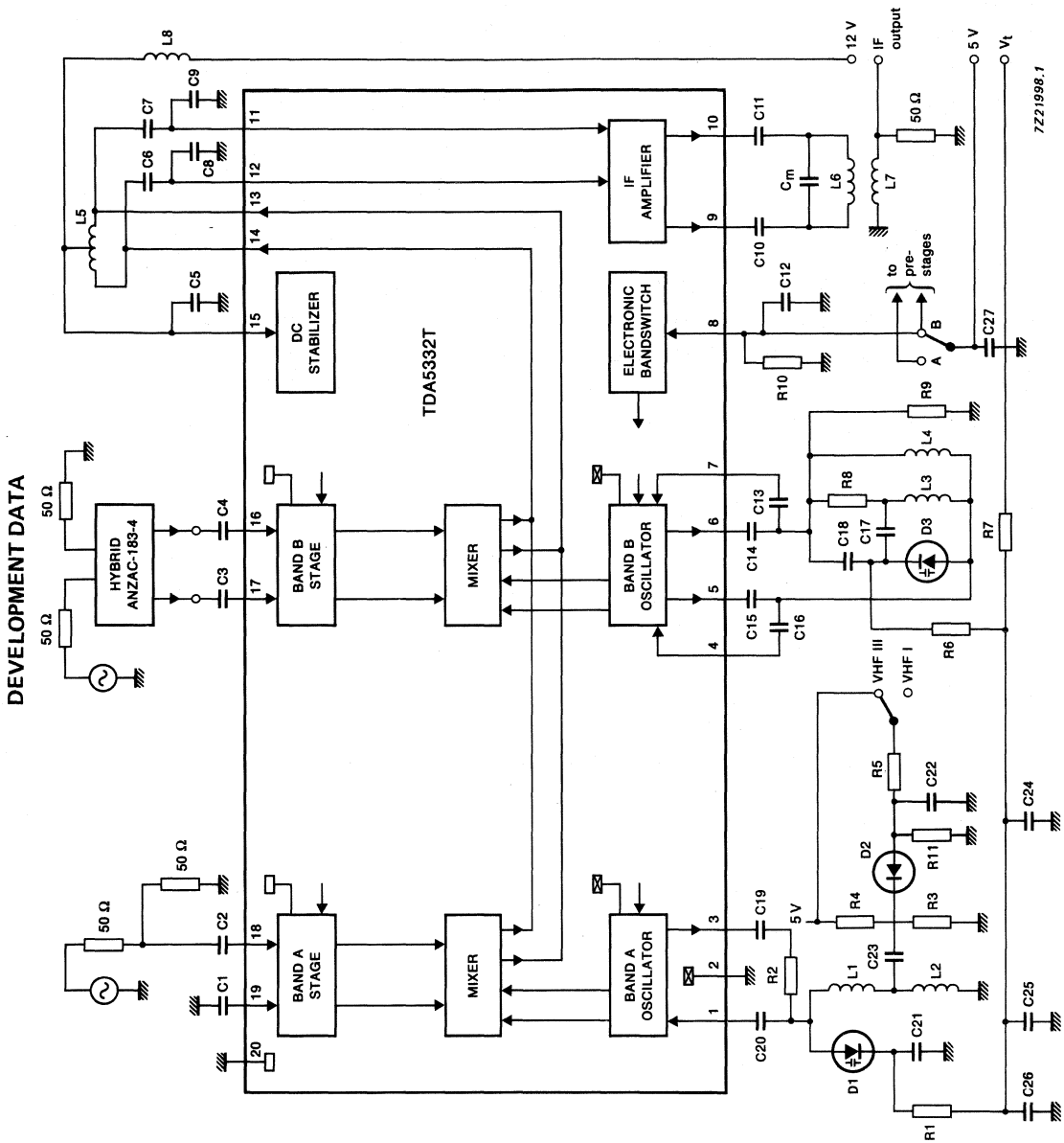
parameter	conditions	symbol	min.	typ.	max.	unit
N + 5 – 1 MHz pulling	notes 2 and 5; 820 MHz		–42	–35	–	dBm
Voltage gain	note 3;					
	160 MHz	G_{VB}	33	36	39	dB
	860 MHz	G_{VB}	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	900	MHz
Frequency shift	note 6; ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	note 7; ΔT = 25 °C	Δf	–	–	800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	400	kHz

Notes to the characteristics

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. The input level of a N + 5 – 1 MHz signal (just visible).
3. The gain is defined as the transducer gain (measured in Fig.3) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
4. All S parameters are referred to a 50 Ω system.
5. The input power is defined as the power delivered by the generator on a 50 Ω load.
6. The frequency shift is defined for a variation of power supply from;
   (a) V_P = 12 V to V_P = 10.8 V
   (b) V_P = 12 V to V_P = 13.2 V
   In both cases the frequency shift is below the specified value.
7. The frequency drift is defined for a variation of ambient temperature from;
   (a) T_{amb} = 25 °C to T_{amb} = 0 °C
   (b) T_{amb} = 25 °C to T_{amb} = 50 °C
   In both cases the frequency shift is below the specified value.

APPLICATION INFORMATION

DEVELOPMENT DATA



Proposal of VHF/UHF tuner band A = VHF I + VHF III (45 to 300 MHz)
band B = UHF (470 to 900 MHz)

Fig.3 Application diagram.

Component values of the application diagram

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 1.2 kΩ	R4 = 4.7 kΩ
R5 = 100 Ω	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 47 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 15 pF (N750)
C9 = 15 pF (N750)	C10 = 1 nF	C11 = 1 nF	C12 = 1 nF
C13 = 0.68 pF (SMD)	C14 = 1 pF (SMD)	C15 = 1 pF (SMD)	
C16 = 0.68 pF (SMD)	C17 = 100 pF (SMD)	C18 = 5.6 pF (SMD)	C19 = 1 pF (NPO)
C20 = 1 pF (NPO)	C21 = 82 pF (N750)	C22 = 1 nF	C23 = 1 nF
C24 = 1 nF	C25 = 1 nF	C26 = 1 μF (40V)	C27 = 1 nF

Cm = 18 pF (N750)

diodes and IC

D1 = BB911	D2 = BA482	D3 = BB405B	IC = TDA5332T

coils

L1 = 2.5 t (ϕ3)	L2 = 8.5 t (ϕ3)	L3 = 1.5 t (ϕ3)
L4 = 1.5 t (ϕ3)	L5 = 2 x 5 t*	L8 = 5 μH (choke coil)

transformer

L6 = 12 t*	L7 = 2 t

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

8 MHz VIDEO OUTPUT AMPLIFIER

GENERAL DESCRIPTION

The TDA6100Q is a video amplifier in a SIL 9 MP (Single In Line 9 pins Medium Power) package, using high-voltage DMOS technology and is intended to directly drive the cathode of a cathode ray tube (CRT).

Features

- High bandwidth and slew rate
- No external heatsink required
- Black-current measurement output for automatic black-current stabilization (ABS)
- A cathode output separated from the feedback output
- Internal protection against CRT flashover discharges
- Protection against electrostatic discharge (ESD)
- Simple application with a variety of colour decoders
- Differential input with designed-in maximum values of the following:
  - common mode input capacitance of 3 pF
  - differential mode input capacitance of 2 pF
  - differential input voltage temperature drift of 0.4 mV/K

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
High supply voltage	V_{P1}	180	–	210	V
Low supply voltage	V_{P2}	10.8	–	13.2	V
Total power dissipation	P_{tot}	0	–	1.9	W
Operating ambient temperature range	T_{amb}	0	–	+ 65	°C

PACKAGING OUTLINE

9-lead SIL; plastic (SOT111B).

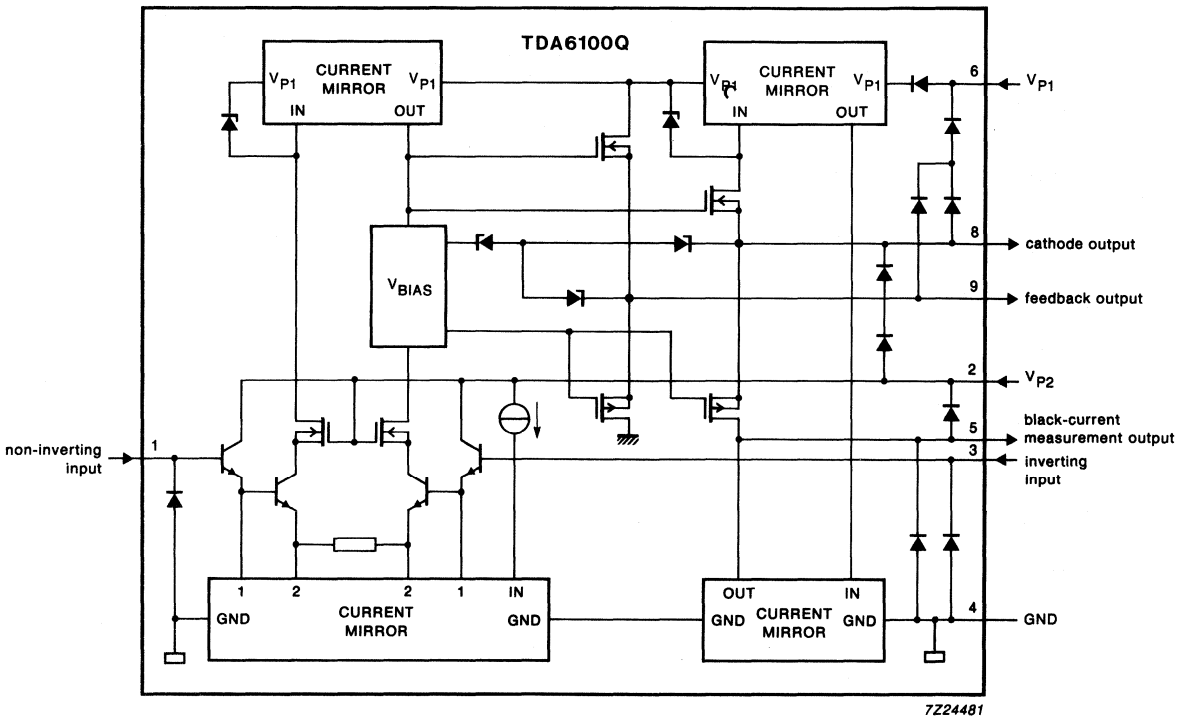


Fig.1 Block diagram.

PINNING

1 Non-inverting input
2 Low supply voltage
3 Inverting input
4 Ground, substrate, heat tab
5 Black-current measurement output
6 High supply voltage
7 Not connected
8 Cathode output
9 Feedback output

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	typ.	max.	unit
High supply voltage		V_{P1}	0	–	250	V
Low supply voltage		V_{P2}	0	–	14	V
Input voltage (pins 1 and 3)		V_1, V_3	0	–	V_{P2}	V
Differential mode input voltage (pin 1 to 3)		V_{1-3}	−6	–	6	V
Black-current measurement output voltage (pin 5)		V_5	0	–	V_{P2}	V
Cathode and feedback output voltage (pins 8 and 9)		V_8, V_9	V_{P2}	–	V_{P1}	V
Non-inverting and inverting input current (pins 1 and 3)		I_1, I_2	0	–	1	mA
Cathode and feedback repetitive peak output current (pins 8 and 9)		I_8, I_9	−25	–	+ 25	mA
Cathode non-repetitive peak output current						
LOW	Q = 50 μC	I_8	−2.5	–	+ 2.5	A
HIGH	Q = 100 nC	I_8	−10	–	+ 10	A
Total power dissipation		P_{tot}	0	–	1.9	W
Storage temperature range		T_{stg}	−65	–	+ 150	°C
Junction temperature range		T_j	0	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	45 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W

CHARACTERISTICS

Operating range

V_{P1} = 180 to 210 V; V_{P2} = 10.8 to 13.2 V; V_1 = 2.6 to 5 V; V_5 = 1.4 V to the smallest of (V_8 − 8 V) or V_{P2}; T_{amb} = 0 to 65 °C.

Test conditions (unless otherwise specified)

V_{P1} = 200 V; V_{P2} = 12 V; V_5 = 6 V; T_{amb} = 25 °C; C_L = 10 pF; V_1 = 5 V (C_L consists of parasitic and cathode capacitance). For test circuit see Fig.2.

parameter	conditions	symbol	min.	typ.	max.	unit
Quiescent current						
high voltage supply	$V_8 = V_{P1}/2$	I_{P1}	4	4.9	6	mA
low voltage supply	$V_8 = V_{P1}/2$	I_{P2}	2.5	3.1	3.8	mA
Input bias current	$V_8 = V_{P1}/2$		0	–	20	μA
Input offset current	$V_8 = V_{P1}/2$		−3	–	+3	μA
Offset current of black-current measurement output	I_8 = 0 A; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$I_{5(off)}$	−10	0	+10	μA
Linearity of current transfer						
LOW I_8	I_8 = 0 to 10 μA; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
HIGH I_8	I_8 = 0 to 3 mA; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
Maximum peak output current (pins 8 and 9)	20 V < V_8 < V_{P1} − 20 V	$\lvert I_{O\,max}\rvert$	–	20	–	mA
Input offset voltage	$V_8 = V_{P1}/2$	$V_{I(off)}$	−50	–	+50	mV
Output voltage (pins 8 and 9)						
minimum	V_{1-3} = −1 V	$V_{O\,min}$	–	–	20	V
maximum	V_{1-3} = 1 V	$V_{O\,max}$	V_{P1} −20	–	–	V
Gain-bandwidth product of open loop gain V_9/V_{1-3}	f = 500 kHz; $V_{8(p-p)}$ = 60 V	BW_g	–	0.7	–	GHz
Small signal bandwidth	$V_{8(p-p)}$ = 60 V sine	BW_s	6.5	8	–	MHz
Large signal bandwidth	$V_{8(p-p)}$ = 100 V sine	BW_l	5	6.5	–	MHz
Cathode output propagation time 50% input – 50% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_p	40	51	62	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Cathode output rise time 10% output – 90% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_r	40	53	65	ns
Cathode output fall time 90% output – 10% output	V_8 = 150 to 50 V square wave; f < 1 MHz; t_r input < 20 ns	t_f	40	53	65	ns
Settling time; 50% input – 99% < output < 101%	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	t_s	–	–	220	ns
Slew rate between 50 and 150 V	$V_{1-3(p-p)}$ = 2 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	SR	–	1700	–	V/μs
Cathode output voltage overshoot	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns; note 1	OV	–	–	5	%
Differential input resistance		R_I	–	100	–	kΩ
High voltage power supply rejection ratio	f < 50 kHz; note 2	HVPSRR	–	80	–	dB
Low voltage power supply rejection ratio	f < 50 kHz; note 2	LVPSRR	–	80	–	dB

DEVELOPMENT DATA

Notes to the characteristics

1. If $V_{P2} - V_1 < 7$ V, there can be more overshoot than specified.
2. PSRR: the ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.
3. The above electrical characteristics and stable operation are specified for a feedback range of 1/75 to 1/90.
4. The cathode output is protected against peak currents (caused by high-resistance flash) of 2.5 A maximum with a charge content of 50 μC.
5. The cathode output is also protected against peak currents (caused by low-resistance flash) of 10 A maximum with a charge content of 100 nC.

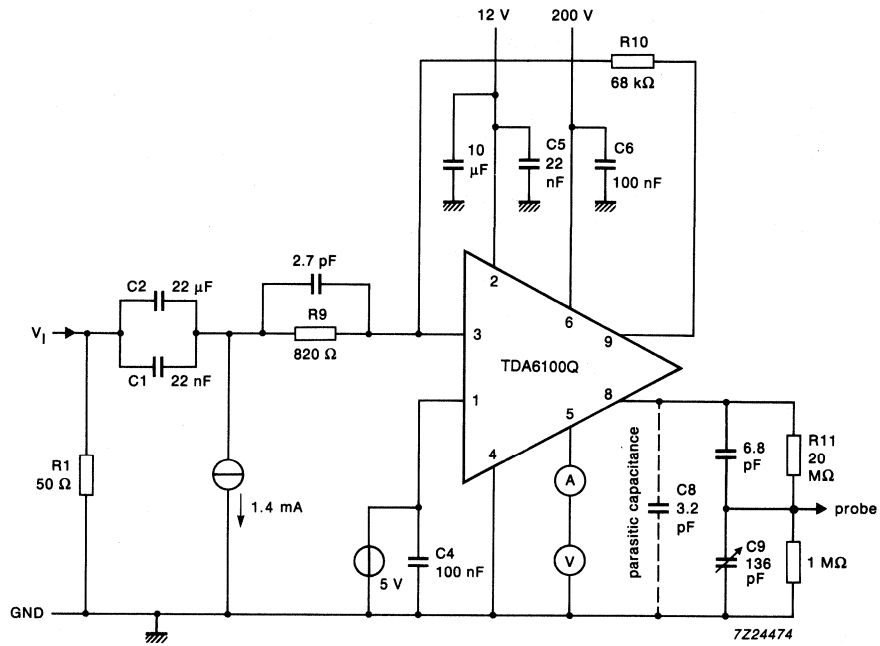


Fig.2 Test circuit with feedback factor of 1/83.

FLASHOVER PROTECTION

The device incorporates protection diodes to prevent CRT flashover discharges; these diodes clamp the cathode output voltage between $V_{P1} + V_{diode}$ and $V_{P2} - V_{diode}$. To limit the diode current the following is needed: an external 1.5 kΩ high-voltage carbon resistor in series with the cathode output and a 1 kV spark-gap (see Fig.9).

V_{P1} – GND has to be decoupled:

- With a capacitor > 20 nF with good HF characteristics (e.g. ceramic). This capacitor (between pins 6 and 4) must be placed as near as possible to the device and no more than 10 mm away from it.
- With a capacitor > 10 µF on the CRT's printed-circuit board (common for the three output stages).

V_{P2} – GND has to be decoupled with a capacitor > 20 nF on the CRT's printed-circuit board.

APPLICATION INFORMATION

Dissipation

There are two components of the dissipation – static dissipation (independent of the frequency) and dynamic dissipation (proportional to the frequency).

The static dissipation is due to both high- and low-voltage supply currents and load currents in the feedback network and CRT and is given by:

$P_{stat} = (V_{P1} \times I_{P1}) + (V_{P2} \times I_{P2}) + (V_8 \times I_8) - (V_9 \times V_9/R_{fb})$.

Where $V_9 = V_8 = 100$ V; feedback resistor $R_{fb} = 68$ kΩ; $I_8 = 0.3$ mA and other typical conditions as provided in the **CHARACTERISTICS**. The static dissipation, $P_{stat} = 0.9$ W.

The dynamic dissipation is given by:

$P_{dyn} = V_{P1} \times (C_L + C_{fb} + C_{int}) \times f \times V_{o(p-p)} \times b$.

Where load capacitance $C_L = 10$ pF; feedback capacitance $C_{fb} = 0$; internal load capacitance $C_{int} = 4$ pF; sine wave frequency $f = 4$ MHz; peak-to-peak output voltage $V_{o(p-p)} = 100$ V and the non-blanking duty factor $b = 80\%$. The dynamic dissipation, $P_{dyn} = 0.9$ W.

To minimize the load capacitance, C_L, TDA6100 must be mounted on the printed-circuit board at the base of the CRT.

The total dissipation, $P_{tot} = P_{stat} + P_{dyn} = 1.8$ W under the conditions given.
From $T_j = T_{amb} + (P_{tot} \times R_{th\ j\text{-}a}) < T_{j,\ max} = 150\ ^oC$, it follows that no additional heatsink is required for $T_{amb} < T_{amb\ max} = 65\ ^oC$.

Black-current stabilization

To use the black-current stabilization feature, a signal source including a black-current stabilization loop is needed (TDA3562A or TDA4580). The black-current needs to be converted to a voltage by, for example, an 82 kΩ resistor connected to ground and a 150 kΩ resistor connected to V_{P2}. A clamping diode connected to V_{P2} prevents capacitive load currents from causing the voltage to exceed $V_{P2} + V_{diode}$. Care must be taken to minimize the parasitic capacitance at the current-to-voltage conversion node. Both TDA4580 and TDA3562A feature sequential black-current stabilization, therefore the black-current measurement outputs of all three video output stages can be added. To obtain the correct ratio of cathode currents for colour balance at the stabilized black-level, the circuit illustrated by Fig.3 may be used.

The output voltage depends on the currents $I_{5,R}$, $I_{5,G}$ and $I_{5,B}$ as expressed in the following formula:

$$V_O = R4 \times \frac{[(R1 + R2 + R3)I_{5,B} + (R1 + R2)I_{5,G} + (R1)I_{5,R}]}{(R1 + R2 + R3 + R4)}.$$

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

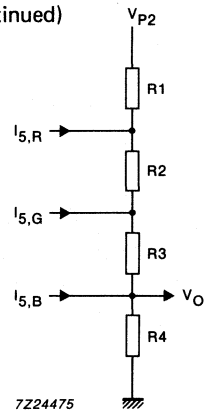


Fig.3 Colour balance diagram.

Figure 4 below illustrates a method for adjusting the ratios of the stabilized black-currents.

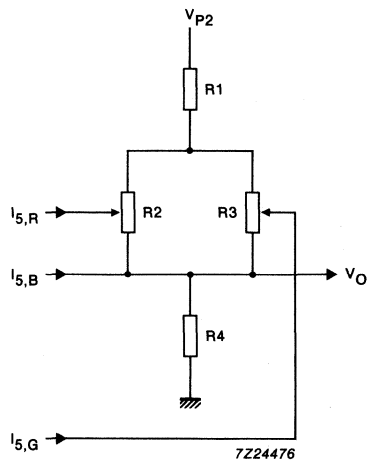


Fig.4 Stabilized black-current adjustment.

The black-current measurement output of the TDA6100Q deals with both positive and negative leakage currents at the cathode output.

Gain and DC biasing

Figure 5 illustrates a circuit in which the gain and the black-level output can be adjusted independently. If the potentiometers have a relatively low value of resistance, the feedback factor remains approximately constant. The input black-level is given by $V_{I,BL}$. Figure 6 illustrates a circuit for this adjustment when ABS is used.

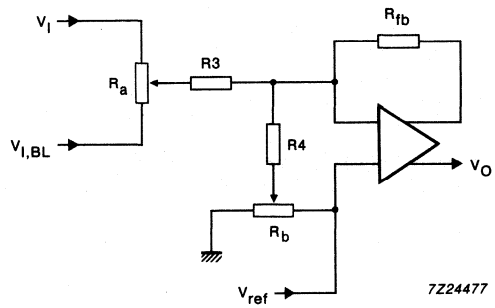


Fig.5 Gain and black-level adjustment.

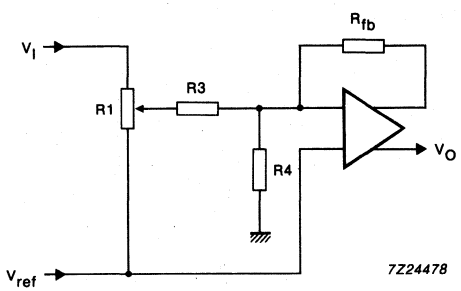


Fig.6 Gain and black-level adjustment with ABS.

APPLICATION INFORMATION (continued)

Referring to the circuit illustrated by Fig.6 the total gain is given by:

$$A = \frac{a \times R_{fb}}{R_a(a\text{-}a^2) + R3} \quad \text{with } 0 \leqslant R_a(a\text{-}a^2) \leqslant R_a/4$$

If the value of the gain is known, then the adjustment of the potentiometer can be found from:

$$a = 0.5 \left\{ \left[\left(\frac{R_{fb}}{A \times R_a} - 1 \right)^2 + \left(4 \times \frac{R3}{R_a} \right) \right]^{1/2} - \left(\frac{R_{fb}}{A \times R_a} - 1 \right) \right\}$$

The feedback factor (stipulating the bandwidth) of the circuit follows from:

$$1/k = 1 + \frac{R_{fb}}{R4//[R3 + R_a(a\text{-}a^2)]}$$

The output black-level is given by:

$$V_{O,BL} = V_{ref} \frac{R_{fb} + R4}{R4} - A(V_{I,BL} - V_{ref})$$

If the value of the black-level is known, then R4 can be calculated as a function of V_{ref} or, V_{ref} as a function of R4, as shown below:

$$R4 = R_{fb} \times \frac{V_{ref}}{V_{O,BL} + A(V_{I,BL} - V_{ref}) - V_{ref}}$$

$$V_{ref} = \frac{V_{O,BL} + A \times V_{I,BL}}{(A + 1 + R_{fb}/R4)}$$

To obtain the required feedback, R3 and R4 or V_{ref} must be chosen. The results can be read from the above formulae.

DC biasing at high gain

When the device is used as an 8 MHz and x 90 gain amplifier with AC coupling of the signal source, DC biasing can be accomplished by using the circuits illustrated by Figs 7 and 8.

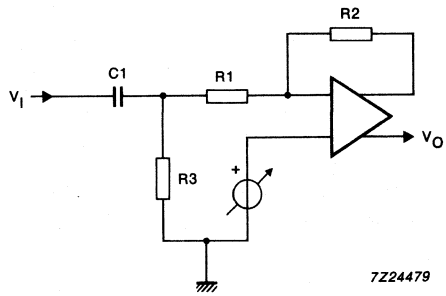


Fig.7 DC biasing using an adjustable voltage source.

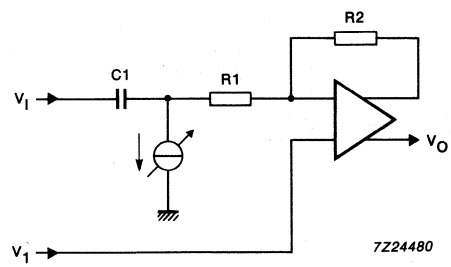
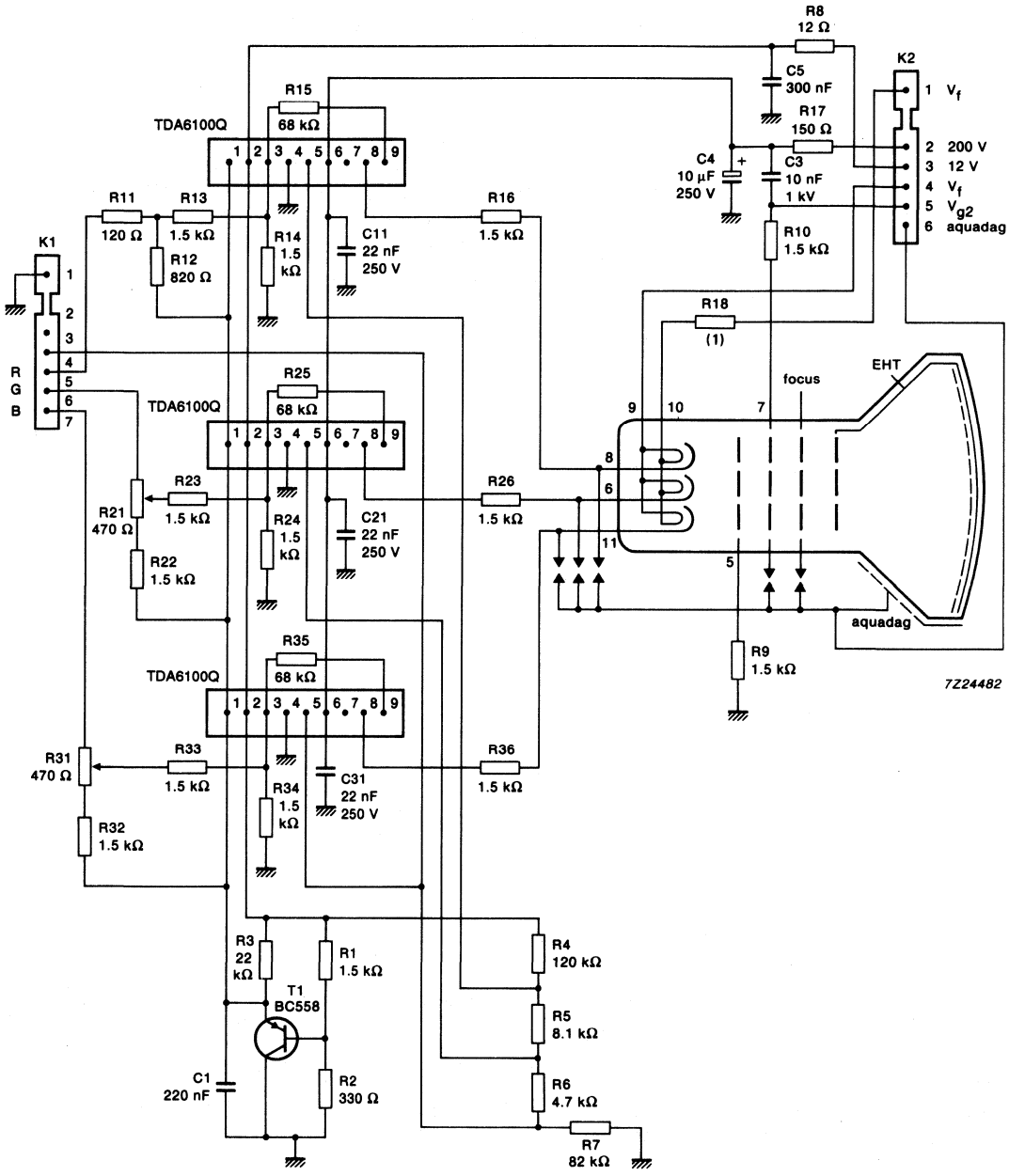


Fig.8 DC biasing using an adjustable current source.

Application circuit

Figure 9 illustrates an application circuit for use with ABS (eg TDA4580), in which a number of components are common for the three output stages.

APPLICATION INFORMATION (continued)



(1) Value to be fixed.

Fig.9 Application circuit for use with ABS (eg TDA4580) using CRT A66EAK00X (30AX).

VIDEO MODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA6800 is a modulator circuit for modulation of video signals on a VHF/UHF carrier. The circuit requires a 5 V power supply and few external components for the negative modulation mode. For positive modulation an external clamp circuit is required. This circuit can be used as a general purpose modulator without additional external components.

Features

- Balanced modulator
- Symmetrical oscillator
- Video clamp circuit for negative modulation
- Frequency range 50 to 800 MHz

QUICK REFERENCE DATA

		min.	typ.	max.	
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	–	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Output voltage (50 MHz)	V_{6-7}	–	13	–	mV
Output voltage (600 MHz)	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation distortion	d_{int}	–	–80	–	dB

PACKAGE OUTLINE

TDA6800 : 8-lead dual in-line; plastic (SOT97A).
TDA6800T: 8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{5-4}	max.	7 V
Input voltage	V_{8-4}	max.	4 V
Output voltage	$V_{6,7-4}$	max.	9 V
Storage temperature	T_{stg}	max.	125 °C
Junction temperature	T_j	max.	125 °C
Operating ambient temperature range	T_{amb}	−25 to + 85	°C

THERMAL RESISTANCE

From junction to ambient in free air

TDA6800T	$R_{th\ j-a}$	260 K/W
TDA6800	$R_{th\ j-a}$	120 K/W

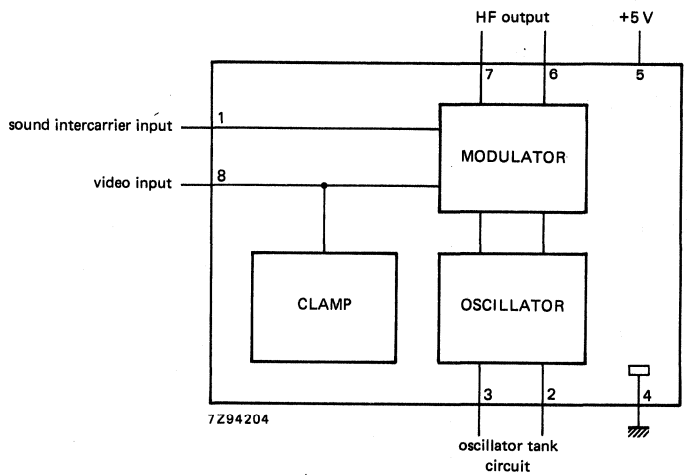


Fig. 1 Block diagram TDA6800 and TDA6800T.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	13	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Voltage (d.c.) at video input (clamp voltage)	V_8	–	1,4	–	V
Voltage (d.c.) at sound input	V_1	–	2,5	–	V
Output voltage f = 50 MHz; R_L = 75 Ω	V_{6-7}	–	13	–	mV
Output voltage f = 600 MHz; R_L = 75 Ω	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation (1,1 MHz) (note 1)		–	–80	–60	dB
Frequency shift V_b = 5%, f = 600 MHz	Δ_f	–	–	100	kHz
Frequency shift V_b = 5%, f = 800 MHz	Δ_f	–	tbf	–	kHz
Frequency drift 25 to 40 °C	Δ_f	–	–	100	kHz
Frequency drift 15 to 55 °C	Δ_f	–	–	300	kHz
Positive modulation (see Fig. 3)					
Residual carrier voltage	V_r	–	–	2,5	%
Cross modulation (note 2)	α	–	0,1	0,25	%

NOTES TO THE CHARACTERISTICS

1. Input signal: d.c. 0,45 V (V_{8-4} = 1,85 V)
   4,4 MHz; input voltage (p-p) = 0,6 V
   5,5 MHz; input voltage (p-p) = 1,26 V
   measured with respect to picture carrier, at f = 600 MHz.
2. Input signal: d.c. 1 V (V_{8-4} = 3,5 V)
   5,5 MHz AM modulated, f_m = 100 kHz
   m = 0,8; input voltage (p-p) = 2,27 V (including modulation)
   measured with respect to the picture carrier, at f = 600 MHz.

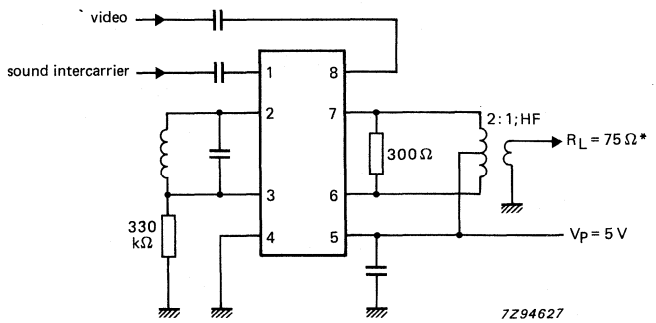


Fig. 2.
Application for negative modulation.

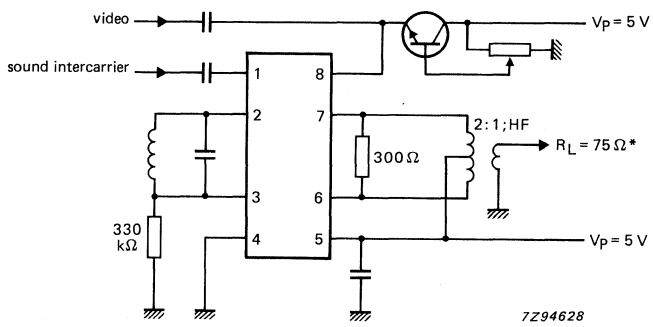


Fig. 3.
Application for positive modulation.

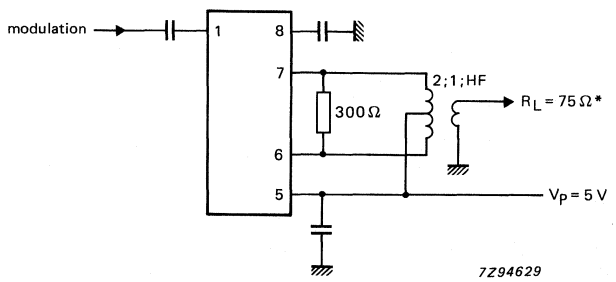


Fig. 4.
Application for general purpose modulation.

* Close to output transformer.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

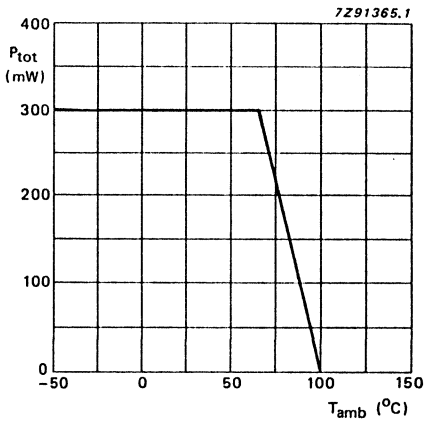


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient $R_{thj\text{-}a}$ = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

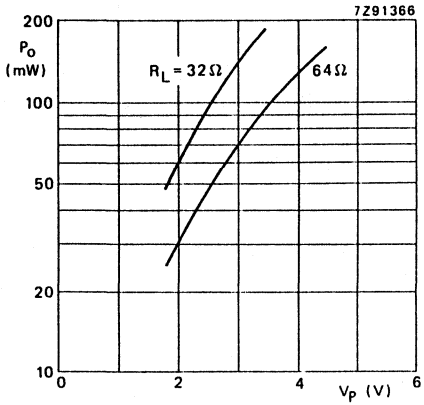


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

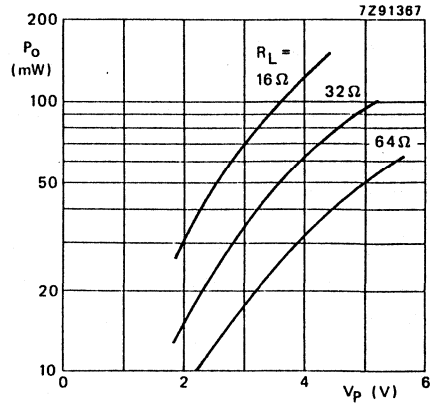


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

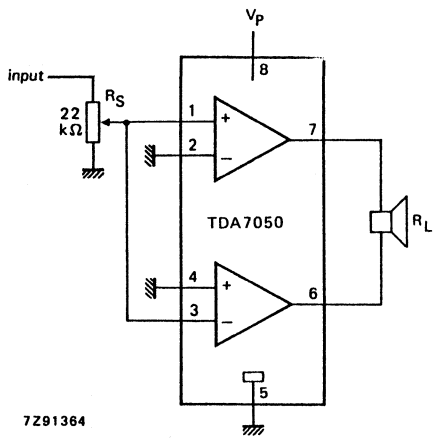


Fig. 4 Application diagram (BTL); also used as test circuit.

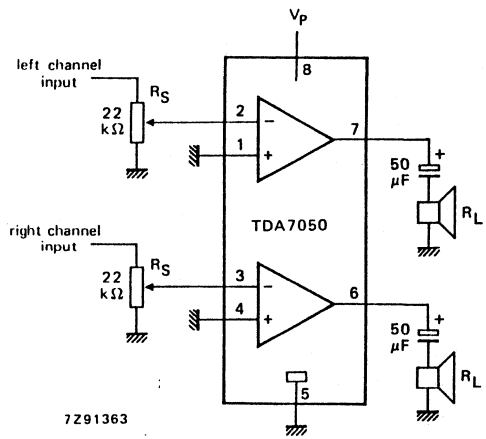


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

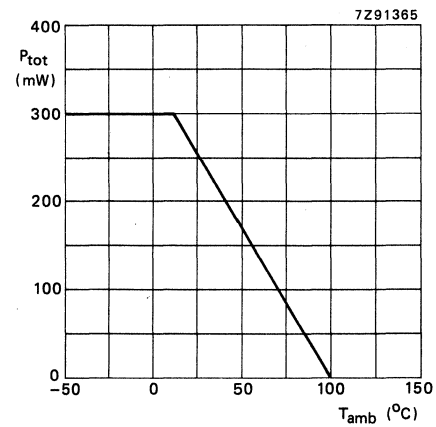


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

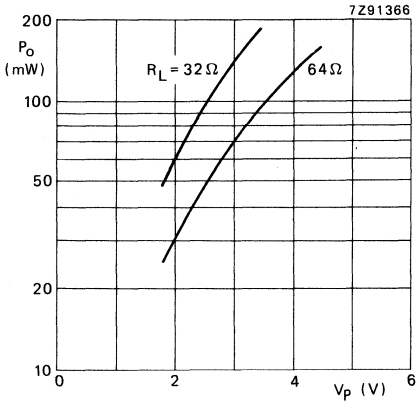


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

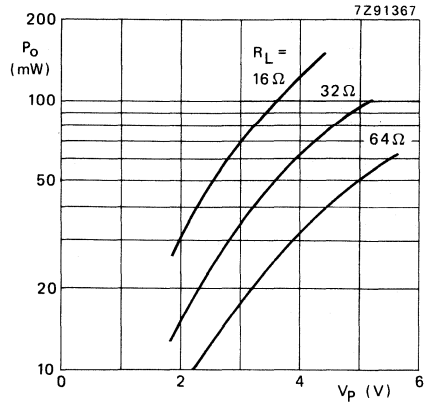


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

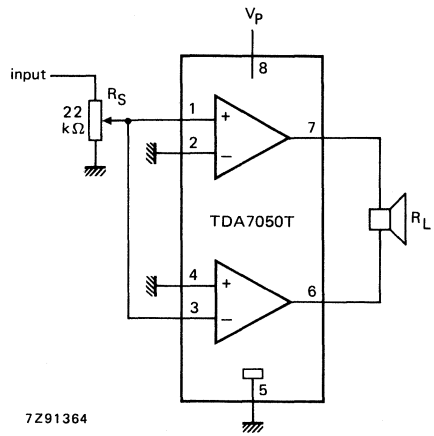


Fig. 4 Application diagram (BTL); also used as test circuit.

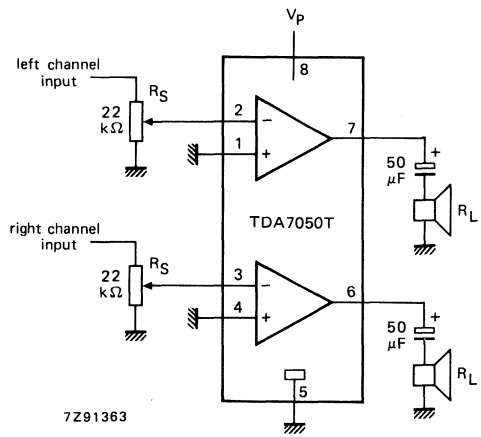


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

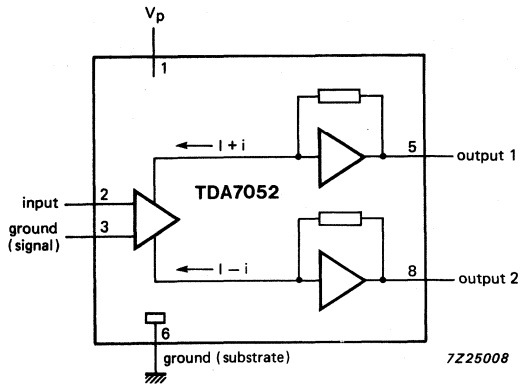


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

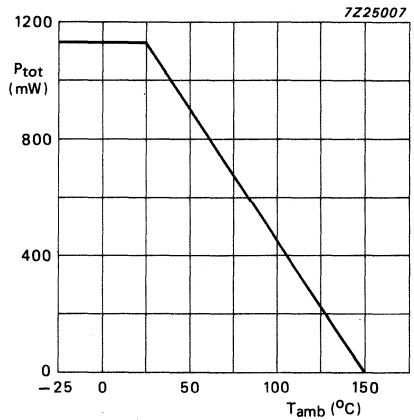


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%	P_o	–	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

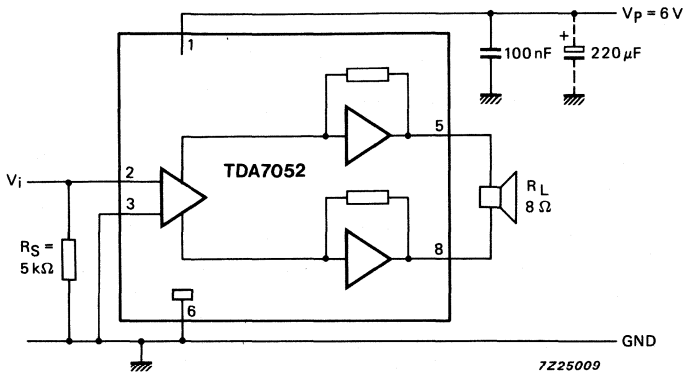


Fig. 3 Application diagram.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_V	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

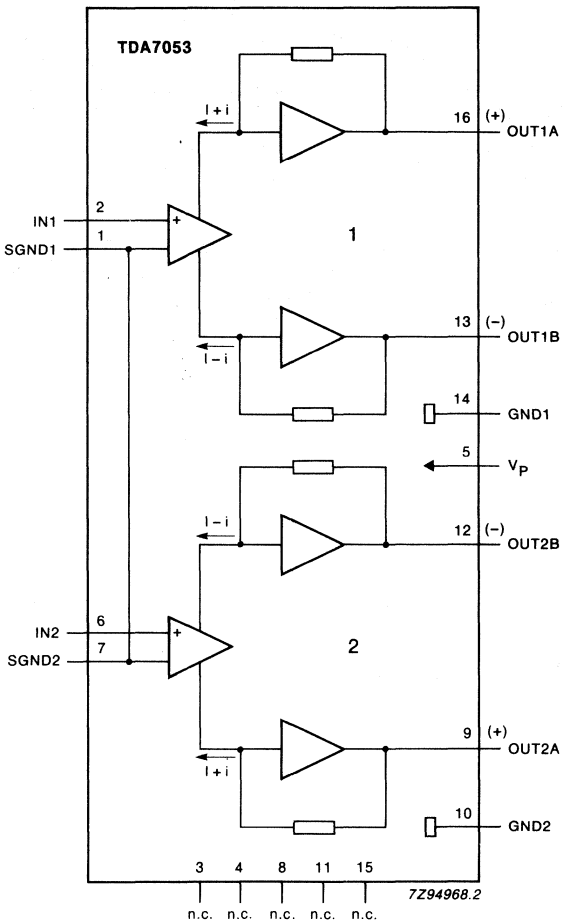


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	−65	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

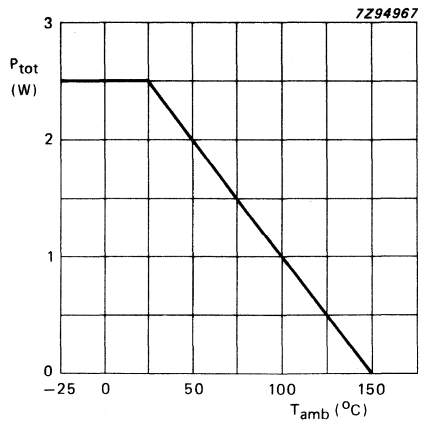


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	R_L = ∞; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_V	38	39	40	dB
Channel balance		ΔG_V	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

APPLICATION INFORMATION

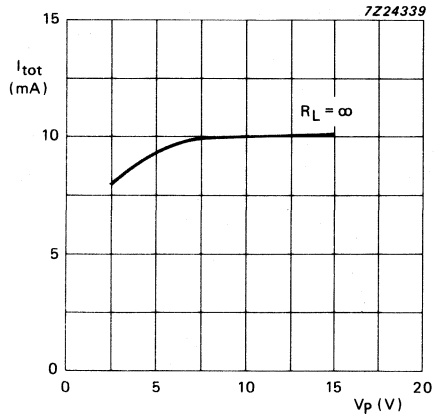


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

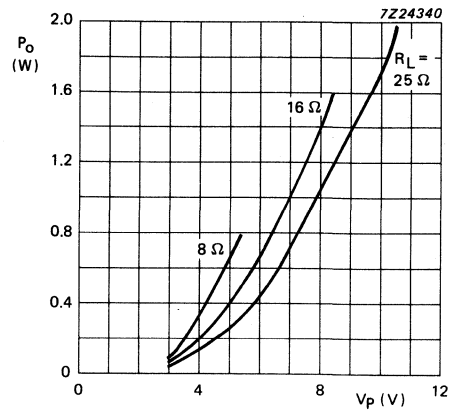
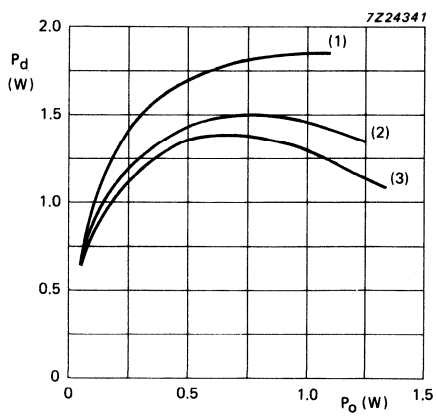
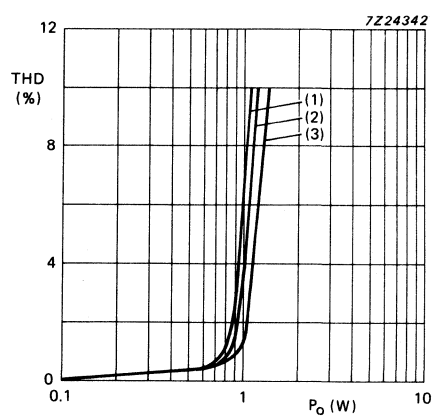


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

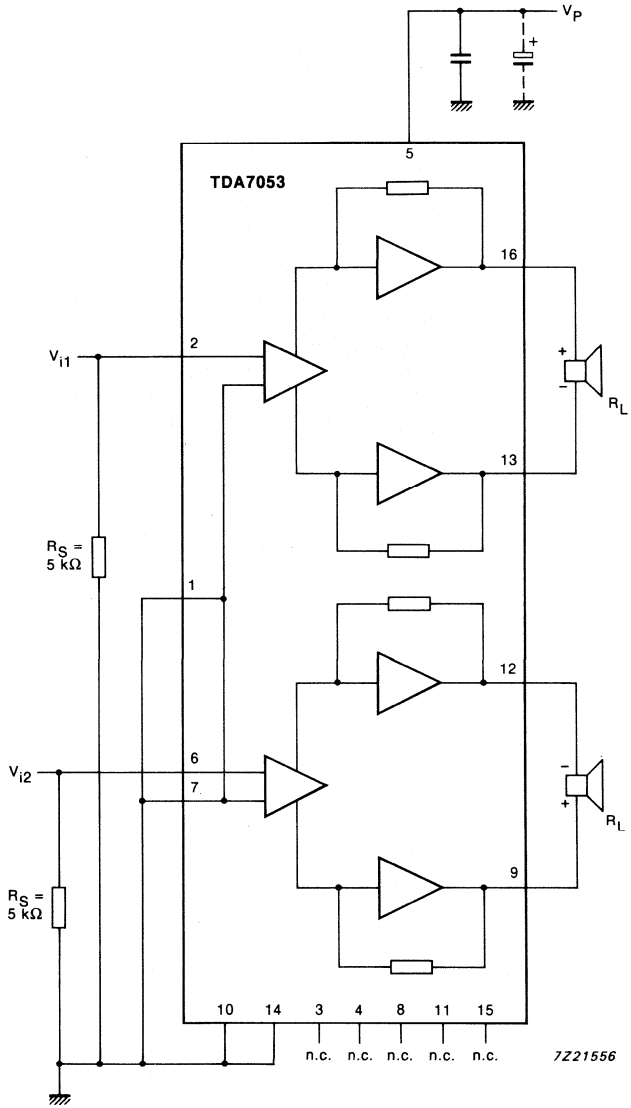


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

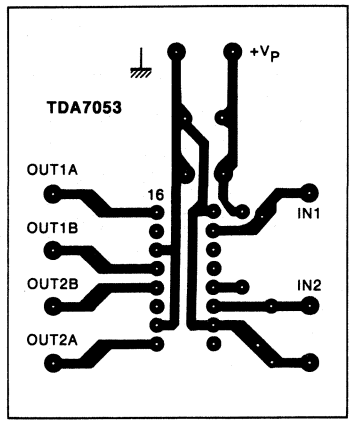


Fig. 8 Printed-circuit board, track side.

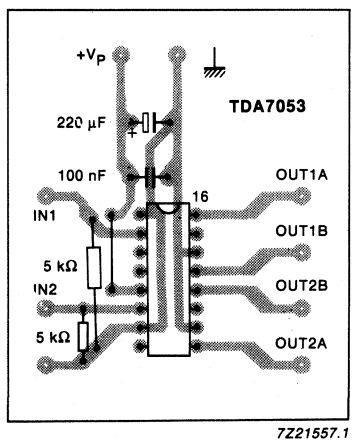


Fig. 9 Printed-circuit board, component side.

SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The TDA8305A is a TV sub-system circuit, for colour television receivers with the following features.

Features

- Vision IF amplifier with synchronous demodulator
- Automatic gain control (AGC) detector suitable for negative modulation
- AGC tuner
- Automatic frequency control (AFC) circuit with sample-and-hold
- Video preamplifier
- Sound IF amplifier and demodulator
- DC volume control or separate supply for starting the horizontal oscillator
- Audio preamplifier
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Generation of sandcastle pulse

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 7)	V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	I_7	75	125	165	mA
Start current (pin 11)	I_{11}	–	6.5	9.0	mA
Video					
IF sensitivity at 38.9 MHz (RMS value)		25	40	65	μV
IF gain control range	G_{8-9}	–	74	–	dB
Signal-to-noise ratio at 10 mV input signal	S/N	50	57	–	dB
AFC output voltage swing (peak-to-peak value)	$V_{18-6(p-p)}$	10.5	–	11.5	V
Sound					
AF output signal (RMS value)	$V_{12-6(rms)}$	400	600	800	mV
AM suppression at V_I = 50 mV	AMS	53	58	–	dB
Total harmonic distortion	THD	–	0.5	2	%

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117)

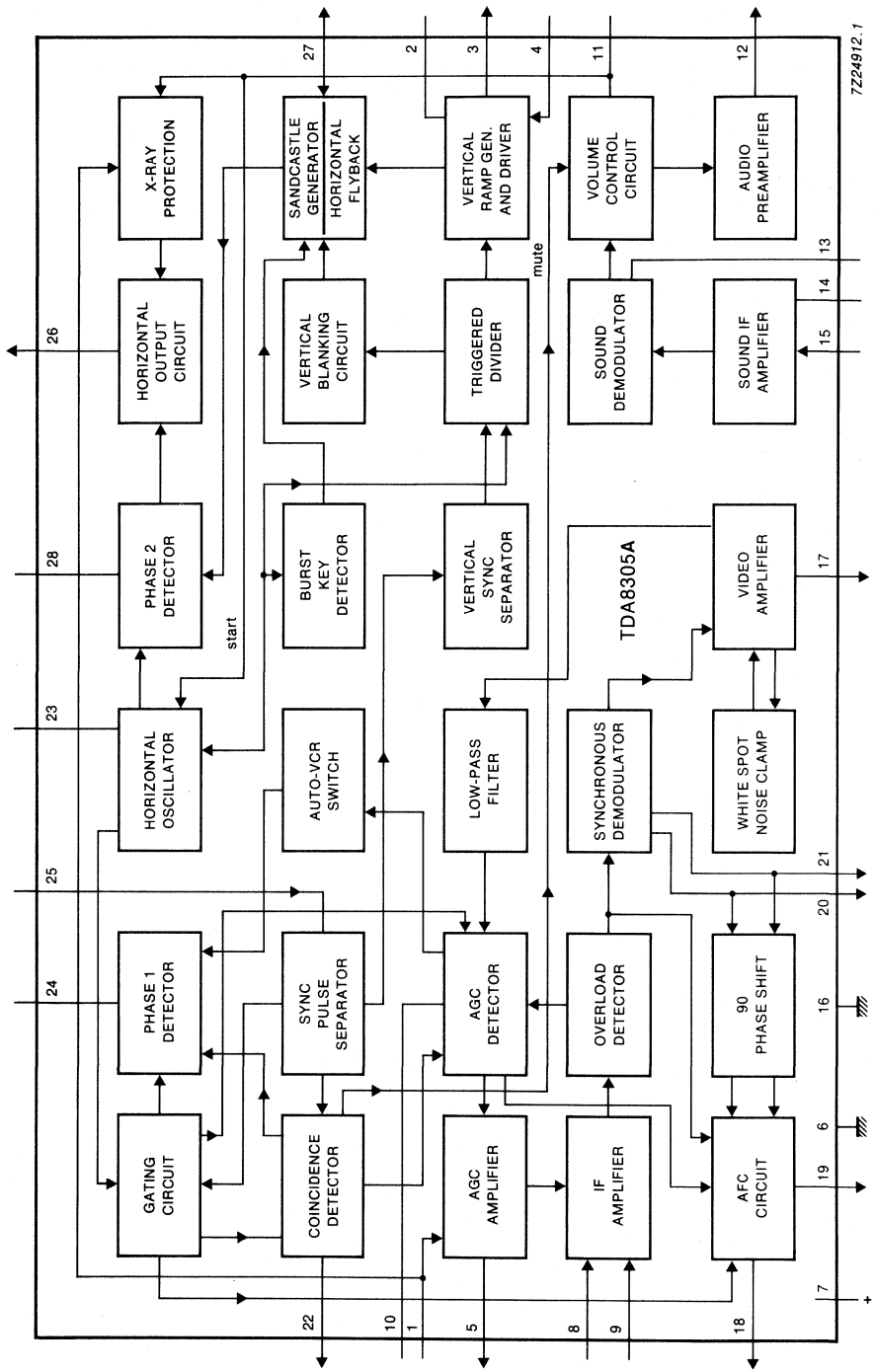


Fig.1 Block diagram.

QUICK REFERENCE DATA (continued)

parameter	symbol	min.	typ.	max.	unit
Sync pulse input amplitude	V_{25}	200	750	–	mV
Flyback input current	I_{27}	0.1	–	2	mA
Sandcastle output					
during burst key	V_{27}	8	–	–	V
during horizontal blanking	V_{27}	4	4.5	5	V
during vertical blanking	V_{27}	2.1	2.5	2.9	V
Coincidence detector voltage					
in synchronized condition	V_{22}	–	9.5	–	V
in no signal condition	V_{22}	–	1.5	–	V
Vertical feedback input					
DC voltage	V_{22}	2.9	3.3	3.7	V
AC voltage (peak-to-peak value)	$V_{22(p-p)}$	–	1.2	–	V

DEVELOPMENT DATA

PINNING

1. AGC take-over/X-ray protection
2. Vertical ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Main supply voltage
8. Vision IF input
9. Vision IF input
10. IF AGC
11. Volume control/start horizontal oscillator
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground (for some critical parts)
17. Video output
18. AFC output
19. AFC S/H, AFC switch
20. Vision demodulator tuned circuit
21. Vision demodulator tuned circuit
22. Coincidence detector
23. Horizontal oscillator
24. First phase detector
25. Sync separator
26. Horizontal drive
27. Sandcastle output/horizontal flyback input
28. Second phase detector

FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

The IF amplifier of the TDA8305A has three AC-coupled stages, each stage having a control range that exceeds 20 dB. AC-coupling means that the DC-feedback circuitry of the amplifier (present in the TDA4505) can be omitted, resulting in a saving of one pin. An additional advantage is the symmetry of the amplifier which results in a less critical application.

In the TDA8305A the regenerated carrier signal is limited by a logarithmic limiter circuit before it is passed on to a passive synchronous demodulator. The limiter has a very low differential phase shift which results in good differential gain and phase figures.

The TDA8305A's video amplifier has a higher bandwidth and better linearity compared with that of the TDA4505. A noise clamp is included in the video amplifier that limits the interference pulses to a level just below the top sync. This circuit is more effective than the noise inverter used in the TDA4505 and results in an improved picture stability, with respect to interference.

AFC circuit

In the TDA4505 and TDA8305A, the reference signal for the AFC circuit is obtained from the demodulator tuned circuit which means only one tuned circuit and adjustment are needed. The disadvantage with this method is that the frequency spectrum fed to the detector is determined by the SAW filter characteristic. This spectrum is asymmetrical with respect to the picture carrier so that the AFC output voltage is dependent on the video signal. This was the main problem found with the TDA4505's AFC circuit.

To remove this problem the TDA8305A is equipped with a sample-and-hold circuit which samples during the sync level of the signal. This means that only the carrier signal is available to the AFC and it will not be affected by the video information. The additional pin required for this circuit is provided by the pin that became available when the DC feedback circuit was removed from the IF amplifier (see previous section).

Weak input signals will cause the drive signal of the AFC to contain a lot of noise. This noise signal has an asymmetrical frequency spectrum that causes an offset in the AFC output voltage, this offset can be reduced by applying a notch to the demodulator circuit. The sample-and-hold circuit is followed by a high output impedance amplifier, therefore the AFC's control steepness is dependent on the load impedance.

AGC circuit

The TDA8305A's AGC detector differs from that of the TDA4505 in that it doesn't need the charge resistor but has an internal current source. Also the circuitry between the detector capacitor and the control stages has been changed to improve the signal-to-noise ratio of the video output signal (no dips in the S/N ratio depending on the input signal amplitude). The point of tuner take-over is preset by the voltage level at pin 1.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is by means of a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a volume control stage to the audio output amplifier. Volume control is obtained by connecting a potentiometer (10 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

Improvement of sound quality was one of the main reasons for redesigning the TDA4505. To obtain a better idea of the performance of the various circuits of the TDA4505 the following measurements were carried out:

- Weak signal performance when a TBA120 is driven with an intercarrier signal obtained from the vision IF circuit of the TDA4505 (the sound IF of the latter was not used)
- The same measurement for the sound IF circuit of the TDA4505 driven from another TDA4505 (again without using the sound IF circuit)
- The same measurement as in the first case but with the sound IF of the TDA4505 connected normally

From the results of these measurements it was established that the sound problem was caused by an interaction between vision IF and sound circuits. The improved sound quality of the TDA8305A as compared to the TDA4505 was achieved by:

- A very symmetrical vision-IF amplifier which is less sensitive to radiation from the sound IF amplifier
- A change to the internal ground and supply connections of the IC to reduce coupling between both circuits

DEVELOPMENT DATA

DC volume control/Horizontal oscillator start

Horizontal oscillator; the operation depending on the application. During switch-on if no current is supplied to pin 11 this pin will act as a volume control. When a current of 9.0 mA is supplied to pin 11 the volume control is set to a fixed output signal and the device will generate drive pulses for the horizontal deflection. The main supply can then be derived from the horizontal deflection circuit.

Horizontal synchronization

The video input signal (positive video) is connected to pin 25. The horizontal synchronization has two control loops that generate a sandcastle pulse. Using the oscillator sawtooth facilitates accurate timing of the burst key pulse. Therefore, the phase of this sawtooth must have a fixed relationship to the sync pulse, which is achieved by use of the second control loop.

The TDA8305A's horizontal synchronization circuit differs from that of the TDA4505 in that:

- The horizontal oscillator's retrace occurs during the horizontal retrace and not during the scan period. This means that with weak input signals no interference will be visible on the screen. It also prevents video crosstalk from disturbing the picture phase
- The reference signal for the horizontal phase detector is nearer to being symmetrical and is independent of the supply voltage and temperature. As a consequence the frequency shift of the horizontal oscillator during noise is reduced
- The current ratio of the phase detector for strong and weak signals is increased to obtain better behaviour during both VCR-playback and weak signal reception. The switching level is independent of supply voltage and temperature.

FUNCTIONAL DESCRIPTION (continued)

Horizontal phase detector

The circuit has the following operating conditions.

(a) Strong input signal, synchronized or non-synchronized.
(The strong/weak signal condition is obtained from the AGC circuit; the in-sync/out-of-sync from the coincidence detector). In this condition the time constant is optimum for VCR-playback i.e. fast time constant during the vertical retrace (to be able to correct VCR head-errors) and such, that during scan, fluctuations of the sync are corrected. The phase detector is not gated.

(b) Weak signal - synchronized
In this condition the time constant is increased compared to condition (a). Also the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by noise in the video signal.

(c) Weak signal - non-synchronized.
In this condition the time constant during scan and vertical retrace are the same as during scan in condition (a).

Vertical synchronization

The TDA8305A's vertical circuit differs from that of the TDA4505 in that it has:

- Improved interlacing - the timing of the internal pulses is now close to a 50/50 ratio. This timing is independent of supply voltage and temperature
- The temperature drift of the vertical amplitude has been reduced
- Reduction of noise in the vertical output signal so that modulation of the line distance will no longer be visible on large screen sets.
- When out-of-sync is detected by the horizontal circuit the divider is switched to 625 lines. This results in a stable amplitude when no input signal is available. In the TDA4505 the divider remains in the wide window during this condition which means interference may affect stability.

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of 10 μs with a separation of 22 μs. These types of vertical sync pulses are sometimes generated by video tapes with anti-copy guard.

Vertical divider system

The TDA8305A embodies a synchronized divider system for generating the vertical sawtooth at pin 2. The divider system has an internal frequency doubling circuit, which allows the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Use of the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 60 Hz to 50 Hz mode. When the trigger pulse comes before line 576 the 60 Hz mode is selected, otherwise the 50 Hz mode is selected.
The divider system operates with 2 different divider reset windows for maximum interference/ disturbance protection.
The windows are activated via an up/down counter.
The counter increases its counter value by 1 each time the separated vertical sync pulse is within the search window. When not within the search window this value is decreased by 1.
The operating modes of the divider system are as follows:

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found - not within the narrow window limits
- Up/down counter value of the divider system operating in the narrow window mode drops below count 10

Mode B

Narrow window (divider ratio between 522 to 528, 60 Hz; or 622 to 628, 50 Hz)

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 10 the divider system switches over to the large window mode.
The divider system also generates an anti-topflutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In Mode A the start is generated by reset of the divider.
In Mode B the anti-topflutter pulse starts at the beginning of the first equalizing pulse.
The anti-topflutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is by reset of the divider while the blanking pulse width is 34 (17 lines) for the 60 Hz mode and at count 42 (21 lines) for the 50 Hz mode.
The vertical blanking pulse at the sandcastle output (pin 27) is generated by adding the anti-topflutter pulse to the blanking pulse. Thus the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in Mode B. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

DEVELOPMENT DATA

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC coupled to this input as shown in Fig.11. It is possible to interrupt this connection and drive the sync separator from other sources such as:

- A teletext decoder in serial mode
- An external video signal via a peritelevision connector

When a teletext decoder is applied the IF amplifier and synchronization circuit are operating in the same phase which means that various connections between the two sections (i.e. AGC gating) can remain active. When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- AFC circuit is active
- Mute circuit not active - sound channel remains switched on
- Phase detector 1 has an optimal time constant for external video sources and is not gated.

X-ray protection

By forcing pin 1 below 1 V the horizontal output changes to a high resistance. The protection can be released by switching off the mains.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 7)	$V_P = V_{7-6}$	–	13.2	V
Total power dissipation	P_{tot}	–	2.3	W
Operating ambient temperature range	T_{amb}	−25	+65	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{7-6} = 12$ V; $T_{amb} = 25$ °C; carrier 38.9 MHz, negative modulation; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage range (pin 7)		V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	at no input	I_7	75	125	165	mA
Start current (pin 11)	note 1	I_{11}	–	6.5	9.0	mA
Start voltage horizontal oscillator		V_{11}	9.5	–	–	V
Start protection level	$I_{11} = 12$ mA	V_{11}	–	–	16.5	V
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38.9 MHz (RMS value)	note 2	V_{8-9}	25	40	60	μV
Input sensitivity at 45.75 MHz (RMS value)	notes 2, 27	V_{8-9}	25	40	60	μV
Differential input resistance	note 3	R_{8-9}	–	1300	–	Ω
Differential input capacitance	note 3	C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	77	–	dB
Maximum input signal		V_{8-9}	100	170	–	mV
Output signal expansion for 48 dB variation of input signal	note 4	ΔV_{17}	–	1	–	dB
Video amplifier	note 5					
Zero signal output level	note 6	V_{17}	–	5.4	–	V
Top sync level		V_{17}	2.3	2.5	2.7	V
Video output signal amplitude	note 7	V_{17}	2.3	2.65	3.0	V
White-spot threshold level			–	5.7	–	V
White-spot insertion level			–	3.8	–	V
Video output impedance		–	–	25	–	Ω
Internal bias current of output transistor (NPN emitter follower)		$I_{17(int)}$	1.4	1.8	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Maximum source current		I_{17}	10	–	–	mA
Bandwidth of demodulated output signal		B	5	7	–	MHz
Differential gain	note 8	G_{17}	–	4	8	%
Differential phase	note 8	φ	–	2	5	deg.
Video non-linearity	note 9	NL	–	2	5	%
Intermodulation	note 10					
f = 1.1 MHz (blue)			50	60	–	dB
f = 1.1 MHz (yellow)			50	60	–	dB
f = 3.3 MHz (blue)			55	65	–	dB
f = 3.3 MHz (yellow)			55	65	–	dB
Signal-to-noise ratio	note 11					
V_i = 10 mV		S/N	50	57	–	dB
end of gain control range		S/N	50	62	–	dB
Residual carrier signal		V_{17}	–	2	10	mV
Residual 2nd harmonic of carrier signal		V_{17}	–	2	10	mV
Tuner AGC						
Minimum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	–	–	0.2	mV
Maximum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	100	150	–	mV
Maximum tuner AGC output swing	V_5 = 3 V	$I_{5(max)}$	4	–	–	mA
Output saturation voltage	I_5 = 2 mA	$V_{5(sat)}$	–	–	300	mV
Leakage current (pin 5)		I_L	–	–	1	μA
Input signal variation complete tuner control		ΔV_i	0.5	2	4	dB
Minimum voltage tuner take-over		V_1	–	–	1	V
Voltage to switch on the X-ray protection	horizontal output high resistance	V_1	–	–	0.8	V
AFC circuit						
AFC sample-and-hold/switch						
AFC switch-off current		I_{19}	0.1	–	–	mA
Output current	V_{19} = 0 V	I_{19}	–	0.1	0.3	mA
Leakage current at pin 19		I_{LO}	–	–	2	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AFC circuit (continued)						
AFC output						
AFC output voltage swing	notes 18, 19	V_{18}	10.5	–	11.5	V
Available output current		I_{18}	0.2	–	–	mA
Control steepness			–	100	–	mV /kHz
AFC output voltage with AFC off		V_{18}	5.5	6	6.5	V
AFC output resistance		R_{18}	–	40	–	kΩ
Measured with an input signal amplitude = 150 μV (RMS value)						
Output voltage swing	note 27	V_{18}	–	11	–	V
Control steepness	note 27		–	80	–	mV /kHz
Output voltage shift with respect to V_i = 10 mV (RMS value)	note 27		–	–2	–	V
Sound circuit	note 12					
Input limiting voltage	$V_{o(max)}$ = –3 dB	V_{15}	–	400	800	μV
Input resistance		R_{15}	–	2.6	–	kΩ
Input capacitance		C_{15}	–	6	–	pF
AM suppression	note 13	AMS	53	58	–	dB
AF output signal (RMS value)	note 14	$V_{12(rms)}$	400	600	800	mV
AF output signal when pin 11 is used as a starting pin or connected to V_P (RMS value)	Δf = 50 kHz	$V_{12(rms)}$	500	900	1500	mV
AF output impedance		Z_{12}	–	25	100	Ω
Total harmonic distortion	note 15	THD	–	0.5	2	%
Ripple rejection	volume control 20 dB; f_k = 100 Hz	RR	–	35	–	dB
Output voltage when muted		V_{12}	–	2.5	–	V
Output level shift due to muting	volume control –20 dB	V_{12}	–	–	0.5	V
Signal-to-noise ratio	note 16	S/N	–	47	–	dB
Voltage with pin 11 disconnected		V_{11}	–	6.0	–	V
Current with pin 11 short circuited to ground		I_{11}	–	1	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature dependance of the output signal amplitude	T_{amb} = 20 °C to 65 °C; −30 dB volume control and voltage of pin 11 fixed; note 27	V_{12}	–	2.5	–	dB
Volume control	note 17; see Fig.8					
External control resistor	note 17	R_{11}	–	4.7	–	kΩ
Suppression output signal during mute condition		OSS	60	66	–	dB
Horizontal synchronization circuit	see Fig.9					
Sync separator						
Required sync pulse amplitude	note 20	V_{25}	200	750	–	mV
Input current pin 25	$V_{25} > 5$ V	I_{25}	–	8	–	μA
	$V_{25} = 0$ V	I_{25}	–	−10	–	mA
First control loop						
Holding range PLL		$\pm\Delta f$	–	1500	2000	Hz
Catching range PLL		$\pm\Delta f$	600	1500	–	Hz
Control sensitivity to oscillator	note 21			see Fig.10		
IF input signal at which the time constant is switched (RMS value)	strong to weak	V_{8-9}	–	2.2	–	mV
Second control loop						
Control sensitivity	note 22	$\Delta t_d/\Delta t_o$	–	100	–	–
Control range		t_d	–	25	–	μs
Controlled edge				positive		
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	±2	–	μs
Horizontal oscillator (pin 23)						
Free running frequency	R = 34.3 kΩ; C = 2.7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δf	–	–	4	%
Frequency variation	ΔV_P = 9.5 to 13.2 V	Δf_{fr}	–	–	2	%
Frequency variation with temperature	note 27	TC	–	−1.6	–	Hz/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal oscillator (pin 23) (continued)						
Maximum frequency deviation at start of horizontal output		Δf_{fr}	–	–	10	%
Frequency variation when only noise is received	note 27	Δf_{fr}	–	–	500	Hz
Horizontal output						
Output limiting voltage		V_{26}	–	–	16.5	V
Output voltage LOW	I_{sink} = 10 mA	V_{26}	–	0.2	0.5	V
Maximum sink current		I_{26}	10	–	–	mA
Duty cycle output signal			–	46	–	%
Rise time of output pulse		t_r	–	260	–	ns
Fall time of output pulse		t_f	–	100	–	ns
Flyback input and sandcastle output	note 23					
Input current required during flyback pulse		I_{27}	0.1	–	2	mA
Output voltage:						
during burst key pulse		V_{27}	8	–	–	V
during horizontal blanking		V_{27}	4	4.4	5	V
during vertical blanking		V_{27}	2.1	2.5	2.9	V
Pulse width:						
burst key pulse	60 Hz	t_W	2.9	3.3	3.7	µs
burst key pulse	50 Hz	t_W	3.2	3.6	4.0	µs
horizontal blanking pulse			flyback pulse width			
Vertical blanking pulse:						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at the video output and the burst key pulse						
trailing edge	60 Hz		–	–	9.3	µs
rising edge			4.7	5.4	6.1	µs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Coincidence detector						
Voltage for:						
synchronized condition		V_{22}	–	9.8	–	V
no signal condition		V_{22}	–	1.5	–	V
Switching level to switch the phase detector from fast to slow		V_{22}	6.2	6.7	7.2	V
Hysteresis slow to fast		V_{22}	–	0.6	–	V
Switching level to activate the mute function (transmitter identification)		V_{22}	2.5	2.8	3.1	V
Hysteresis mute function		V_{22}	–	2	–	V
Delay time of mute release after transmitter insertion					300	μs
Allowable load on pin 22					10	μA
External video mode		V_{22}	–	–	0.7	V
Current at pin 22	V_{22} = 0 V	I_{22}	–	–	0.8	mA
Vertical circuit	note 25					
Vertical ramp generator						
Input current during scan		I_2	–	–	2	μA
Discharge current during retrace		I_2	–	0.8	–	mA
Sawtooth amplitude (peak-to-peak value)		$V_{2(p-p)}$	–	1.9	–	V
Interlace timing of the internal pulses			30	32	34	μs
Vertical output						
Available output current	V_3 = 4 V	I_3	–	–	3	mA
Maximum output voltage	I_3 = 0.1 mA	V_3	4.4	5	–	V
Vertical feedback input						
Input voltage						
DC component		V_4	2.9	3.3	3.7	V
AC component (peak-to-peak value)		$V_{4(p-p)}$	–	1	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	3	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Temperature dependence of the amplitude	T_{amb} = 20 °C to 65 °C		–	–	2	%

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Vertical circuit (continued)						
Vertical guard	note 26					
Active switching level at a deviation with respect to the DC feedback level:	V_{27} = 2.5 V					
guard level LOW		ΔV_4	–	2.1	–	V
guard level HIGH		ΔV_4	–	2	–	V

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 9.0 mA is supplied to this pin, it is used to start the horizontal oscillator.
   The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The input impedance has been chosen such that a SAW-filter can be applied.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS value) top sync input signal.
6. So-called projected zero point; i.e. with switched demodulator.
7. White 10% of the top sync amplitude.
8. Measured according to the test line illustrated by Fig.2:
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig.3.
   The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are illustrated by Fig.4. The figures are measured at an input signal of 10 mV (RMS value).
11. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20 \log \frac{V_{\text{out black-to-white}}}{V_{n(\text{rms}) \text{ at B = 5 MHz}}}$$

12. The sound circuit is measured (unless otherwise specified) with an input signal of V_{15} of 50 mV (RMS value), a carrier frequency of 5.5 MHz at a Δf of 27.5 kHz and an AF frequency of 1 kHz. The QL of the demodulator tuned circuit is 16 and the volume control is connected to the supply. The reference circuit must be tuned in such a way that the output is symmetrical clipping at maximum volume.
13. The test set-up is illustrated by Fig.6. The AM rejection curve (typical) is illustrated by Fig.7.
14. The output signal is measured at aΔf = 7.5 kHz and maximum volume control.
15. The demodulator tuned circuit must be tuned at minimum distortion.
16. Weighted noise, measured according to; CCIR 468.
17. See also note 1. The volume can be controlled by using a potentiometer connected to ground (value 10 kΩ) or by means of a variable direct voltage. In the latter case the relatively low input impedance (pin 11) must be taken into account.

18. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90 degree phase shift network. The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is followed by a sample-and-hold circuit which samples during the sync level. As a result the AFC output voltage contains no video information. The specified control steepness is without using an external load resistor. The control steepness decreases when the AFC output is loaded with two resistors between the voltage supply and ground.
19. At very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built in to the demodulator tuned circuit. The characteristics given for weak input signals are measured without a notch circuit, with a SAW filter connected in front of the IC (input signal such that the input signal of the IC is 150 μV (RMS value).
20. The minimum value is obtained with a 1.8 kΩ series resistor connected between pin 17 and pin 25. The slicing level can be varied by changing the value of this resistor (a higher resistance results in a larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
21. Frequency control is obtained by supplying a correction current to the oscillator RC-network. This is achieved via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by:

    - short-circuit the sync separator bias network (pin 25) to the voltage supply.

    To avoid the necessity of a VCR switch, the time constant of the phase detector at strong input signals is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that VCR head errors are compensated for at the beginning of the scan. During weak signal conditions (information derived from the AGC circuit) the time constant is increased to obtain a good noise immunity.
22. This figure is valid for an external load impedance of 82 kΩ connected between pin 28 and the shift adjustment potentiometer.
23. The horizontal flyback input and the sandcastle output have been combined on pin 27. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
24. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
25. The vertical scan is synchronized by means of a divider system, therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
26. To avoid screenburn due to a collapse of the vertical deflection, a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
27. These figures are based on sampled tests.

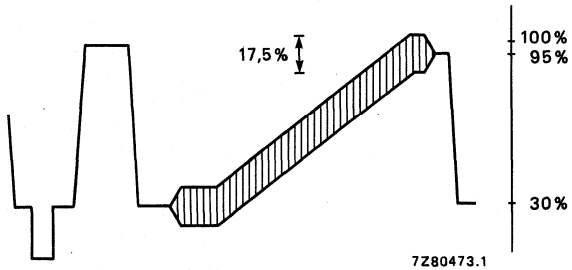


Fig.2 Video output signal.

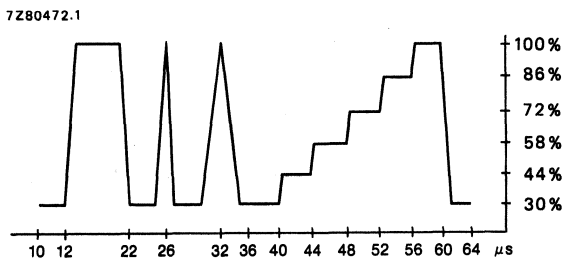
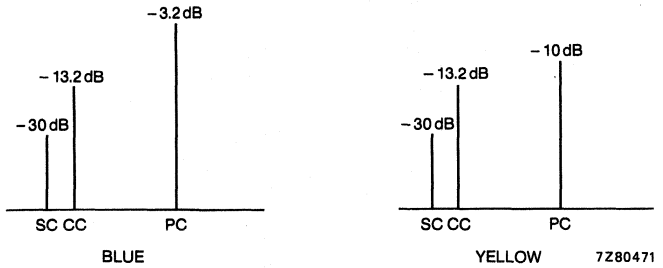
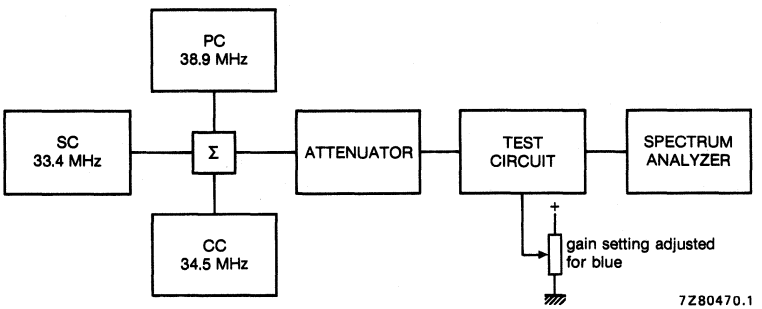


Fig.3 European Broadcasting Union (EBU) test signal waveform (line 330).



Where

SC = sound carrier
CC = chrominance carrier
PC = picture carrier
All values are with respect to the top sync level



Where

Value at 1.1 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$

Value at 3.3 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$

Fig.4 Test set-up intermodulation.

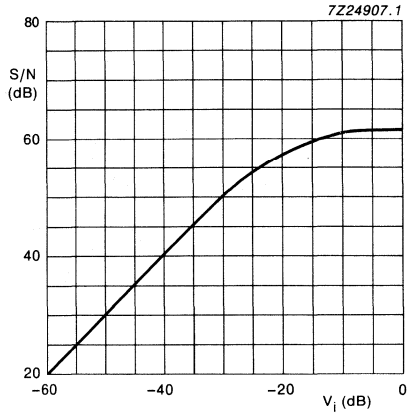


Fig.5 Signal-to-noise ratio as a function of input voltage; 0 dB = 100 mV.

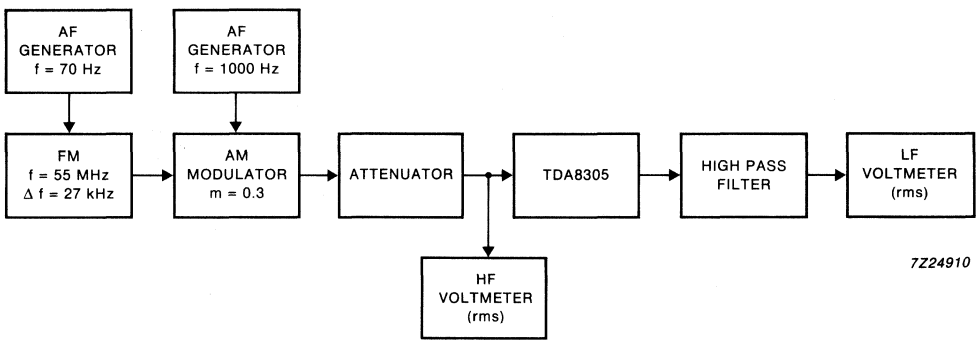


Fig.6 Test set-up AM suppression.

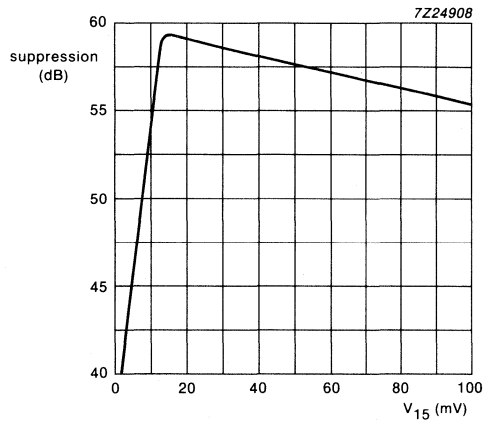


Fig.7 AM suppression.

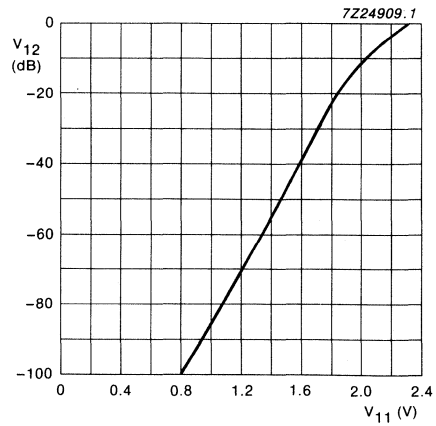
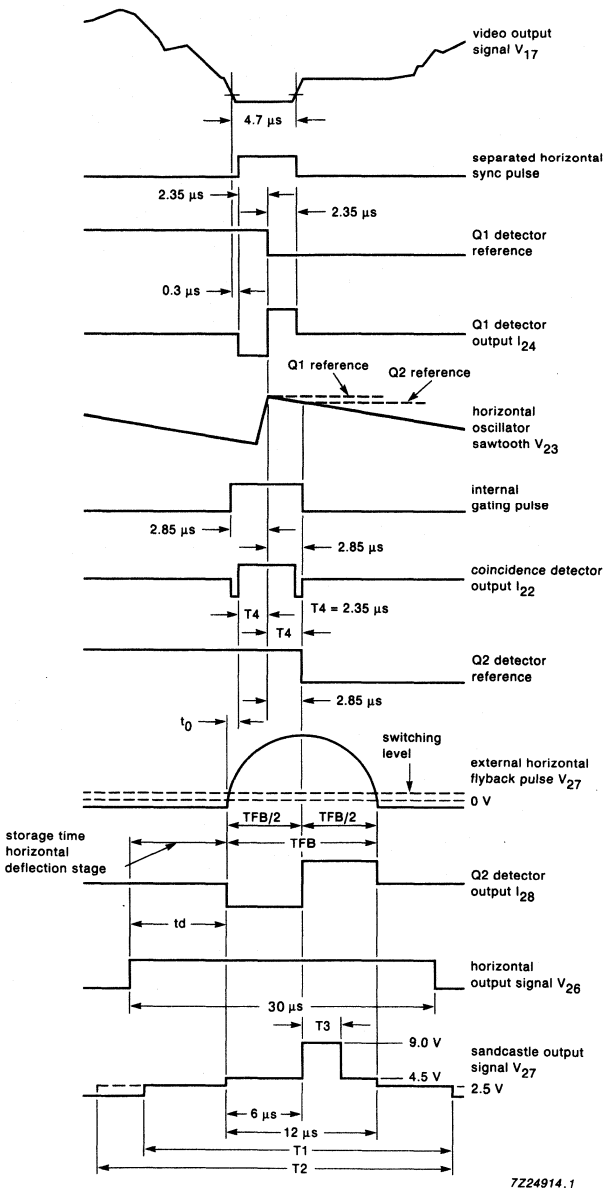


Fig.8 Volume control characteristics.

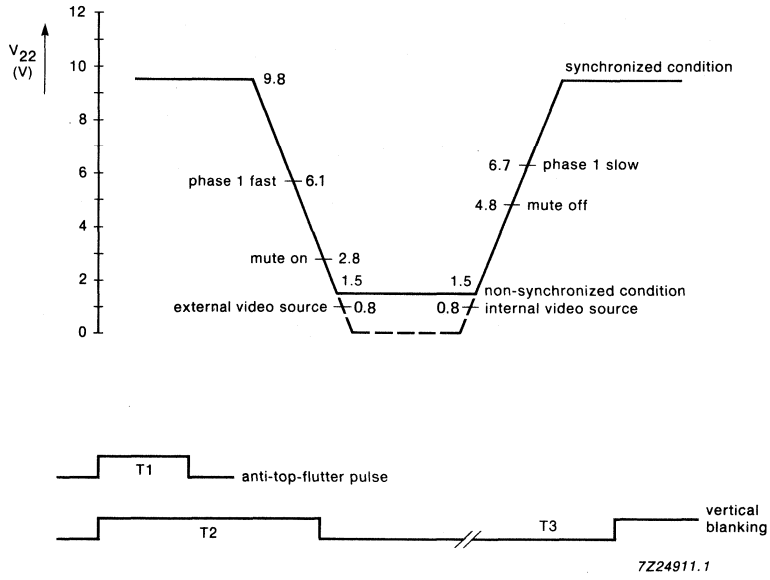
DEVELOPMENT DATA



	50 Hz	60 Hz
T1 – search window –	42P	34P
T2 – narrow window –	50P	42P
T3	3.6 µs	3.3 µs

$$P = \frac{1}{2F_H}$$

Fig.9 Timing diagram.



condition	control sensitivity horizontal oscillator		vertical sync separation pulse after
	T2 – T1	T3 = scan	
$V_{22} > 6.7$ V			
strong signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
weak signal	1.3 kHz/μs	1.3 kHz/μs	16 μs
$1 < V_{22} < 5.7$ V			
strong signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
weak signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
$V_{22} < 0.7$ V	11.3 kHz/μs	7.6 kHz/μs	16 μs

Fig.10 Switching levels coincidence detector.

APPLICATION INFORMATION

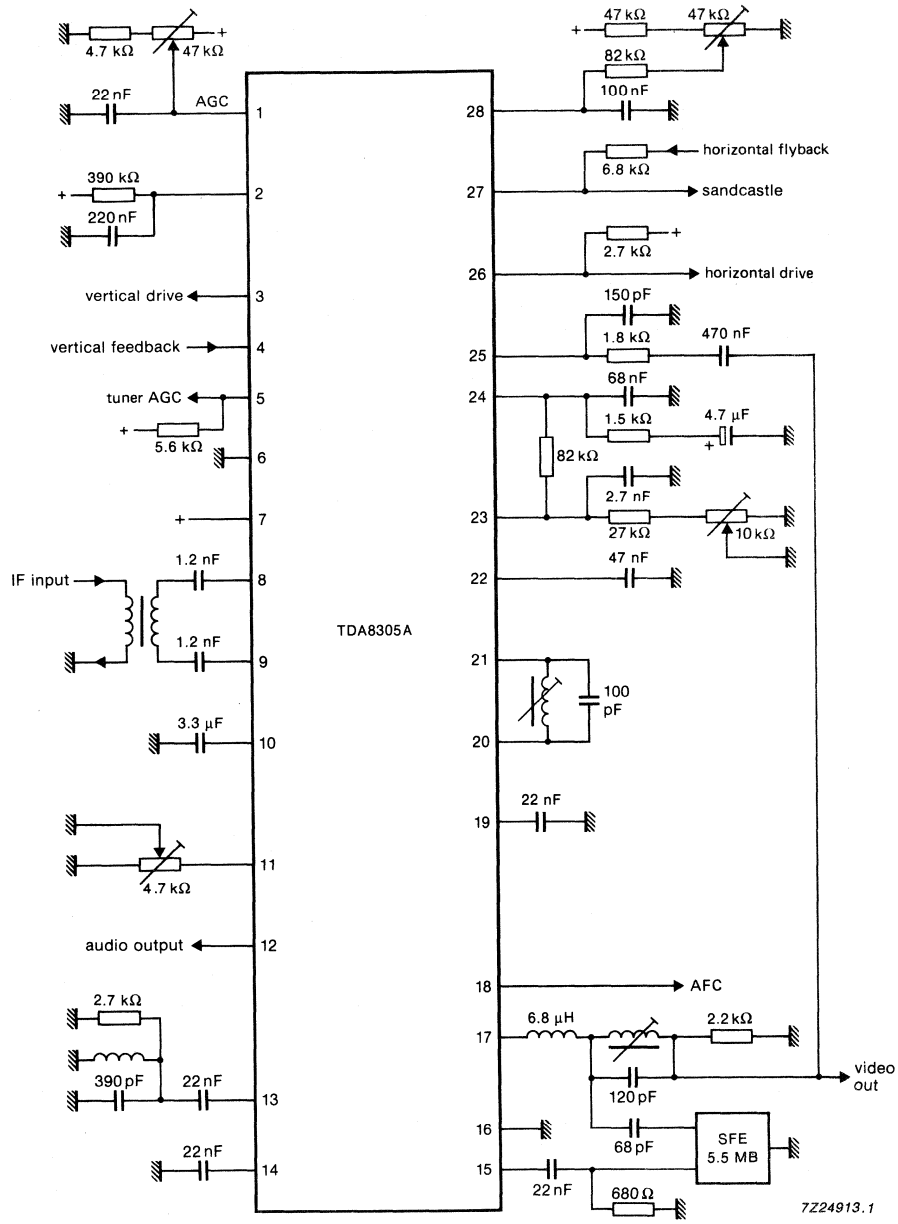


Fig.11 Application diagram.

DEVELOPMENT DATA

TELEVISION IF AMPLIFIER AND DEMODULATOR

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1-16(rms)}$	20	40	80	μV
IF gain control range		G_v	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5-13(p-p)}$	–	10	–	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38).
TDA8340Q; TDA8341Q: 16-lead QIL; plastic (SOT58).

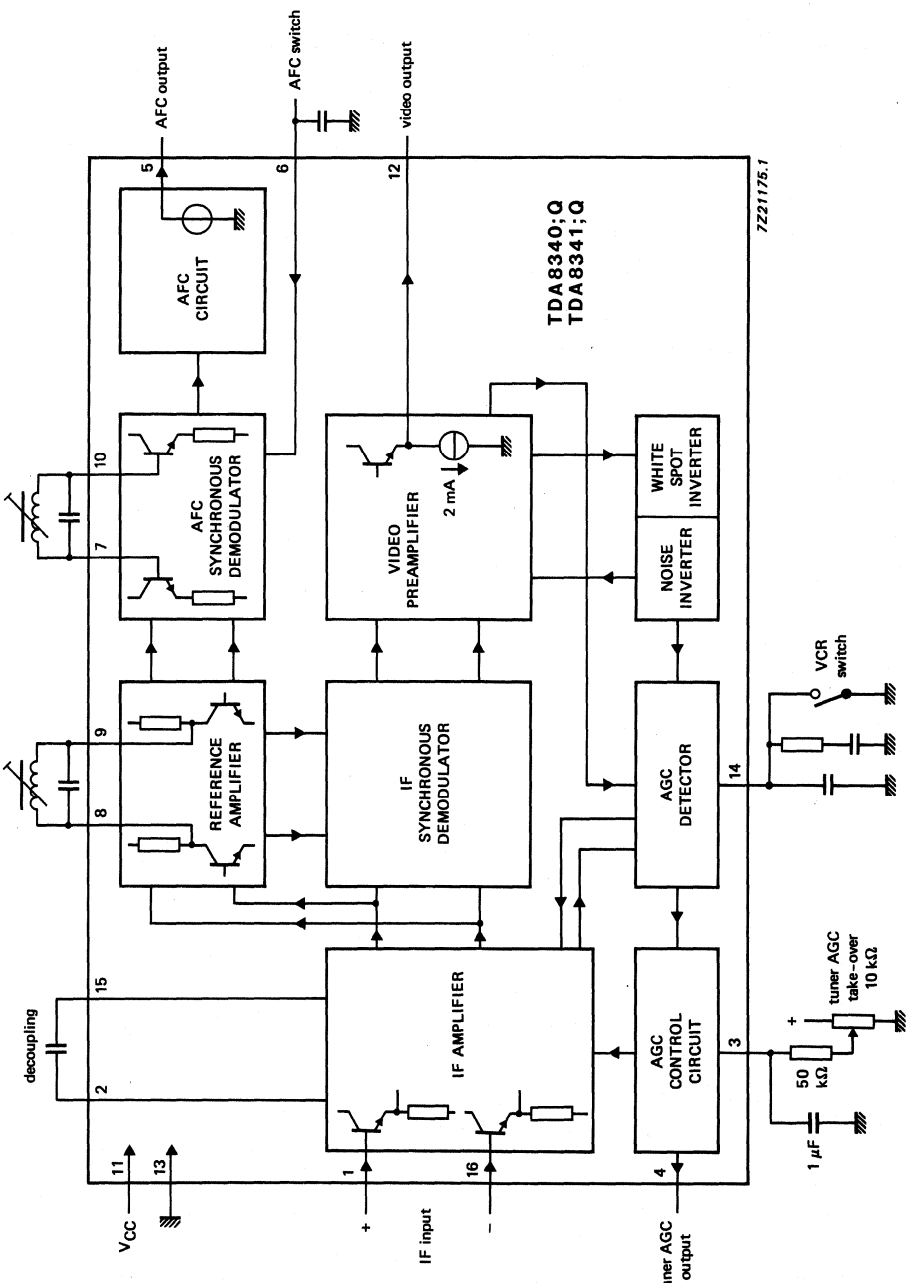


Fig. 1 Block diagram.

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier $\pi/2$ rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

DEVELOPMENT DATA

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwith of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 μH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC dectector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No 'hang-up' occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

FUNCTIONAL DESCRIPTION (continued)

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 11)	$V_{CC} = V_{11-13}$	9,4	13,2	V
IF AGC voltage/VCR switch	V_{14-13}	–	13,2	V
Tuner AGC voltage	V_{4-13}	–	12	V
AFC switch voltage	V_{6-13}	–	13,2	V
Maximum voltage level with VCR switch active	V_{12-13}	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature	T_{amb}	−25	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

Measured in circuit of Fig. 3; V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	μV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point (note 3)	R_{3-11} = 39 kΩ	V_{1-16}	–	–	3	mV
	R_{3-13} = 39 kΩ	V_{1-16}	70	–	–	mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; I_4 = 1 to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	I_4 = 7 mA	V_{4-13}	–	200	300	mV
Leakage current	V_4 = 12 V	I_4	–	–	1	μA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwith of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Video output (continued)						
Residual 2nd harmonic of carrier signal (r.m.s. value)	note 8	$V_{12\text{-}13(rms}$	–	2	10	mV
Variation of video voltage for ΔV_{CC} = 1 V		$\frac{\Delta V_{12\text{-}13(p\text{-}p)}}{\Delta V_{11\text{-}13}}$	0,1	0,2	0,3	
Intermodulation	notes 8 and 9;					
	1,1 MHz, blue	α	–	–65	–60	dB
	1,1 MHz, yellow	α	–	–60	–56	dB
	3,3 MHz	α	–	–	–68	dB
Signal-to-noise ratio	note 10;					
	V_i = 10 mV	S/(S+N)	50	58	–	dB
	max. gain	S/(S+N)	54	61	–	dB
Spot inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	6,3	6,8	7,3	V
Insertion level		$V_{12\text{-}13}$	4,2	4,5	4,8	V
Noise inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	1,6	1,8	2,0	V
Insertion level		$V_{12\text{-}13}$	3,5	3,8	4,1	V
VCR switch						
Level below which video output switches off		$V_{14\text{-}13}$	1,8	2,2	2,6	V
Switch current	$V_{12\text{-}13}$ = 0,7 V	$-I_{14}$	40	60	100	μA
AFC circuit (note 12)						
Output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V
Change of frequency for an AFC output voltage swing of 10 V		Δf	–	60	120	kHz
AFC output voltage	at f = 38,9 MHz	$V_{5\text{-}13}$	–	6	–	V
	no input signal	$V_{5\text{-}13}$	2	6	10	V
	during AFC off	$V_{5\text{-}13}$	5	6	7	V
AFC output resistance		$R_{5\text{-}13}$	–	500	–	Ω
AFC switch: level below which AFC output switches off		$V_{6\text{-}13}$	1,4	2,0	2,8	V
AFC switch current	during AFC on	I_6	–	200	500	μA
Max. AFC switch current	during AFC off;					
	$V_{6\text{-}13}$ = 0 V	I_6	–	–	5	mA

Notes to the characteristics

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Tuner AGC starting point is defined as 'level of input signal when tuner AGC current = 1 mA'.
4. Measured with pin 3 connected via 39 kΩ resistor to V_{CC} (pin 11), with an r.m.s. voltage of 10 mV top sync input signal and with pin 12 not loaded.
5. At the 'projected zero point', e.g. with switched demodulator.
6. Measured in the circuit of Fig. 7:

   the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level;

   the differential phase is defined as 'the difference (in degrees) between the largest and smallest phase angles'.
7. Measured according to the test line shown in Fig. 9:

   the non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step;

   the mean step is (white level — black level) divided by the number of steps.
8. Measured up to 45 dB gain control.
9. Test set-up and input conditions for intermodulation measurements as in Figs 6 and 7.
10. Measured with a 75 Ω source:

$$S/(S+N) = 20 \log \frac{V_{\text{out black to white}}}{V_{n(\text{rms}) \text{ at } B = 5 \text{ MHz}}}.$$

11. Video output waveform showing white spot and noise inverter threshold levels.
12. Measured with input signal $V_{1\text{-}16}$ = 10 mV and with no load at AFC output.

DEVELOPMENT DATA

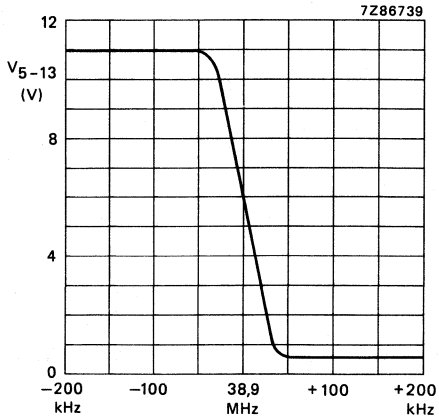


Fig. 2 AFC output voltage as a function of frequency.

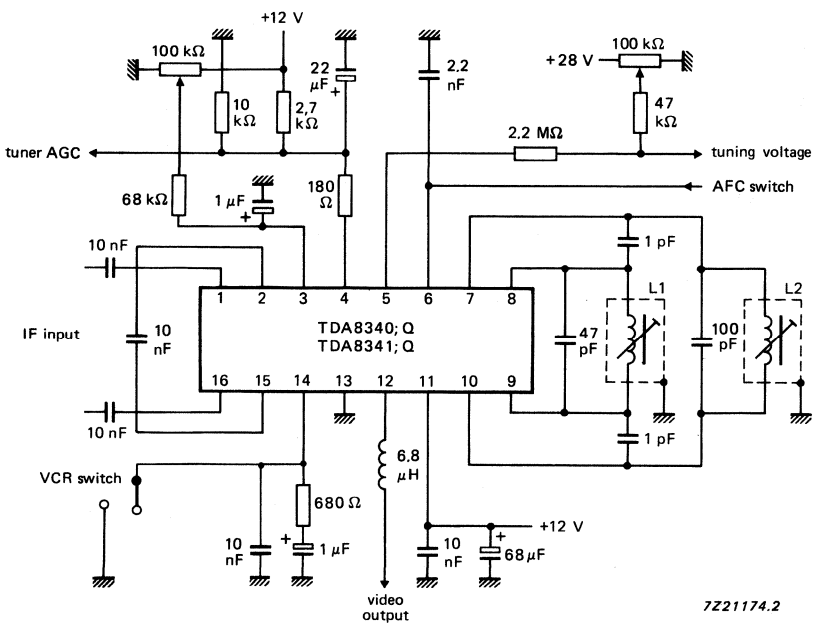


Fig. 3 Typical application circuit diagram;
Q of L1 and L2 = 80; f_o = 38,9 MHz.

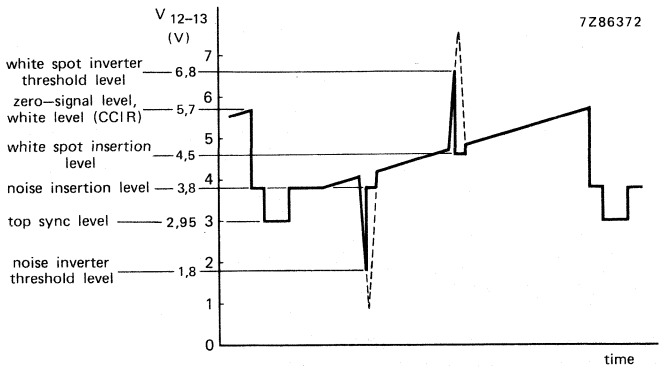


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

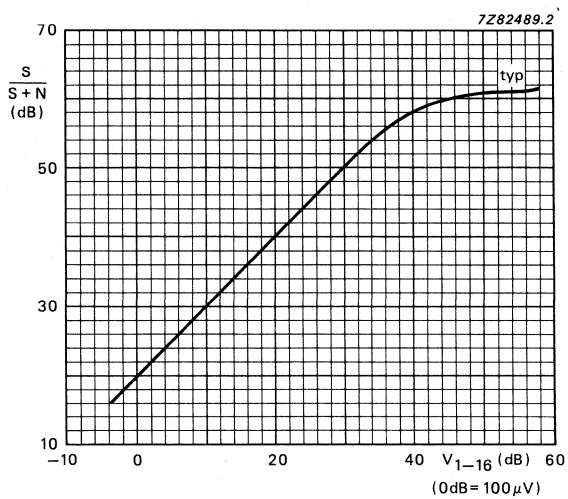
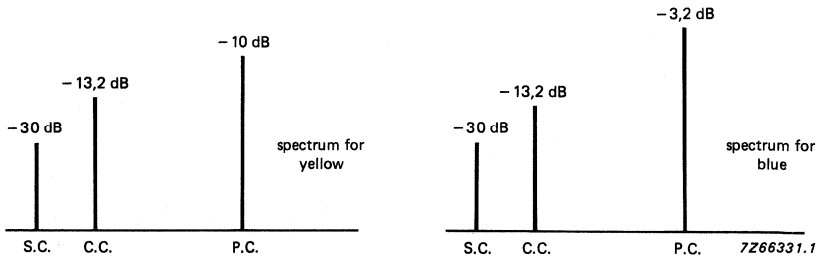


Fig. 5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

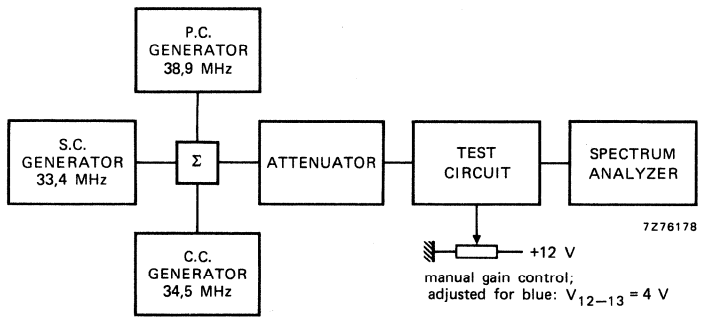


Fig. 7 Test set-up for intermodulation measurements.

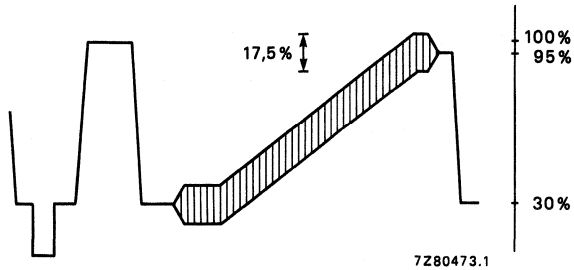


Fig. 8 Video output signal.

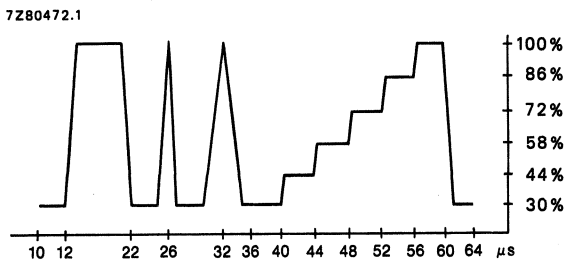


Fig. 9 E.B.U. test signal waveform (line 330).

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA8349A

Multistandard IF Amplifier and demodulator

GENERAL DESCRIPTION

The TDA8349A is a multistandard IF amplifier and demodulator with AGC and AFC functions for television receivers. The device has a video recognition circuit and a video switch for internal or external video for full SCART applications.

FEATURES

- Full range gain-controlled wide-band IF amplifier up to 60 MHz
- Wide-band video amplifier with good linearity and a class AB output stage to ensure a very low output impedance
- Supply independent video output level
- Small second harmonic IF output
- AGC circuit which operates on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC) with reduced sensitivity for high sound carriers
- AFC circuit with an internal 90° phase shift circuit, a sample-and-hold circuit for negatively modulated signals to reduce video dependent AFC information and an analog or digital output
- Video recognition possibility based on horizontal pulse duty cycles
- Video switch for selection of internal or external video signals
- Wide supply voltage range and ripple rejection
- Requires few external components
- Tuner AGC output for npn and pnp tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current (pin 14)	V_i = 10 mV	40	55	65	mA
$V_{1-2(RMS)}$	IF input sensitivity (RMS value)		-	50	80	µV
G_v	IF gain control range		66	72	-	dB
$V_{11-17(p-p)}$	video output voltage (peak-to-peak value)		1.7	1.9	2.1	V
S/N	signal-to-noise ratio	V_i = 10 mV	54	61	-	dB
$V_{8-17(p-p)}$	AFC output voltage swing (peak-to-peak value)		10	-	11	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8349A	20	DIL	plastic	SOT146

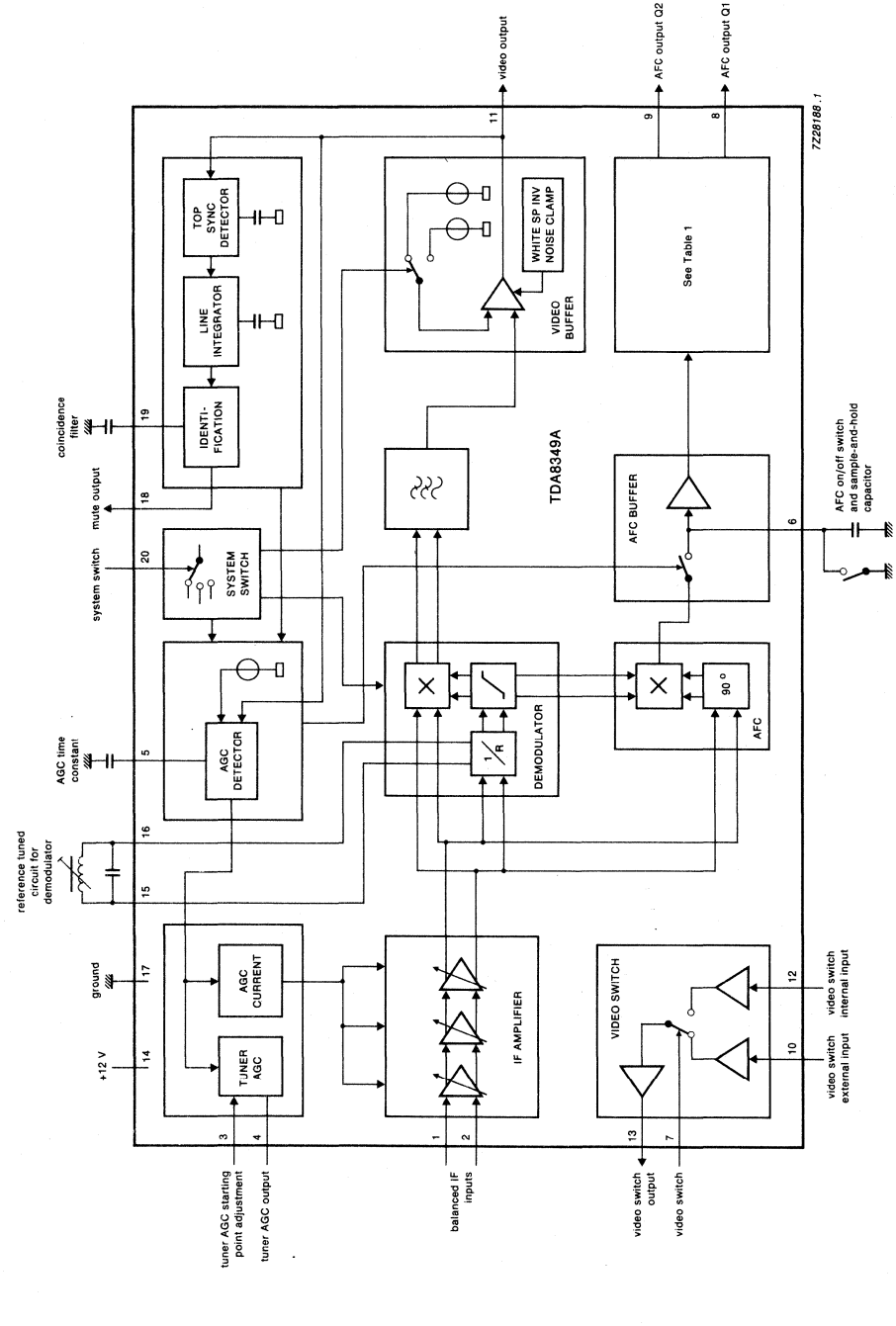


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1,2	balanced IF inputs
3	tuner AGC starting point adjustment
4	tuner AGC output
5	AGC time constant
6	AFC on/off switch and sample-and-hold capacitor
7	video switch
8	AFC output Q1
9	AFC output Q2
10	video switch external input
11	video output
12	video switch internal input
13	video switch output
14	positive supply voltage
15,16	reference tuned circuit for demodulator
17	ground
18	mute output
19	coincidence filter
20	system switch

FUNCTIONAL DESCRIPTION

General

The IC consists of the following parts as illustrated in Fig.1:

- Gain controlled video IF amplifier
- Quasi-synchronous demodulator
- Video amplifier/buffer with white spot clamp/inverter and noise clamp
- AGC circuit which operates either on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC)
- AFC circuit with sample-and-hold circuit for negatively modulated signals, on/off switch and a digital or analog output (switchable)
- Circuit for switching between positive and negative modulation
- Video recognition circuit for sound muting and tuning indication
- Video switch which facilitates selection between two different video signals, with different gain settings

IF amplifier

The IF amplifier consists of three AC coupled differential gain stages with adjustable feedback in the emitter. The AC coupling allows simple biasing, cascades can be used and no DC feedback is required. This provides a control range above 70 dB with good linearity. The minimum input signal to obtain the nominal output amplitude is 50 μV RMS.

Demodulator

The demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and a tuned circuit for selectivity. The regenerated carrier signal is limited by a clamping circuit before it is fed to the demodulator. Switching between positive and negative modulation is achieved by the system switch which provides currents to the demodulator in a positive or negative direction.

Video amplifier

The video amplifier based on the feedback principle improves the linearity of the video output buffer. It has an internal bandgap reference to ensure a stable video output at different supply voltages and temperatures. This bandgap also reduces the supply ripple on the video output to values less than −30 dB. The video amplifier has a typical bandwidth of 10 MHz which allows application for all new video standards with bandwidths of up to 10 to 12 MHz. The video output signal has an amplitude of 2 V (p-p).

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers. A switchable DC shift for positively modulated IF signals ensures correct signal handling. This switching is obtained via pin 20, which is the same pin used for switching the demodulation polarity in the demodulator.
The circuit also has a noise clamp which prevents the video output becoming less than ±400 mV below the top sync level at noise peaks.
The output buffer of the video amplifier consists of a class A/B circuit which can handle large source as well as large sink currents. This makes the circuit more flexible in several applications with one or more ceramic filters connected to this output buffer.

AGC control circuit

This converts the AGC detector voltage (pin 5) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted by a voltage between 3 and 5 V for pnp tuners and between 7 and 9 V for npn tuners via pin 3.

AGC circuit

A new AGC system has been designed for the AGC. It will be a top sync-detector for negatively modulated signals and a top white level AGC for positively modulated signals.
For optimal flexibility reasons the load and unload currents of the AGC are chosen such that both, a relatively fast set, as well as a set with a low tilt are possible for positive (L) and negative (B/G) modulated signals. For this reason a tilt ratio between positive (L) and negative (B/G) of approximately 3:1 has been chosen. This means that in a fast set the choice of a typical tilt for negatively modulated signals of 2% will obtain a typical tilt for positively modulated signals (L) of 6%. For a digital set which requires a small tilt the choice of tilt can be a factor of 5 or 10 smaller by increasing the AGC capacitor.

The chosen AGC currents:

MODE	UNLOAD CURRENT	LOAD CURRENT	TILT AT 2.2 µF
B/G	50 µA	1.5 mA	typ. 0.5% (line tilt)
L	500 nA*	1.5 mA	typ. 1.5% (field tilt)
MAC(positive)	200 nA	1.5 mA	typ. 1.2% (frame tilt)
MAC(negative)	500 nA	1.5 mA	typ. 1.5% (field tilt)

Switching between the first three modes can be achieved by the system switch. This is a 3-level switch which when grounded selects B/G; open or 5 V selects L, and with pin 20 connected to V_{CC} selects positively modulated MAC. The IC operates in a fourth mode if the identification capacitor at pin 19 is connected to V_{CC}, it can be used for negatively modulated MAC.
During channel switching a situation can occur that requires the AGC to increase the gain more than for example 50 dB. If this increase of gain has to be done for a positively modulated (L) signal, it will be achieved by the 500 nA load current and is therefore extremely slow. Because the identification information can be used to indicate that the signal is too small, in this event the identification circuit will mute, it is possible to increase the positive unload current to the same value as that used for negatively modulated signals. This switching is fully automatic and cannot be switched off.

AFC circuit

The AFC circuit consists of a demodulator stage which is fed with signals 90°out of phase. A very accurate internally realized 90° phase shift circuit makes it possible to use the demodulator IF regenerator tuned circuit for tuning the AFC circuit. To prevent video ripple on the AFC output voltage a sample-and-hold circuit is used for negatively modulated signals. The output signal of the demodulator is sampled during

* As long as no signal has been identified by the identification detector the unload current will be 50 µA.

sync level of the video signal and will be stored with the aid of an external capacitor. This sample-and-hold circuit is not used in the L mode, but it will function as a low-pass filter in this mode and therefore also reduces the video dependency of the AFC. A gain stage amplifies the voltage swing by 5 times. The output of the AFC circuit will be an inverse analog output on pin 8 when pin 9 is connected to a voltage above 8 V. If pin 9 is connected to a voltage above 10 V the output will be a normal analog output. Normally pins 8 and 9 together provide digital AFC information.

Video recognition circuit

For full scart functions it is necessary to implement a second mute function for non-video signals in the whole television concept. This is realized in this IF-IC. With an internal sync separator and an internal integrator it is possible to achieve a very sensitive identification circuit, which measures the mean frequency of the input signal. This is normally approximately 16 kHz. The integrator capacitor will be loaded during the whole line time and unloaded during the sync pulse. The maximum voltage at this internal capacitor is a value for the main frequency of the video signal. By changing the value of an external capacitor it is possible to influence the speed and sensitivity of the recognition circuit. It is possible to gain sensitivity performance at disturbed signals by increasing the value of the external capacitor, however this will reduce the speed of the identification circuit.

Video switch circuit

The video switch also provides application for full SCART functions. The circuit has two inputs, one output and a control pin. The switch selects either internal or external video signals. A x 2 gain stage for the external input provides an equal output level for internal or external video from the SCART. The crosstalk of the unwanted signal is better than –50 dB and the total signal handling meets all the requirements for SCART specifications.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)	–0.5	13.2	V
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+ 75	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; carrier frequency 38.9 MHz; negative modulation; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
supply						
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current	V_i = 10 mV	40	55	65	mA
IF amplifier (note 1)						
V_{1-2}	input sensitivity	note 2	-	50	80	μV
R_{1-2}	differential input resistance	note 3	-	2	-	kΩ
C_{1-2}	differential input capacitance	note 3	-	2	-	pF
ΔG_{1-2}	gain control range		66	72	-	dB
ΔV_{11}	output signal for 50 dB input signal variation	note 4	-	0.5	-	dB
V_{1-2}	maximum input signal		100	-	-	mV
f_{1-2}	maximum operating frequency		60	-	-	MHz
Video output (note 5)						
	zero signal output level	note 6				
V_{11}	negative modulation		-	4.75	-	V
V_{11}	positive modulation		-	2.65	-	V
V_{11}	top sync level (top sync AGC)	note 7	-	2.7	-	V
V_{11}	white level (white level AGC)	note 8	-	4.6	-	V
$V_{11(p-p)}$	amplitude of video output signal (peak-to-peak value)		1.7	1.9	2.1	V
V_{11}	amplitude difference (positive/negative)		-	0	10	%
V_{11}	video output voltage variation	ΔV_P = 1 V	-	–30	-	dB
V_{11}	white spot threshold level	see Fig.3	-	5.6	-	V
V_{11}	white spot insertion level	see Fig.3	-	3.8	-	V
V_{11}	noise clamping level	see Fig.3	-	2.3	-	V
Z_{11}	output impedance		-	-	10	Ω
I_{11}	maximum sink current		5	-	10	mA
I_{11}	maximum source current		5	-	10	mA
B_{11}	bandwidth of demodulated output signal		7.5	10.0	-	MHz
G_d	differential gain	note 9	-	2	-	%
φ_d	differential phase	note 9	-	7	-	deg
Y_{nl}	luminance non-linearity	note 10	-	2	5	%
	intermodulation	see Figs 6 and 7				
α	1.1 MHz blue		-	–66	-	dB
α	1.1 MHz yellow		-	–60	-	dB
α	3.3 MHz blue		-	–60	-	dB
α	3.3 MHz yellow		-	–60	-	dB
	signal-to-noise ratio	note 11				
S/N		V_i = 10 mV	54	61	-	dB
S/N		minimum gain	60	66	-	dB
$V_{1(rms)}$	residual carrier signal (RMS value)		-	10	20	mV
$V_{11(rms)}$	residual 2nd harmonic of carrier signal (RMS value)		-	3	10	mV
System switch (note 12)						
V_{20}	maximum voltage for mode B/G		1.4	-	-	V
I_{20}	input current	V_{20} = 0 V	-	–300	-	μA
V_{20}	minimum voltage for mode L		-	-	3	V
V_{20}	maximum voltage for mode L		7	-	-	V
I_{20}	input current	3 V ≤ pin 20 ≤ 7 V	–150	-	250	μA
V_{20}	minimum voltage for MAC (positive)		-	-	9.5	V
I_{20}	input current	V_{20} = V_P	-	500	-	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC control circuit						
t_{11}	response to an amplitude increase of 52 dB of the IF input with the AGC switched to mode B/G	note 13	-	2	-	ms
t_{11}	response to an amplitude decrease of 52 dB of the IF input with the AGC switched to mode B/G	note 14	-	25	-	ms
	allowed leakage current of the AGC capacitor					
I_5	top sync level AGC		-	10	-	µA
I_5	white level AGC		-	200	-	nA
I_5	positive MAC AGC		-	50	-	nA
I_5	negative MAC AGC		-	200	-	nA
Tuner AGC (note 15)						
	input voltage for tuner AGC starting point					
V_3	IF input = 200 µV; negative slope		3.0	3.5	-	V
V_3	IF input = 100 mV; negative slope		-	5.0	5.5	V
V_3	IF input = 200 µV; positive slope		7.0	7.5	-	V
V_3	IF input = 100 mV; positive slope		-	9.0	9.5	V
I_4	maximum current swing of tuner AGC output		3	5	-	mA
V_4	output saturation voltage	I_4 = 2 mA	-	-	300	mV
I_4	leakage current		-	-	1	µA
ΔV_i	input signal variation complete tuner control		0.5	2.0	4.0	dB
V_3	minimum tuner take over voltage		-	-	1	V
Video switching circuit						
EXTERNAL VIDEO INPUT (AC coupled)						
$V_{10(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	1.0	-	V
I_{10}	input current		-	3.5	-	µA
V_{10}	top sync clamping level	I_{10} = 1 mA	-	3.3	-	V
INTERNAL VIDEO INPUT (DC coupled)						
$V_{12(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	2.0	-	V
$\lvert Z_{12} \rvert$	input impedance		-	2.0	-	kΩ
V_{12}	black level input voltage		-	3.3	-	V
VIDEO OUTPUT						
$V_{13(p-p)}$	output signal voltage (peak-to-peak value)		-	2.0	-	V
V_{13}	top sync level		-	2.7	-	V
V_{13}	noise clamping voltage level	I_{13} = 1 mA	-	2.5	-	V
I_{13}	internal bias current of npn emitter follower output transistor		-	1.5	-	mA
I_{13}	maximum source current		5	-	10	mA
B_{13}	bandwidth of output signal		-	5	-	MHz
	crosstalk of video signal	note 16				
α	external to internal		-	60	55	dB
α	internal to external		-	55	50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO SWITCH INPUT (note 17)						
V_7	maximum voltage for external video signal		-	-	2	V
V_7	minimum voltage for internal video signal		1	-	-	V
I_7	minimum source current for internal video signal		-	-	300	µA
I_7	input current	$V_7 = 0$ V	-	-	–1	mA
I_7	input current	$V_7 = V_P$	-	-	3	µA
AFC circuit (note 18)						
AFC SAMPLE-AND-HOLD/SWITCH (note 19)						
I_6	AFC switch: current level below which AFC outputs switches off		-	-	–500	µA
I_6	maximum AFC switch current	$V_6 = 0$ V	-	-	–1	mA
I_6	maximum leakage current		-	-	1	µA
AFC ANALOG OUTPUT ($V_9 > 8$ V; see Figs 4 and 5)						
$V_{8(p-p)}$	output voltage swing (peak-to-peak value)		10	-	11	V
I_8	maximum output current		500	-	-	µA
	control steepness		60	75	100	mV/kHz
V_8	AFC output voltage	AFC off	5	6	7	V
AFC DIGITAL OUTPUT (see Table 1)						
$V_{8,9}$	output voltage LOW		-	-	0.5	V
$V_{8,9}$	output voltage HIGH	50 kΩ load	4.5	-	5.5	V
Δf	frequency swing for switching AFC output Q1		65	80	100	kHz
$I_{8,9}$	maximum allowable output current		500	-	-	µA
AFC Analog SWITCH (note 20)						
I_9	minimum sink current for analog AFC		-	-	1.5	mA
V_9	minimum voltage for negative slope		-	-	10.2	V
V_9	minimum voltage for positive slope		-	-	8.0	V
V_9	maximum voltage for positive slope		10.2	-	-	V
I_9	output current	$V_9 = V_P$	-	500	-	µA
I_9	output current	$V_9 = 8$ to 10 V	-	150	-	µA
Video transmitter identification output (note 21)						
V_{18}	output voltage active	no sync; $I_{18} = 1$ mA	-	0.3	0.5	V
I_{18}	output current inactive	sync	-	-	3	µA
t_d	delay time of mute release after sync insertion		-	-	10	ms
I_{19}	allowed leakage current of identification detector capacitor		-	-	50	nA

Notes to the characteristics

1. All input signals are measured in RMS values at 100% carrier level and a frequency of 38.9 MHz.
2. On set AGC.
3. Input impedance selected so that a SAW filter can be applied without extra components.
4. Measured with 0 dB = 200 μV.
5. Measured at 10 mV(RMS) top sync input signal and the video output unloaded.
6. Projected zero point with internally switched demodulator.
7. With the AGC switch switched to ground, for the B/G standard, or with the identification capacitor switched to V_{CC} for the negative MAC standard.
8. With the AGC switch switched open for the L standard, or switched to V_{CC} for the positive MAC standard.
9. Measured in accordance with the test line given in Fig.8.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the phase angle of the 4.4 MHz signal at 20% and 80% luminance signal.
10. Measured in accordance with the test line shown in Fig.9.
    - The non-linearity is measured by comparing the differences between adjacent pairs of six luminance levels that make up the 5 step staircase. The measurement result is the largest percentage deviation in adjacent step values. The sign is always positive.
11. Measured with a 75 Ω source:

$$S/N = 20 \log \frac{V_{o\ \text{black-to white}}}{V_{n\ (RMS)\ \text{at}\ B = 5\ MHz}}$$

12. The internal circuit of pin 20 behaves as an internal voltage source of 4.5 V with an input resistance of 15 kΩ. Using the system switch three conditions can be obtained:
    - Negative modulation with top sync level AGC. This is achieved with pin 20 connected to ground.
    - Positive modulation with white level AGC. This is achieved with pin 20 open, or connected to 5 V.
    - Positive modulation with top white AGC and an increased time constant for MAC signals. This is achieved with pin 20 connected to V_{CC}.
13. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 200 μV to 80 mV input signals.
14. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 80 mV to 200 μV input signals.
15. It is possible to adjust the tuner AGC over the whole AGC range of the IF amplifier for both pnp and npn tuners. Tuner AGC starting point is defined as an output current of 0.2 mA for pnp and 1.8 mA for npn, in an application with a resistance of 6 kΩ to V_P at pin 4.
16. Crosstalk is defined as:

$$20 \log \frac{V_o\ \text{unwanted video black-to-white}}{V_o\ \text{wanted video black-to-white}}\ \text{measured at 4.4 MHz}$$

17. The video switch is controlled by a voltage on pin 7. The switching level is approximately 1.4 V. With pin 7 open-circuit internal video is selected; with pin 7 pulled to ground external video is selected.
18. Measurement taken with an input 10 mV(RMS). The unloaded Q factor of the reference tuned circuit is 70.
19. Switching off the AFC is obtained by a voltage of less than 2 V on pin 6. Normally this is achieved by pulling pin 6 to ground.

Notes to the characteristics (continued)

20. Switching to the normal analog AFC mode can be done by pulling pin 9 to a voltage above 10.2 V. Normally this is achieved by pulling pin 9 to V_P.
    The inverse analog AFC mode can only be obtained by a voltage of between 8 and 10 V applied to pin 9.
21. All timing figures defined with a capacitor of 2.2 nF at pin 19. The identification can be speeded up by lowering the value of this capacitor, however this makes the circuit also less sensitive if the video signal is disturbed (airplane flutter etc.). If the identification is only used as a sound mute a capacitor of 47 nF is recommended to improve the sensitivity.

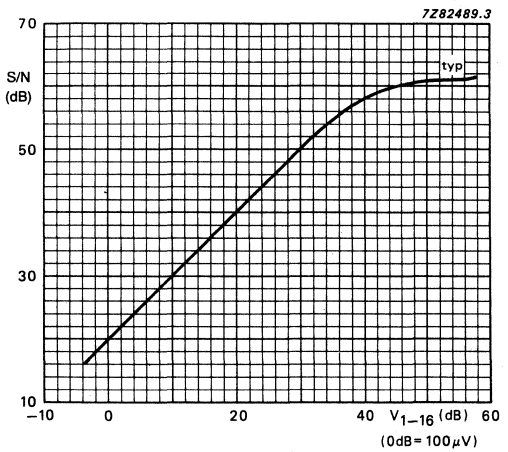


Fig.2 Signal-to-noise ratio as a function of video input.

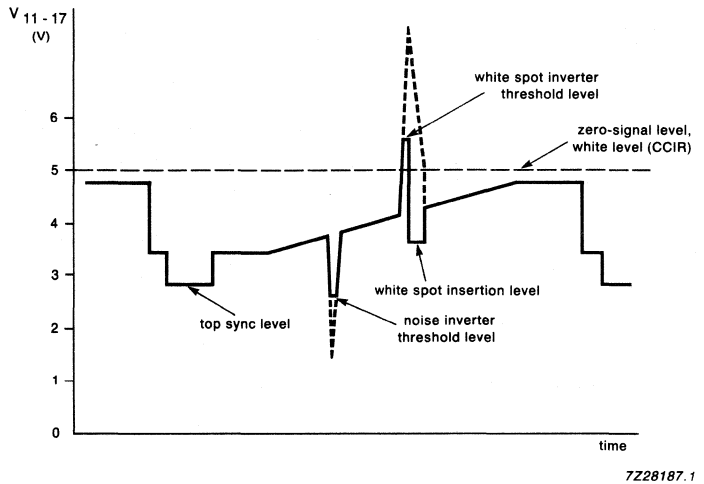


Fig.3 Video waveform showing white spot threshold and insertion levels, and noise clamping level.

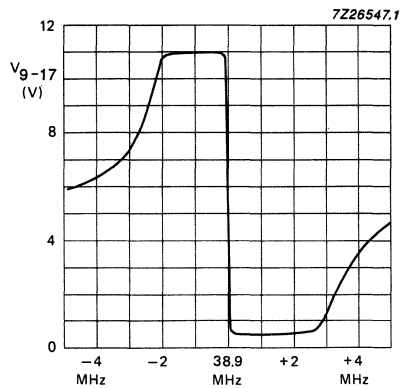


Fig.4 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

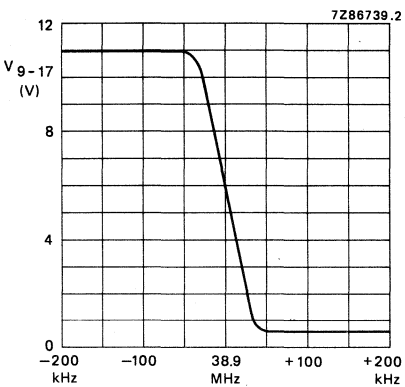
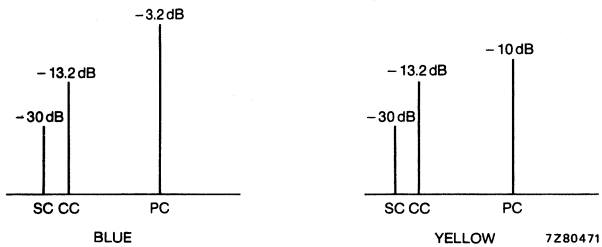


Fig.5 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

Table 1 Digital AFC truth table

INPUT FREQUENCY	Q1	Q2
> IF +40 kHz	0	1
> IF	1	1
< IF	1	0
< IF −40 kHz	0	0



SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level

Fig.6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

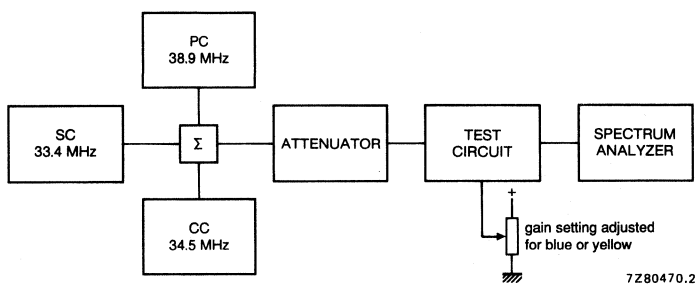


Fig.7 Test set-up intermodulation measurements.

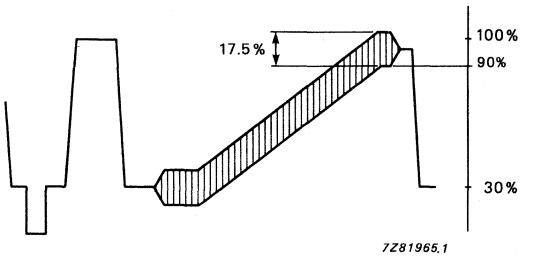


Fig.8 Video output signal.

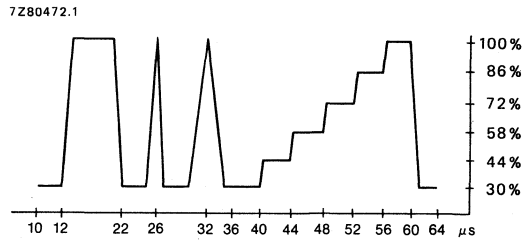


Fig.9 E.B.U. test signal wave form (line 330).

SYNCHRONIZATION PROCESSOR FOR TELEVISION RECEIVERS

GENERAL DESCRIPTION

The TDA8370 is a sync processor designed to generate and synchronize horizontal and vertical signals in medium and high performance television receivers. The device is particularly suitable for application with teletext decoders and video tape recorders.

A video switch controlled by I^2C bus command or analogue switched voltage selects internal or external composite video signals.
The processing of not line-locked vertical sync in non-standard mode is also possible.

Features

- Two separate video inputs adapted to:
  I.F. detector (front-end output)
  or
  peri-television connector selected by the video switch
- Buffered video output
- Horizontal sync separator with self-aligning levels
- Vertical sync separator 1 with self-aligning levels when standard mode selected
- Vertical sync separator 2 with self-aligning levels when non-standard mode selected (e.g. video tape recorder signal)
- Noise invertor
- Gated phase discriminator with switchable time constant for non-standard applications
- 6 MHz VCO for generation of clock signal for teletext display
- Noise level detector
- Automatic low-current starting circuit
- φ 2 phase control with shift adjustment not affecting gain or time constant
- Horizontal output optimized for operation with self-oscillating power supply
- Vertical divider system with automatic selection of 625 or 525 standard
- 50/60 Hz identification output voltage
- Mute output
- Coincidence detector
- Vertical shaping and feedback system with automatic 60 Hz amplitude correction
- 3-level sandcastle output
- Vertical guard circuit active via sandcastle output
- Scan composite sync ($\overline{\text{S.C.S.}}$) output as slave input for teletext decoder
- Special "sense" ground pin to ensure correct feedback voltage in the frame deflection circuit
- I^2C bus controlled teletext non-interlaced signal (N.I.L.)
- Line and frame frequencies switched to nominal when noise only is received in standard mode

PACKAGE OUTLINES

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5	5,5	10	mA
Video input voltage (positive video)					
pin 1 (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3	V
pin 5 (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1	1,4	V
Horizontal flyback input current (pin 18)	I_{18}	0,3	1	4	mA
Vertical comparator input (pin 14)					
a.c. input voltage (peak-to-peak value)	$V_{14\text{-}20(p\text{-}p)}$	–	3	–	V
d.c. input voltage	$V_{14\text{-}20}$	–	2,5	–	V
I^2C clock input/analogue input (pin 7)					
analogue video switching voltage level	$V_{7\text{-}20}$	6,5	–	7,5	V
I^2C data input/analogue input (pin 8) for selecting peri-television connector input					
analogue switching voltage level for selecting non-standard mode (equal to V.T.R.)	$V_{8\text{-}20}$	6,5	–	7,5	V
Max. horizontal output voltage (pin 17)	$V_{17\text{-}20}$	14	–	16	V
Max. vertical drive output voltage (pin 13)	$V_{13\text{-}20}$	–	–	10	V
Sandcastle 3-level output voltage (pin 9)					
burstkey	$V_{9\text{-}20}$	–	10,8	–	V
horizontal blanking	$V_{9\text{-}20}$	4,1	4,4	4,9	V
vertical blanking	$V_{9\text{-}20}$	2,1	2,6	2,9	V
Scan composite sync output (pin 10)					
high output voltage at $-I_{10} = 5$ mA	$V_{10\text{-}20}$	4,3	4,8	5,3	V
output current	$-I_{10}$	–	1	–	mA
Video output (pin 3)					
a.c. output voltage (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,6	3	3,4	V
d.c. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
50/60 Hz identification output voltage (pin 4)					
50 Hz at $I_4 = 0,1$ mA	$V_{4\text{-}20}$	–	1,3	1,7	V
60 Hz at $-I_4 = 5$ mA	$V_{4\text{-}20}$	8	10	–	V
output current	$-I_4$	–	–	5	mA
Mute output voltage (pin 28)					
in-sync at $I_{28} = 0,1$ mA	$V_{28\text{-}20}$	–	1,2	1,5	V
out-of-sync/no sync at $-I_{28} = 0,5$ mA	$V_{28\text{-}20}$	–	10,5	–	V

DEVELOPMENT DATA

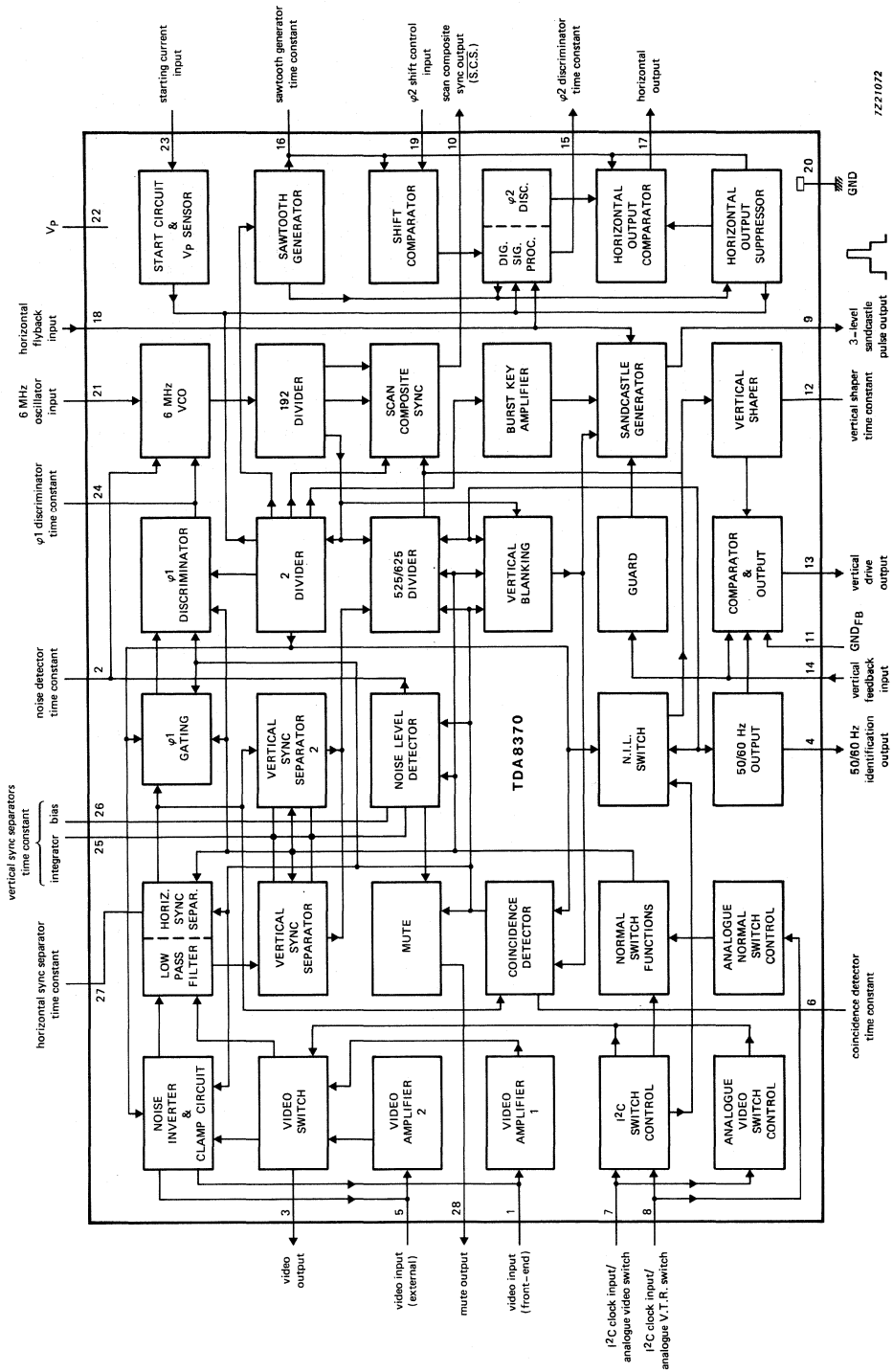


Fig. 1 Block diagram.

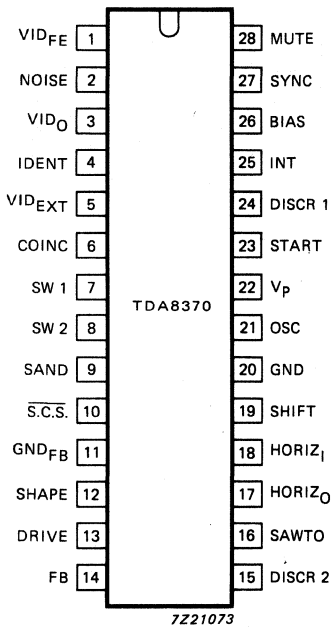


Fig. 2 Pinning diagram.

PINNING

1	VID_{FE}	video input (front-end)
2	NOISE	noise detector time constant
3	VID_O	video output
4	IDENT	50/60 Hz identification output
5	VID_{EXT}	video input (external)
6	COINC	coincidence detector time constant
7	SW 1	I^2C clock input/analogue video switch
8	SW 2	I^2C data input/analogue V.T.R. switch
9	SAND	3-level sandcastle pulse output
10	$\overline{S.C.S.}$	scan composite sync output
11	GND_{FB}	ground feedback input
12	SHAPE	vertical shaper time constant
13	DRIVE	vertical drive output
14	FB	vertical feedback input
15	DISCR 2	φ 2 discriminator time constant
16	SAWTO	sawtooth generator time constant
17	$HORIZ_O$	horizontal output
18	$HORIZ_I$	horizontal flyback input
19	SHIFT	φ 2 shift control input
20	GND	ground
21	OSC	6 MHz oscillator time constant
22	V_P	positive supply voltage
23	START	starting current input
24	DISCR 1	φ 1 discriminator time constant
25	INT	integrator time constant vertical sync separators
26	BIAS	time constant bias vertical sync separators
27	SYNC	horizontal sync separator time constant
28	MUTE	mute output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 22)	V_P	max.	13,2	V
Starting current (pin 23)	I_{23}	max.	10	mA
Power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

Thermal resistance

From junction to ambient (in free)	$R_{th\ j\ a}$	=	40	K/W
Operating junction temperature	T_j	max.	150	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; I_{23} = 5,5 mA; 6 MHz clock oscillator operating at nominal frequency; synchronized; T_{amb} = 25 °C; measured in test set-up Fig. 6; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5,0	5,5	10	mA
Video input (pin 1)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3,0	V
D.C. level top sync	$V_{1\text{-}20}$	5,0	5,5	6,5	V
Input impedance	$\lvert Z_{1\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression *		20	–	–	dB
Video input (pin 5)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1,0	1,4	V
D.C. level top sync	$V_{5\text{-}20}$	3,5	4,2	4,9	V
Input impedance	$\lvert Z_{5\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression		20	–	–	dB
Video output (pin 3)					
Output voltage** positive video (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,7	3,0	3,3	V
D.C. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
Resistance npn emitter follower	$R_{3\text{-}20}$	–	–	50	Ω
Bandwidth at $-I_3$ = 5 mA	B	10	15	–	MHz
Crosstalk between video signals pin 1 or pin 5 to pin 3		–	–	–54	dB
Noise inversion threshold level	$V_{3\text{-}20}$	1,9	2,1	2,3	V

* When not selected the negative-going input voltage is clamped at 0 V.

** Measured at $V_{1\text{-}20(p\text{-}p)}$ = 2,25 V or $V_{5\text{-}20(p\text{-}p)}$ = 1 V.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Horizontal sync separator (pin 27)					
D.C. voltage level	V_{27-20}	–	6,2	–	V
Line ripple voltage (peak-to-peak value)					
during standard mode	V_{27-20}	–	2,8	–	mV
during non-standard mode	V_{27-20}	–	0,6	–	mV
φ 1 discriminator (pin 24)					
Catching range	$\pm \Delta f$	600	1000	1400	Hz
Holding range	$\pm \Delta f$	*	1000	1200	Hz
Phase shift		–	0,5	–	μs/kHz
Input resistance during sync pulse					
with slow time constant	R_{24-20}	–	12,6	–	kΩ
with fast time constant	R_{24-20}	–	2,2	–	kΩ
6 MHz VCO (pin 21)					
Output frequency free running at $V_{2-20} > 7$ V	f_o	–	6	–	MHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%
Frequency variation as a function of supply voltage	$\Delta f_o/\Delta V_p$	–	–	0,01	
Temperature coefficient of oscillator frequency	TC_{osc}	–	1400	–	Hz/K
A.C. input voltage (peak-to-peak value)	$V_{21-20(p-p)}$	–	0,3	–	V
D.C. input voltage	V_{21-20}	–	1,6	–	V
Sawtooth generator (pin 16)					
Start of negative slope of sawtooth	V_{16-20}	–	7,2	–	V
Start flyback of sawtooth	V_{16-20}	–	3,7	–	V
φ 2 trigger pulse width (see Fig. 3)	t_W	–	6,8	–	μs
φ 2 loop not synchronized by φ 1 loop					
Start of negative slope of sawtooth	V_{16-20}	–	7,2	–	V
Start flyback of sawtooth	V_{16-20}	–	3,4	–	V
Flyback time (see Fig. 3)	t_{fb}	0,9	1,3	1,7	μs
Output frequency free running at V_p = 8,5 V	f_o	–	15,4	–	kHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal output (pin 17)					
Output current open collector npn; V_{17-20} = 0,5 V	I_{17}	–	–	10	mA
Output voltage protection (2 internal zener diodes)	V_{17-20}	14	–	16	V
Maximum output current during voltage protection	I_{17}	–	0	1	mA
Delay between start of sawtooth output pulse at pin 16 and:					
negative-going edge of horizontal output voltage (see Fig. 3)	t_{d1}	14,5	16	17,5	μs
positive-going control edge of horizontal output voltage (see Fig. 3)	$t_{d2(min.)}$	25	28	31	μs
	$t_{d2(max.)}$	–	T_H	–	μs
	t_{d2}*	–	T_H	–	μs
Condition: I_{23} = 5 to 10 mA					
Horizontal output pulse present if:	V_{23-20}	–	–	6	V
Horizontal output pulse not present if:	V_{23-20}	4	–	–	V
and	I_{23}	3	–	–	mA
δ Horizontal output is a function of the input voltage at pin 23					
δ = 0	V_{23-20}	–	–	4	V
δ = maximum	V_{23-20}	8,5	–	–	V
Horizontal output suppression time	t_s	20	22	24	μs
φ 2 discriminator (pin 15)					
Control current	$\pm I_{15}$	600	800	1000	μA
Control sensitivity	$\Delta\varphi_i/\Delta\varphi_o$	–	400	–	
Input current at V_{15-20} = 4 V; V_P = 0 V	I_{15}	–	–	0,6	μA
Condition: No flyback pulse and $V_{23-20} > 5$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V
Condition: $V_P < 8,9$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V

* Delay with no horizontal flyback pulse present at pin 18.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
φ 2 shift control input (pin 19)					
Shift control range		–	$1/16T_H+\Delta$	–	μs
Δ		0,2	–	1	μs
Delay between rising edge of horizontal flyback at the slicing level and rising edge of burst key pulse (see Fig. 2)	$t_{d3(min.)}$	–	3	–	μs
	$t_{d3(max.)}$	–	$7+\Delta$	–	μs
t_{d3} = min. when:	V_{19-20}	–	–	4,5	V
t_{d3} = max. when:	V_{19-20}	0	–	–	V
Shift control is active when:	V_{22-20}	$>8,9$	$>9,5$	>10	V
Starting control input (pin 23)					
Starting by current to pin 23: minimum	I_{23}	3	–	5	mA
maximum allowed	I_{23}	–	–	10	mA
Starting by a voltage on pin 22: required input current	I_{23}	0	–	10	mA
Stabilized voltage	V_{23-20}	8,2	8,7	9,2	V
Supply current is added to starting current if: $V_P > V_{23-20}$ and $V_{23-20} < 8,5$ V	V_{23-20}	–	V_P-V_{BE}	–	V
Horizontal flyback input (pin 18)					
Slicing level input voltage	V_{18-20}	0,7	0,9	1,1	V
Input current	I_{18}	0,3	1	4	mA
Maximum input current	$-I_{18}$	–	–	1	mA
Maximum input voltage	V_{18-20}	–	–	V_P	V
Vertical sync separator integrator time constant (pin 25)					
Condition: Standard mode					
D.C. voltage level of vertical sync top of integrated video	V_{25-20}	8,5	9,0	9,5	V
black level of integrated video during vertical blanking	V_{25-20}	4,0	4,5	5,0	V
Input resistance	R_{25-20}	–	5,1	–	kΩ
Condition: Non-standard mode					
Input voltage level of integrated vertical sync top level	V_{25-20}	9,5	10,7	11,0	V
integrated vertical sync amplitude (peak-to-peak value)	$V_{25-20(p-p)}$	–	8,9	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Vertical sync separator biasing (pin 26)					
Input voltage in standard mode	V_{26-20}	–	5,9	–	V
Input voltage in non-standard mode	V_{26-20}	–	8,4	–	V
Vertical shaper (pin 12)					
Condition: 50 Hz					
Ramp voltage starting level	V_{12-20}	–	2	–	V
Flyback voltage starting level	V_{12-20}	6,0	6,25	6,5	V
Condition: 60 Hz					
Ramp voltage starting level	V_{12-20}	–	2	–	V
Flyback voltage starting level	V_{12-20}	5,35	5,6	5,85	V
Flyback time (normal)	t_{fb}	170	220	270	μs
Flyback time controlled by second half of N.I.L. signal		–	$t_{fb}-32$	–	μs
Vertical drive output (pin 13)					
Open collector pnp					
Maximum output current at V_{13-20} = 8 V	$-I_{13}$	3	–	–	mA
Output voltage LOW with 100 kΩ resistor to ground	V_{13-20}	–	–	300	mV
Vertical feedback input (pin 14)					
A.C. input voltage not synchronized					
50 and 60 Hz condition: non-standard mode input voltage (peak-to-peak value)	$V_{14-11(p-p)}$	–	3	–	V
d.c. average input voltage	V_{14-11}	–	2,8	–	V
Parabolic pre-correction convex (50 Hz)		–	4	–	%
Parabolic pre-correction convex (60 Hz)		–	3,3	–	%
Guard circuit input input voltage HIGH	V_{14-11}	5,3	5,7	6,1	V
input voltage LOW	V_{14-11}	–	–	0	V
input voltage at V_{14-20} = 2,5 V	$-I_{14}$	–	1,5	6,1	μA
Ground feedback input (pin 11)					
A.C. feedback voltage	V_{11-20}	–	0	–	V

parameter	symbol	min.	typ.	max.	unit
50/60 Hz identification output (pin 4)					
50 Hz output voltage at I_4 = 0,1 mA	V_{4-20}	–	1,3	1,7	V
60 Hz output voltage at $-I_4$ = 5 mA	V_{4-20}	8	10	–	V
3-level sandcastle output (pin 9)					
Output voltage during burst key at $-I_9$ = 0,5 mA	V_{9-20}	–	10,8	–	V
at $-I_9$ = 5 mA	V_{9-20}	8,0	9,7	–	V
Output voltage during horizontal blanking at $-I_9$ = 0,5 mA	V_{9-20}	4,1	4,4	4,9	V
Output voltage during vertical blanking at $-I_9$ = 0,5 mA	V_{9-20}	2,1	2,6	2,9	V
Zero level output voltage at I_9 = 0,5 mA	V_{9-20}	–	0,25	0,5	V
Pulse width: burst key at V_{9-20} = 7 V	t_W	3,7	4,0	4,3	µs
horizontal blanking at V_{9-20} = 3,5 V	t_W	–	*	–	
Vertical blanking (see Fig. 4)					
Condition: 50 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	µs
Duration of vertical blanking	t_d	–	$22{,}5T_H - t_{bk}$	–	µs
Condition: 50 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	$-(2{,}5T_H + 20\ \mu s)$	–	
Duration of vertical blanking	t_d	–	$25T_H + 2\ \mu s$	–	
Condition: 60 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	µs
Duration of vertical blanking	t_d	–	$18{,}5T_H - t_{bk}$	–	µs
Condition: 60 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	0	–	µs
Duration of vertical blanking	t_d	–	$18{,}5T_H$	–	µs
Phase position of burst key delay between the middle of the sync pulse on the video input and the rising edge of the burst key pulse at a slicing level of 7 V		2,5	2,9	3,3	µs

* Width of horizontal flyback on pin 18 pulse at the slicing level.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
$\overline{\text{S.C.S.}}$ output (pin 10)					
Output voltage HIGH at $-I_{10} = 5$ mA	$V_{10\text{-}20}$	4,3	4,8	5,3	V
Output voltage LOW at $I_{10} = 0{,}5$ mA	$V_{10\text{-}20}$	–	0,2	0,5	V
Conditions:*					
Noise only on video input pin 1 or 5 or indirect sync 50 Hz with a 4,7 μs horizontal sync pulse width on pin 1 or 5					
Delay between the starting edge of the horizontal sync pulse of the video input signal and the starting edge of the horizontal sync pulse in the $\overline{\text{S.C.S.}}$ signal		–0,25	0	0,25	μs
Noise detector time constant (pin 2)					
Condition: Standard mode					
Output voltage					
strong signal	$V_{2\text{-}20}$	–	4,6	5,3	V
noise only**	$V_{2\text{-}20}$	–	7,2	–	V
Switching voltage level					
strong signal → noise only	$V_{2\text{-}20}$	5,7	6,2	6,7	V
noise only → strong signal	$V_{2\text{-}20}$	–	5,6	–	V
Coincidence detector (pin 6)					
Average voltage level					
in-sync	$V_{6\text{-}20}$	6,8	8	–	V
out-of-sync	$V_{6\text{-}20}$	–	–	2,1	V
noise only	$V_{6\text{-}20}$	–	–	2,4	V
Switching voltage level (see also Fig. 5)					
fast → normal$^{\Delta}$	$V_{6\text{-}20}$	–	4,4	–	V
normal → fast$^{\Delta}$	$V_{6\text{-}20}$	–	2,4	–	V

* All other conditions will cause distorted vertical sync pulses and/or equalizing pulses in the $\overline{\text{S.C.S.}}$ signal.

** When noise only is received the 6 MHz oscillator is switched to nominal frequency and the frame divider to the 625 standard.

Δ This switching level is also valid for clamp gating, φ 1 gating, muting, frame divider indirect/direct sync, horizontal sync separator gated/self-aligned and noise detector inhibit/inhibit off.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 28)					
Output voltage					
not synchronized					
at $-I_{28}$ = 0,5 mA	V_{28-20}	–	10,5	–	V
at $-I_{28}$ = 5 mA	V_{28-20}	7,0	8,5	–	V
synchronized					
at I_{28} = 0,1 mA	V_{28-20}	–	1,2	1,5	V
I²C clock input/ analogue input video switch (pin 7)					
Input voltage					
analogue input inactive	V_{7-20}	5	–	–	V
analogue input switching level (external video selected)	V_{7-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\lvert I_7 \rvert$	–	–	10	μA
at V_P = 12 V	$-I_7$	–	–	10	μA
I²C clock input switching voltage level	V_{7-20}	1,5	2,6	3,0	V
I²C data input/ * analogue V.T.R. switch (pin 8)					
Input voltage					
analogue input inactive	V_{8-20}	5	–	–	V
analogue input switching level (non-standard mode)	V_{8-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\lvert I_8 \rvert$	–	–	10	μA
at V_P = 12 V	$-I_8$	–	–	10	μA
I²C data input switching voltage level	V_{8-20}	1,5	2,6	3,0	V
During acknowledge					
pull-down current	$-I_8$	–	–	5	mA
saturation voltage	V_{8-20}	–	–	1,5	V

* For address and data byte definition see Fig. 6 and Table 1 respectively.

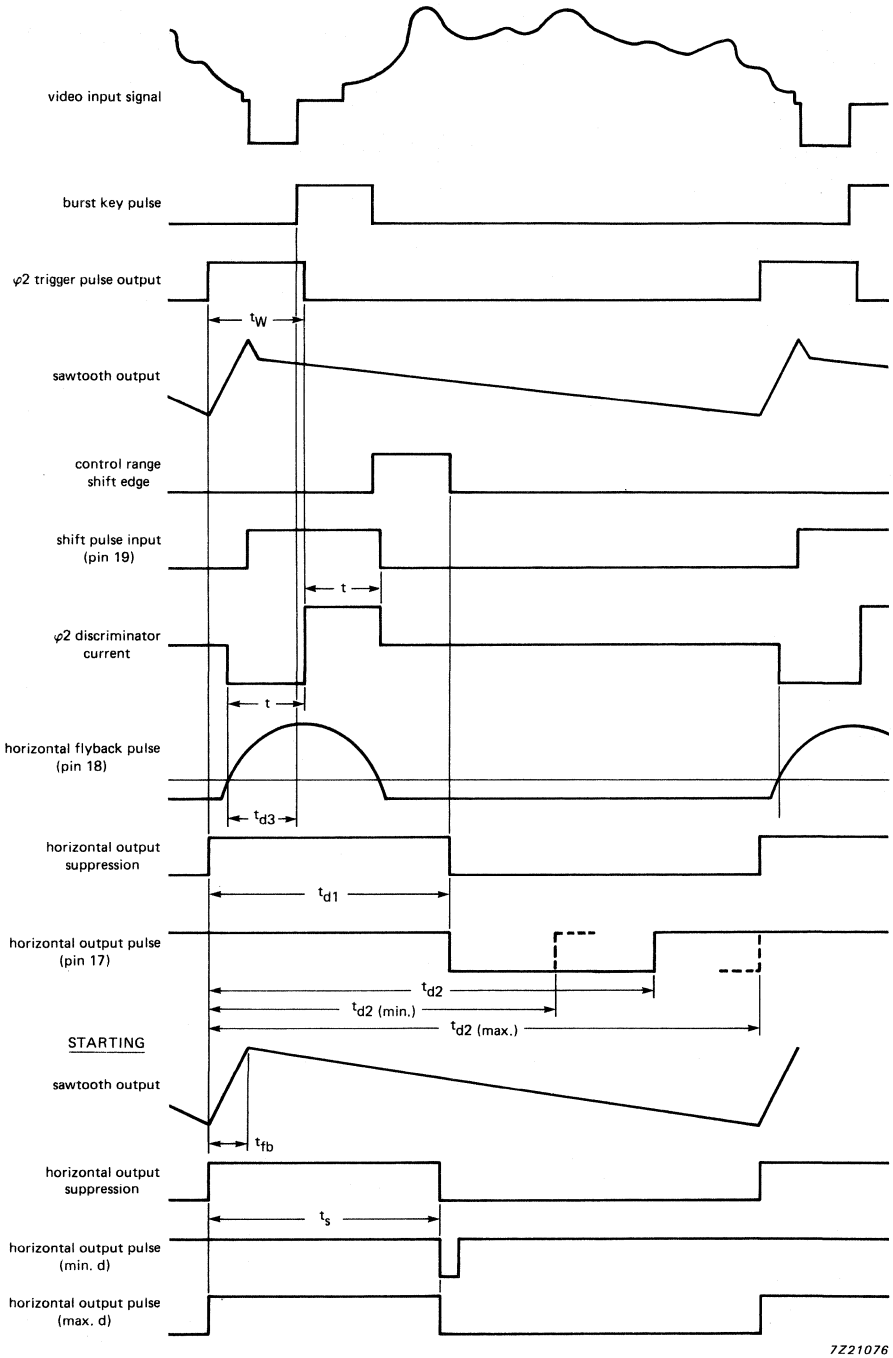


Fig. 3 Timing diagram; video input and starting time.

DEVELOPMENT DATA

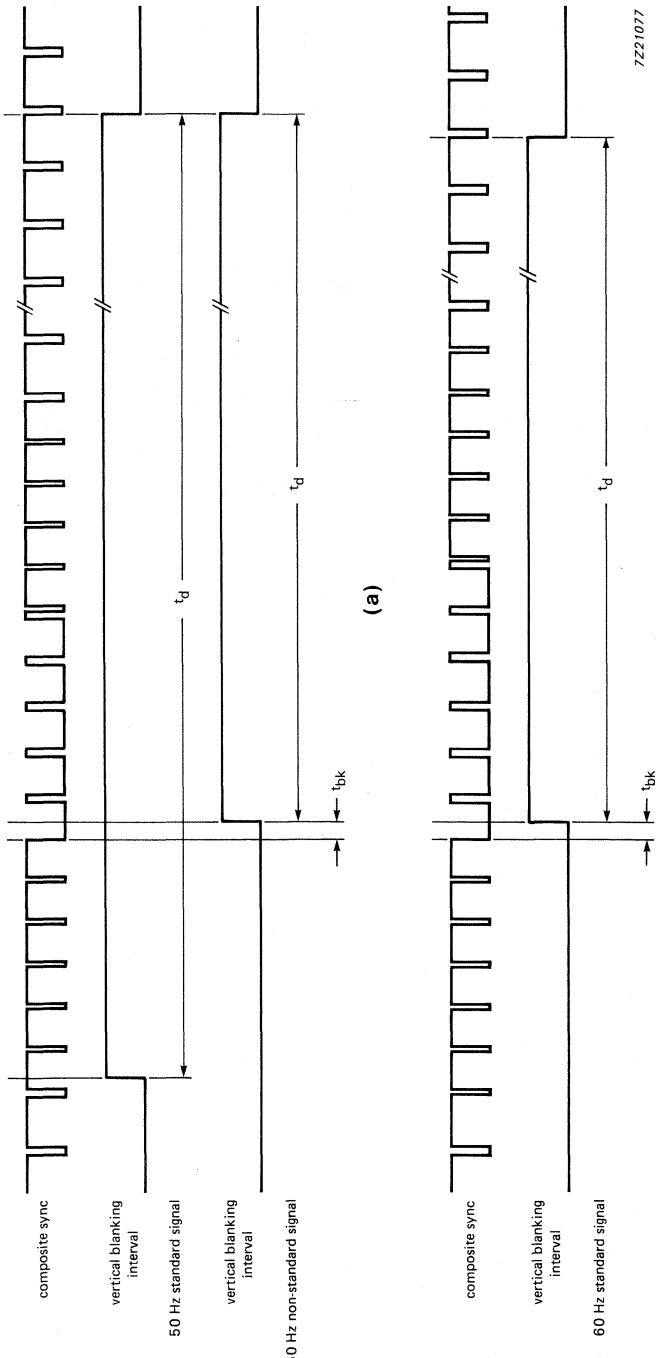
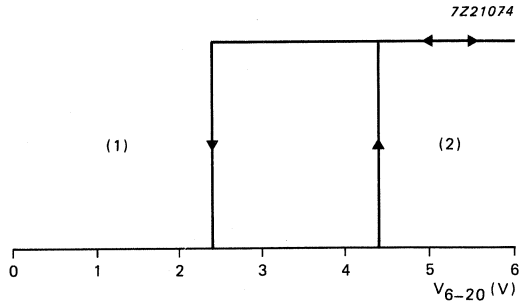


Fig. 4 Timing diagram; vertical blanking synchronization
(a) 50 Hz standard (b) 60 Hz standard.



(1) φ 1 gating circuit off
φ 1 discriminator to fast mode
clamping gate off
mute output HIGH
frame divider direct sync
horizontal sync separator self-aligned
noise detector not inhibited

(2) φ 1 gating circuit on
φ 1 discriminator to slow mode
clamping gate on
mute output LOW
frame divider indirect sync
horizontal sync separator gated
noise detector inhibited

Fig. 5 Coincidence detector time constant switching levels.

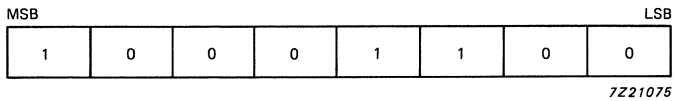


Fig. 6 Address byte.

Table 1 Data byte

	bit no.	logic level	description
MSB	D7	1	*
	D6	1	*
	D5	1	*
	D4	1	*
	D3	1	bit number D5 = don't care
	D3	0	bit numbers D6 and D7 = don't care
	D2	1	$\overline{\text{N.I.L.}}$ (inactive)
	D2	0	N.I.L. (active)
	D1	1	$\overline{\text{VID}_{\text{EXT}}}$ (inactive)
	D1	0	VID_{EXT} (active)
	D0	1	standard mode
LSB	D0	0	non-standard mode

* Bits D7 to D4 are used for measuring procedure in the IC factory.
For application use they must be inactive (logic 1).

DEVELOPMENT DATA

APPLICATION INFORMATION

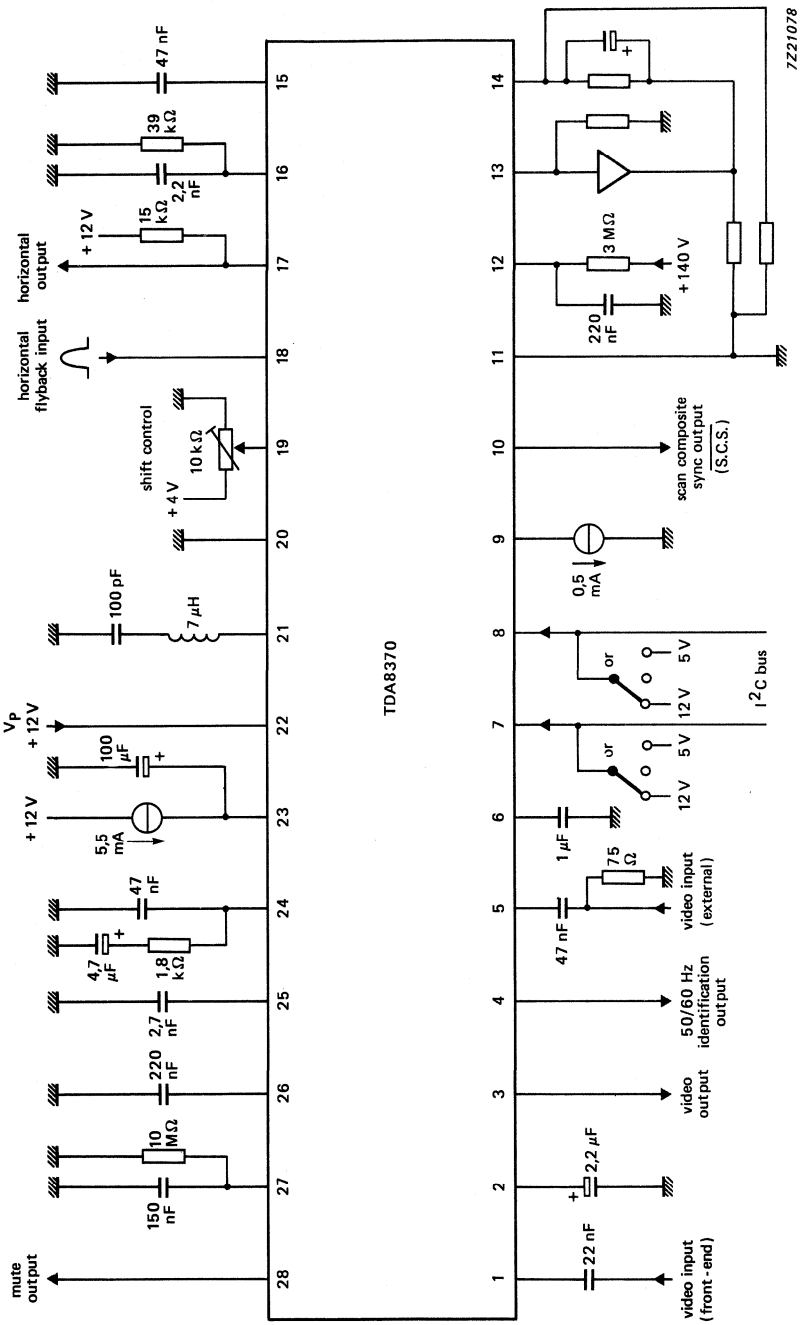


Fig. 7 Application diagram and test circuit.

CONTROL CIRCUIT FOR SWITCHED MODE POWER SUPPLIES

GENERAL DESCRIPTION

The TDA8380 is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380 operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

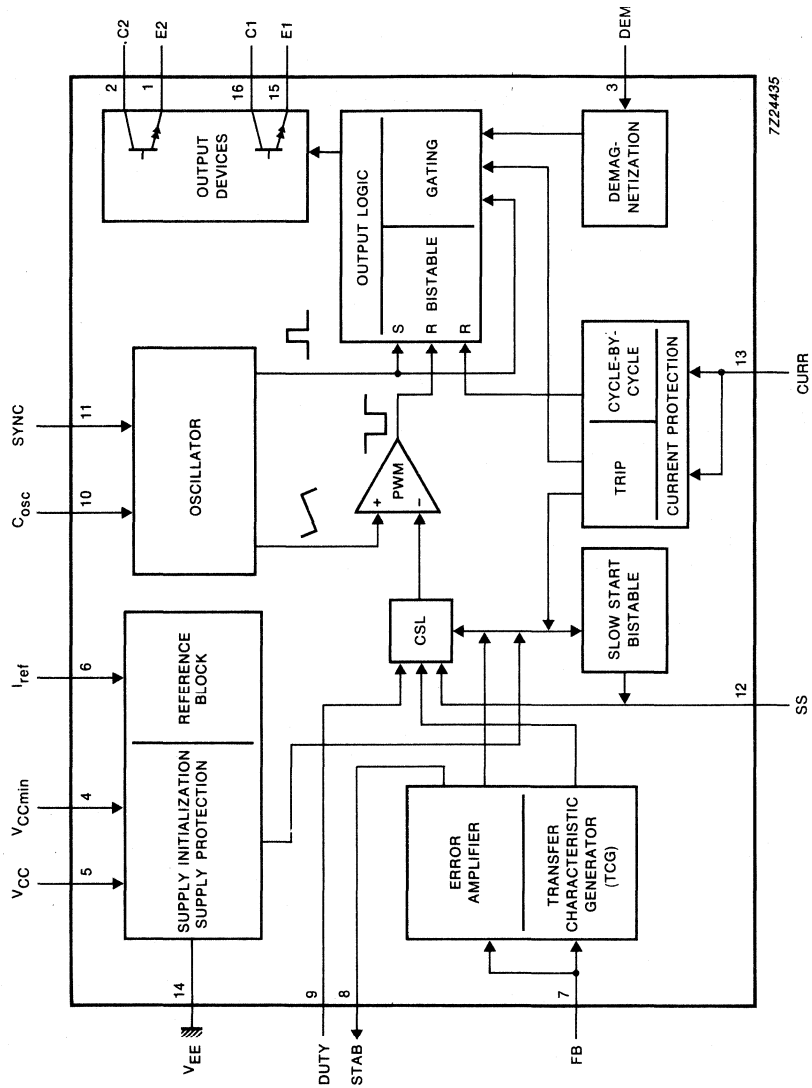


Fig.1 Block diagram.

PINNING

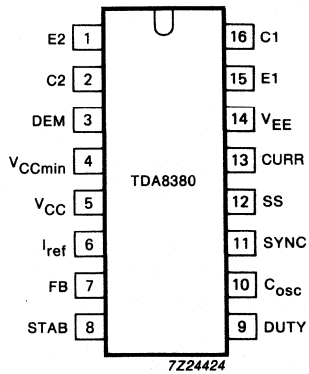


Fig.2 Pinning diagram.

DEVELOPMENT DATA

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380 is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

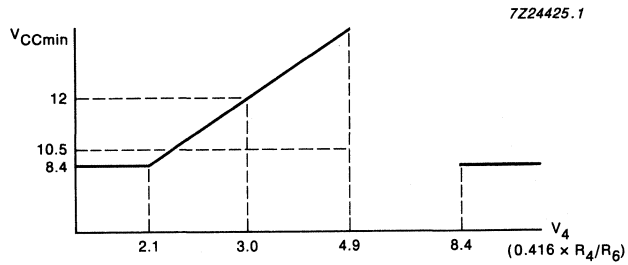


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

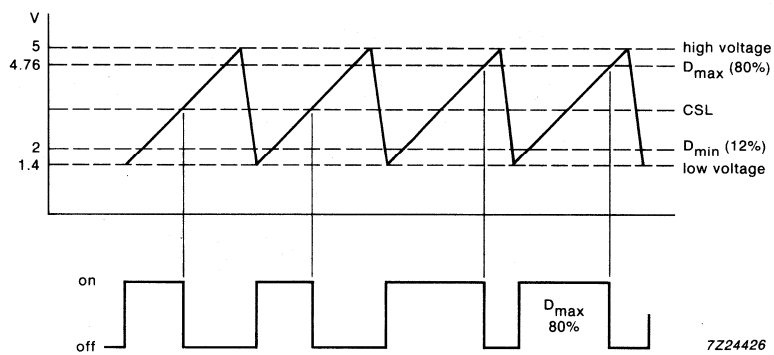


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

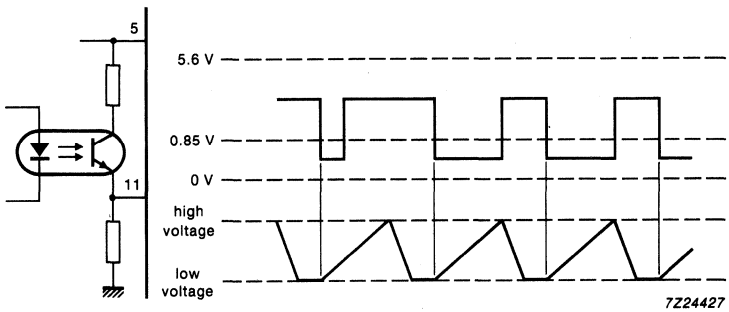


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

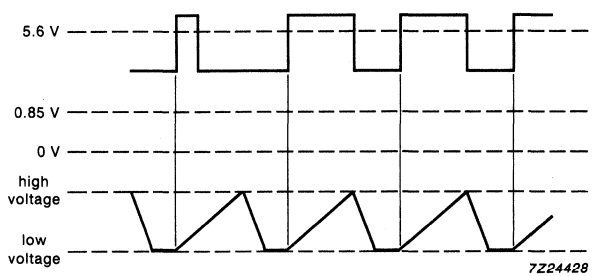
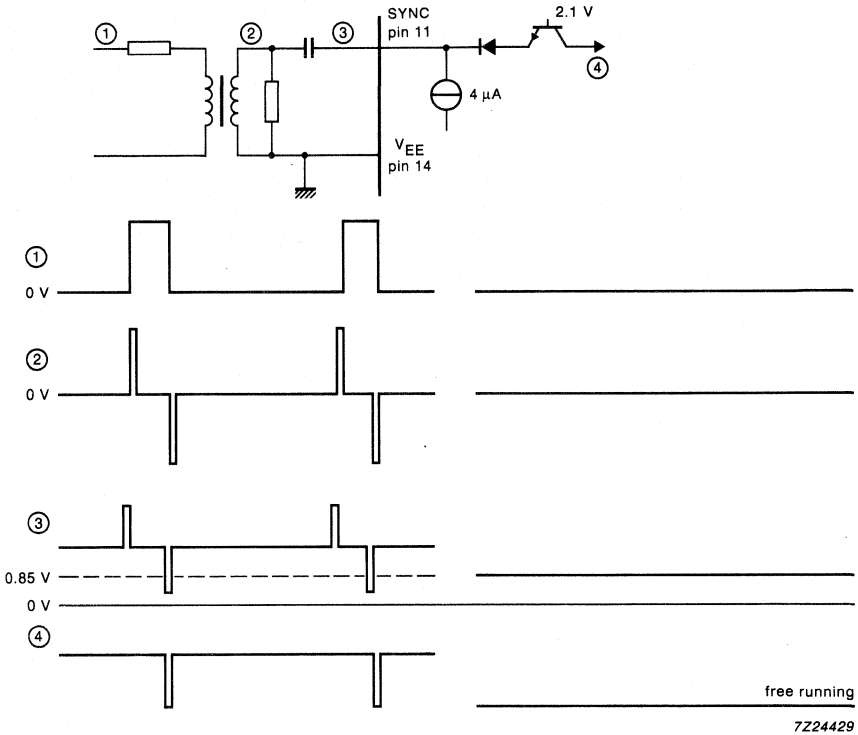


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

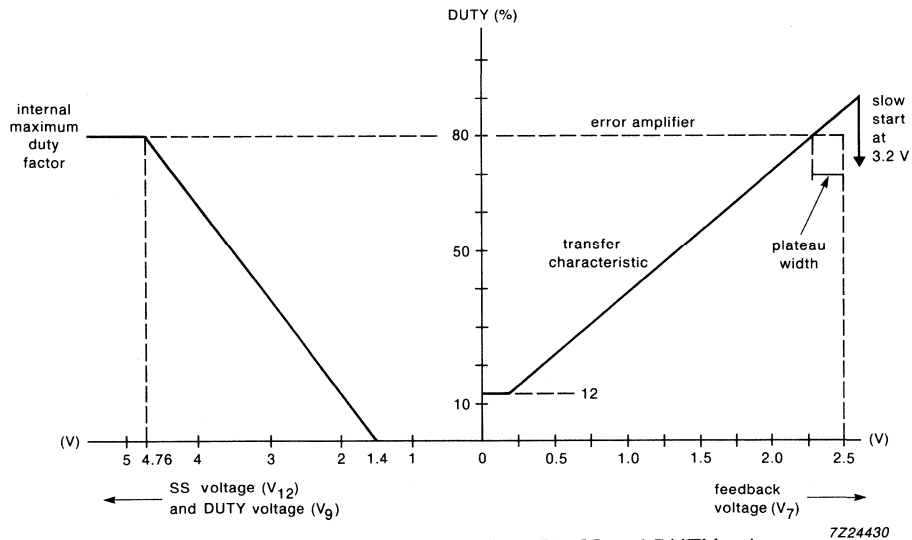


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

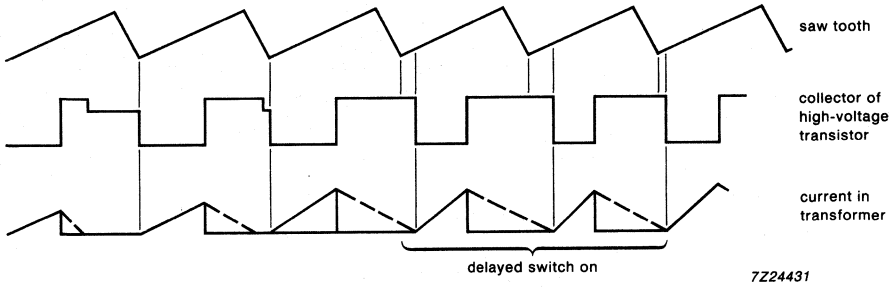


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

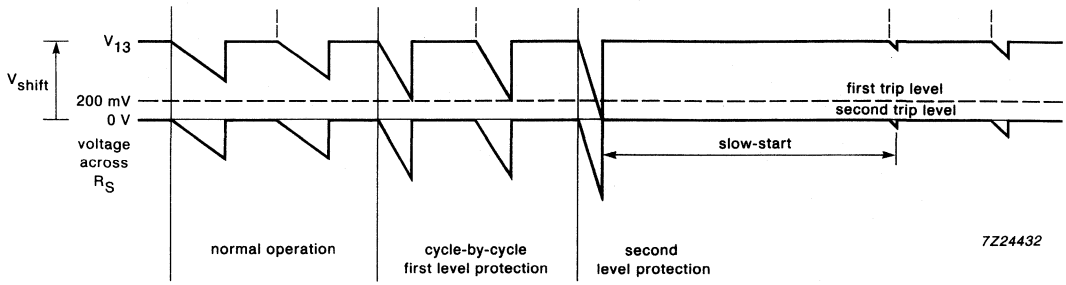


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

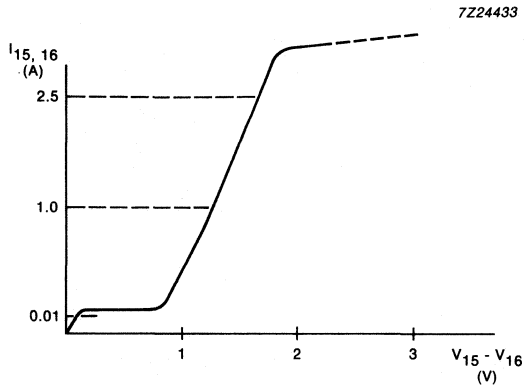


Fig.10 Saturation curve.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.11			
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 55$ K/W

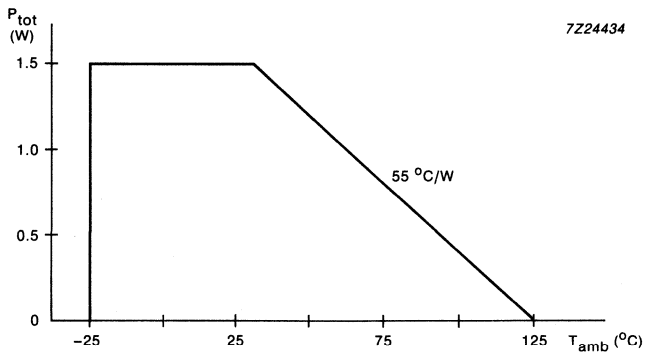


Fig.11 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	I_6/5.7	I_6/6	I_6/6.4	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	I_6/5.7	I_6/6	I_6/6.3	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	–	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	–	V
at 1 A		$V_{16} - V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	–	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16\text{-}15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at −700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Pin voltage	at 0 A	V_3	–	690	–	mV
Input current	at 0 V	I_3	−30	−40	−55	μA
Current range of clamp circuits		I_3	−10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at −10 mA	V_3	–	−800	–	mV
Current protection						
Input current	note 1	I_{13}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	−10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to −200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	−800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

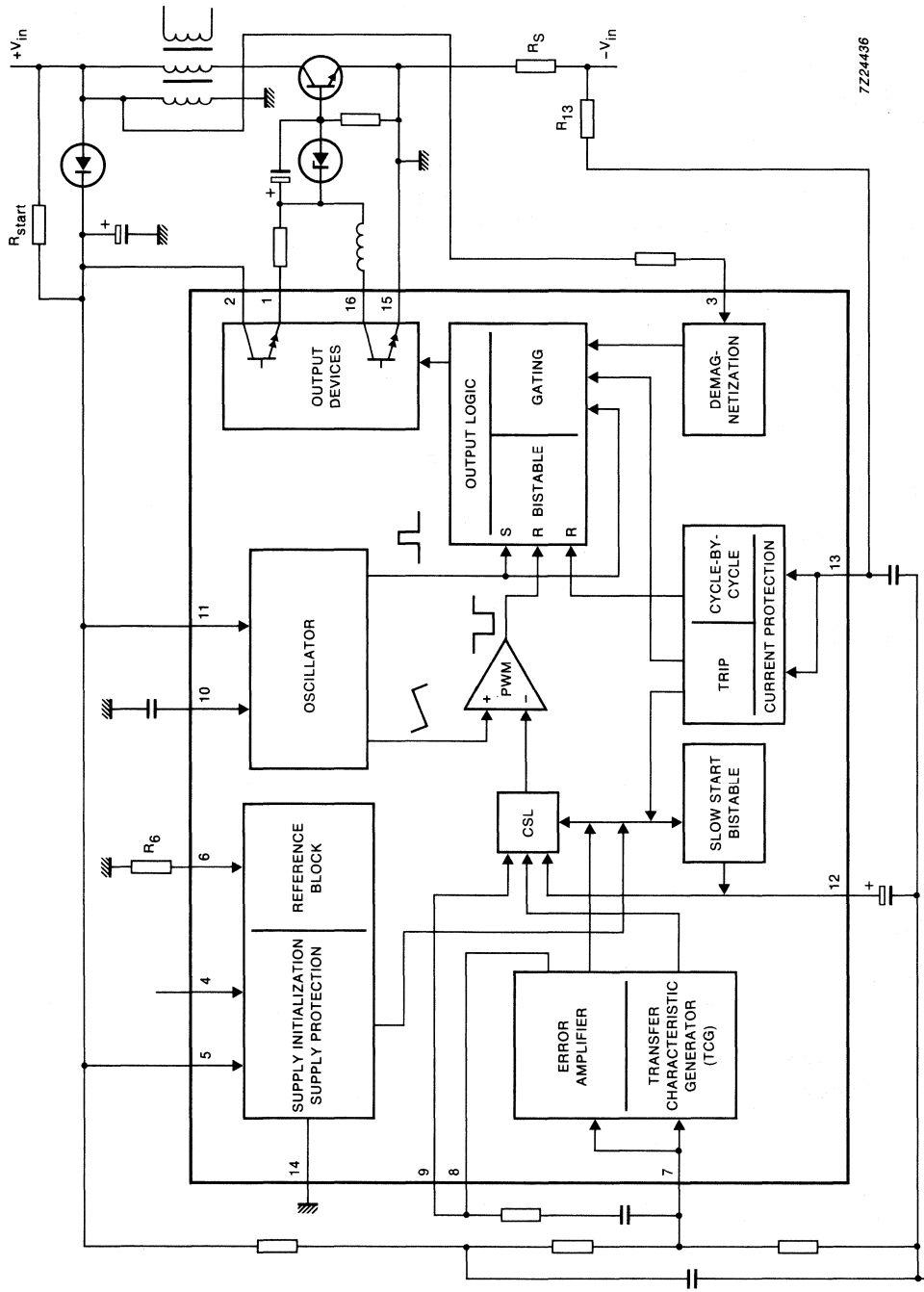


Fig.12 Simplified application diagram.

DEVELOPMENT DATA

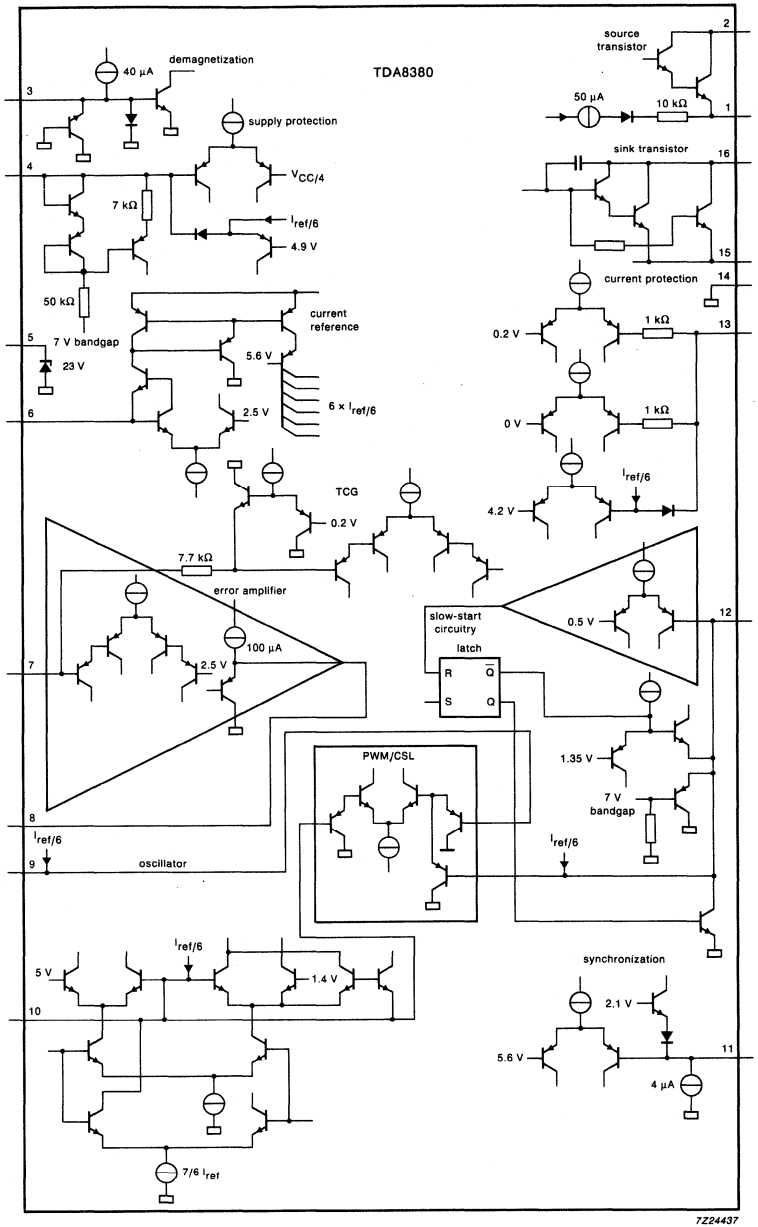


Fig.13 Input and output loading diagram.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8415 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8415 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Function and software are compatible with the TDA8405
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation						
stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

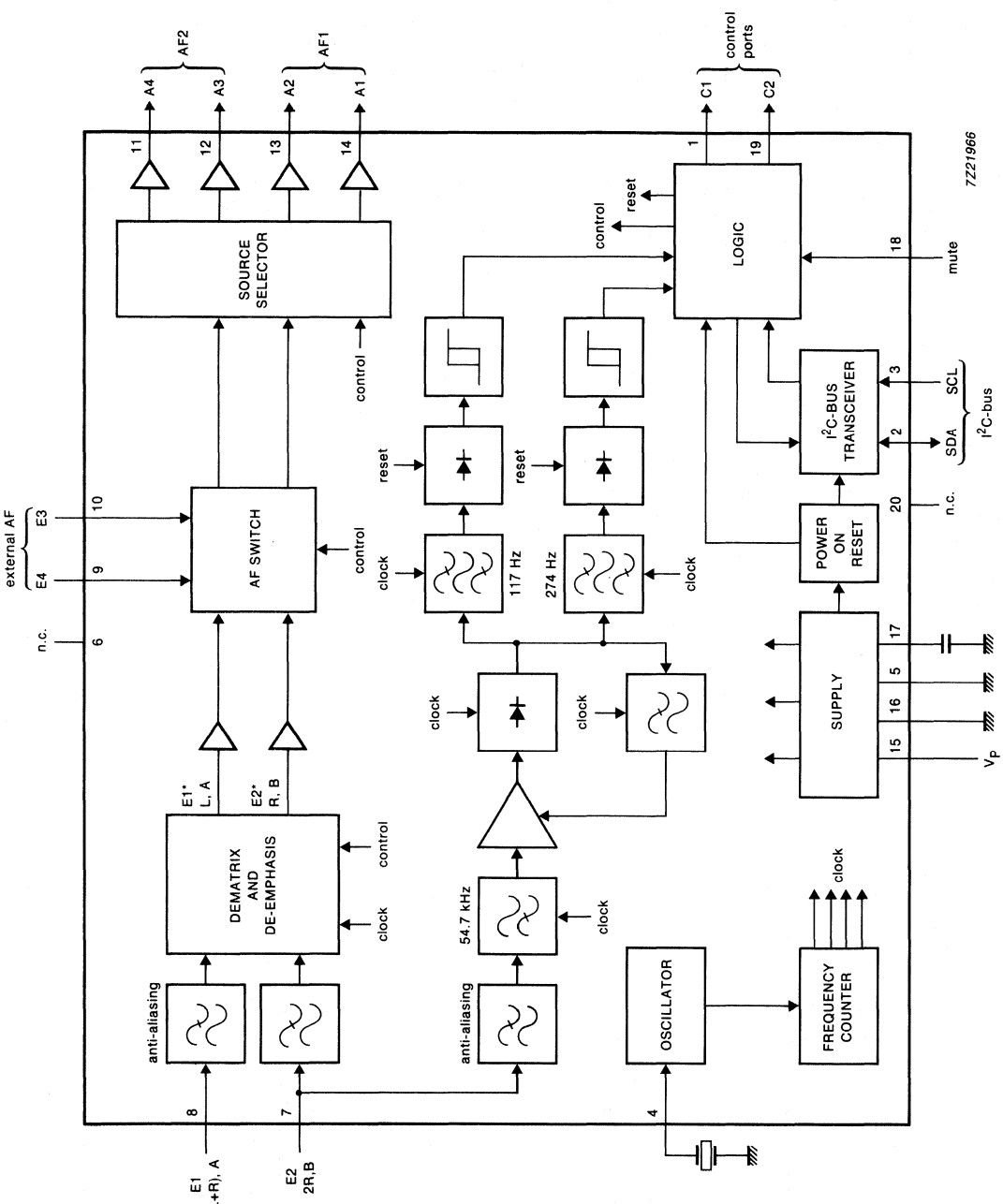


Fig.1 Block diagram.

DEVELOPMENT DATA

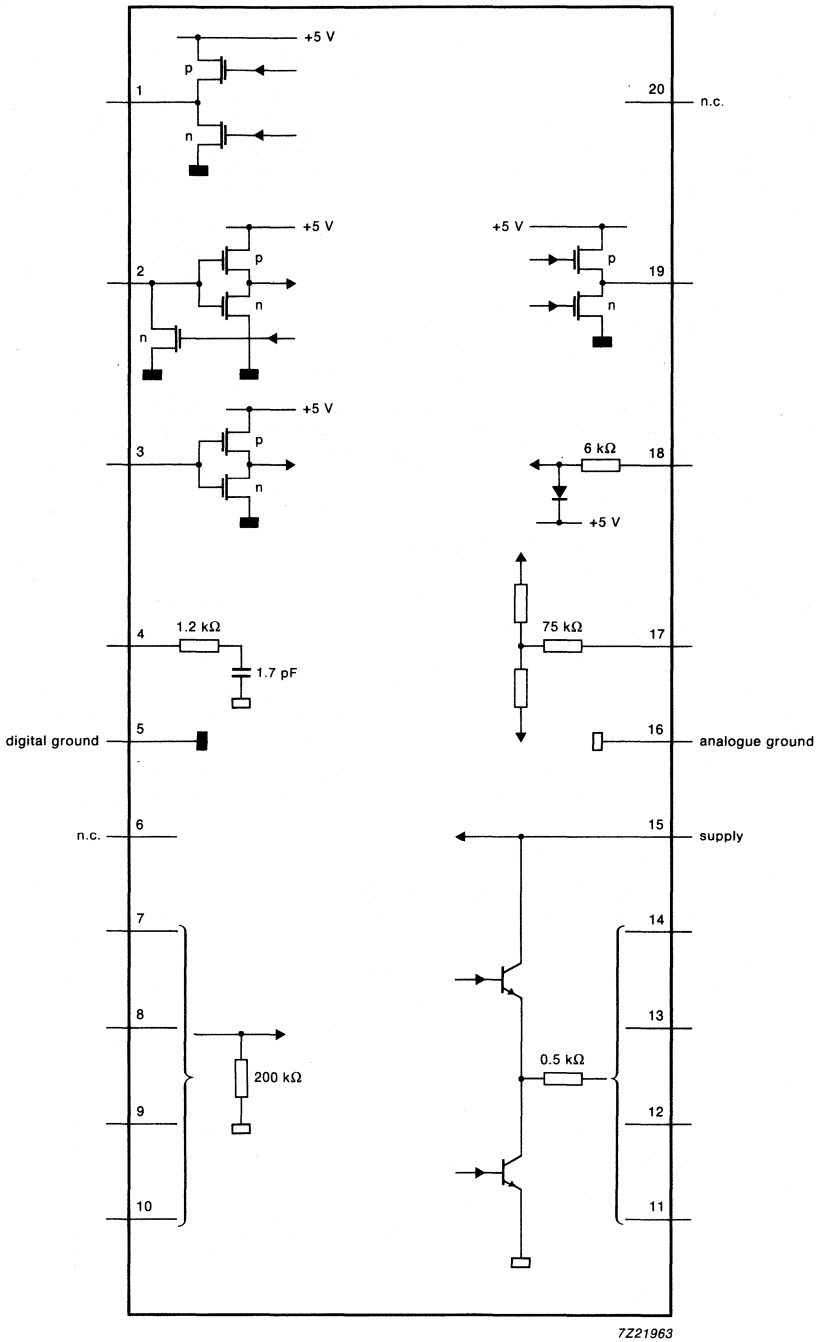


Fig.2 Input and output loading diagram.

PINNING

1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I^2C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I^2C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage V_P
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	External AF input (E3)	20	Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where L = left channel signal; R = right channel signal; A = first sound channel signal and B = second sound channel signal.

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

DEVELOPMENT DATA

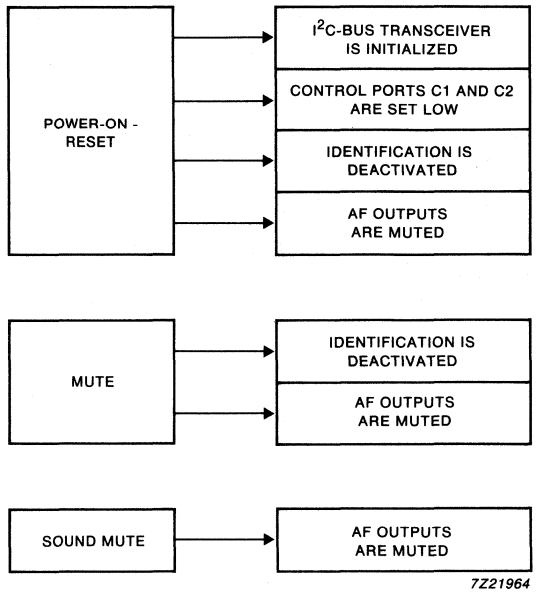


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8415 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

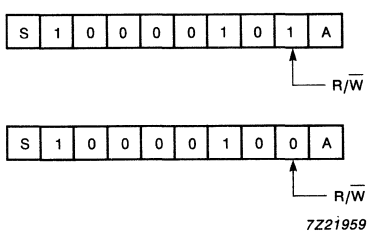
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8415

The TDA8415 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8415 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8415 is a slave transmitter)

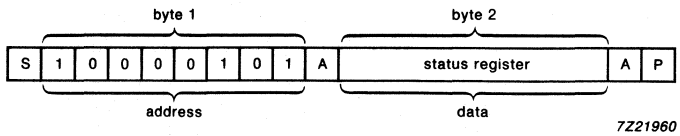
Write to (TDA8415 is a slave receiver)

Where S = start bit and A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8415

Reading the TDA8415 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

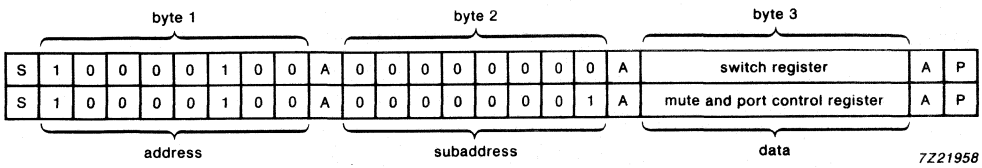
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission
1	1	not possible

Writing to the TDA8415

Writing to the TDA8415 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

DEVELOPMENT DATA

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where: X = don't care.

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)

Where: M = mono; St = stereo. DS = dual sound; R = right; L = left; L* = (L+R)/2; A = sound A; B = sound B.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)		500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

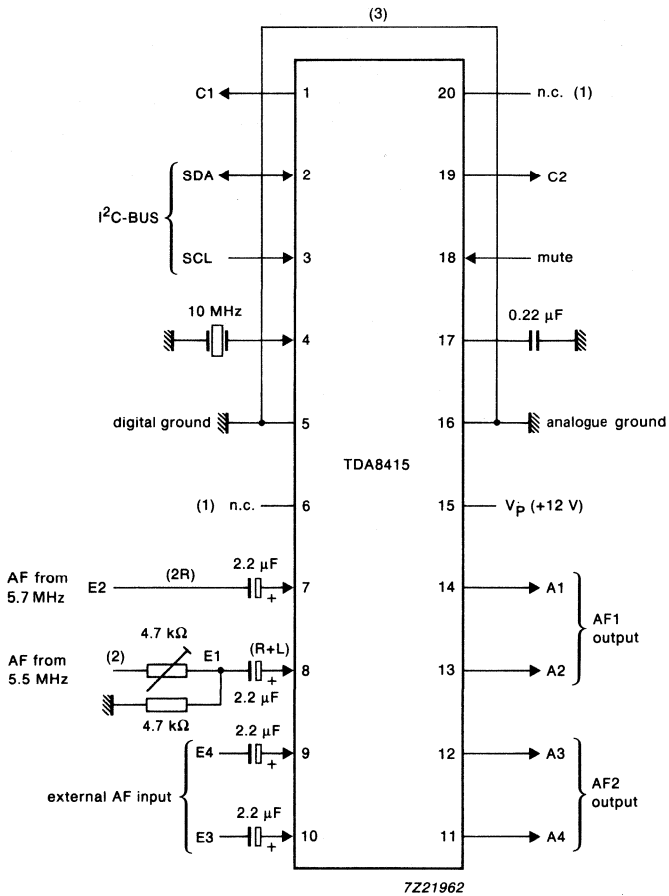
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. $f = 400$ Hz; $R_L = 1$ MΩ.
6. $40\ \text{Hz} \leqslant f \leqslant 15$ kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at $f = 3.183$ kHz.
10. $V_o = 1$ V RMS; $f = 1$ kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

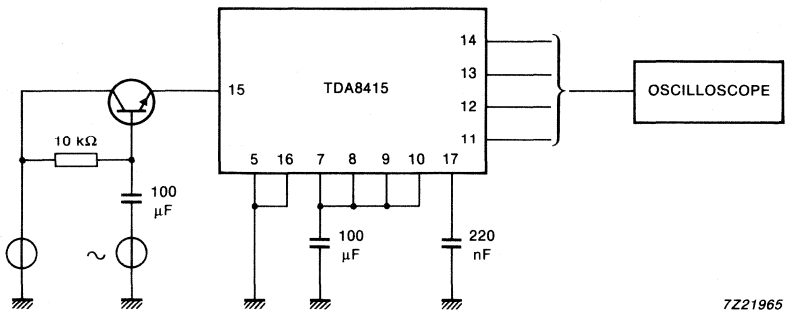


(1) These pins are not connected internally and should not be connected on the printed circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

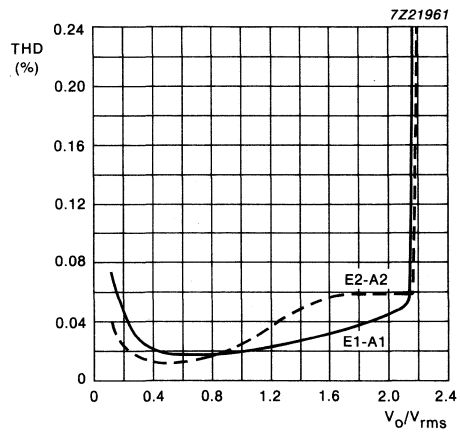


Fig.9 Total harmonic distortion diagram (stereo mode).

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8416 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8416 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation						
stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

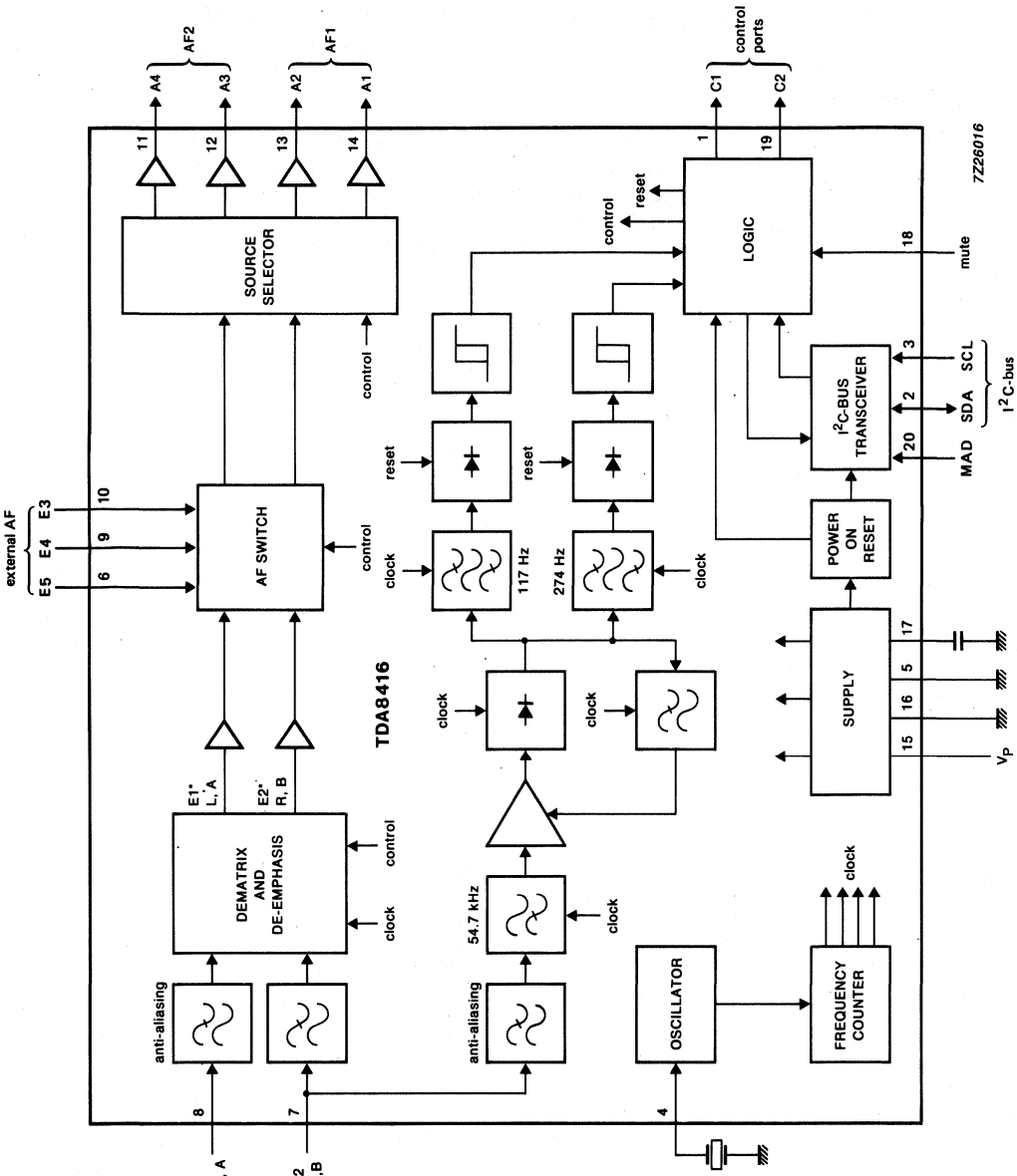


Fig.1 Block diagram.

DEVELOPMENT DATA

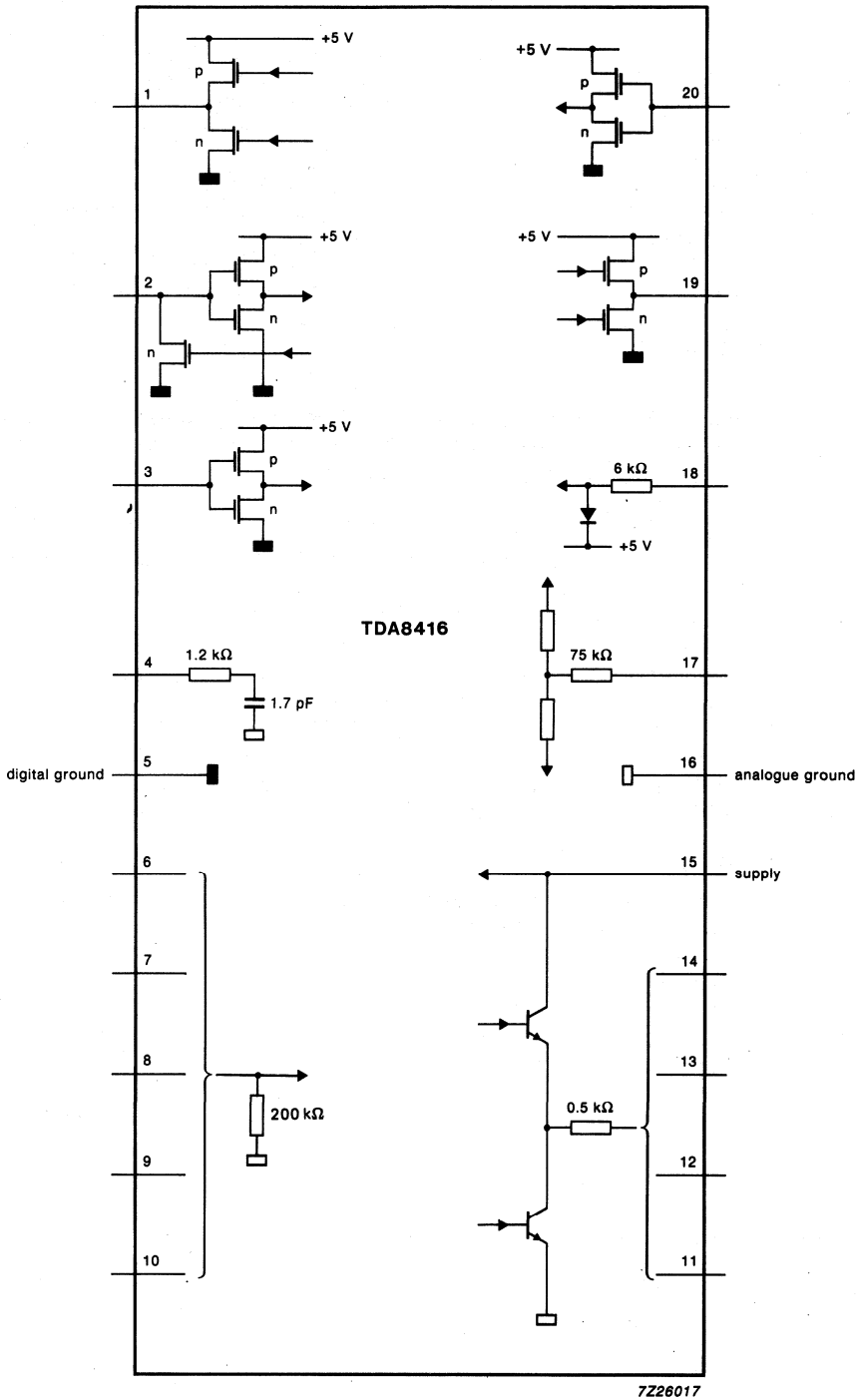


Fig.2 Input and output loading diagram.

PINNING

1 Control port C1
2 SDA, serial data line (I^2C-bus)
3 SCL, serial clock line (I^2C-bus)
4 Oscillator input (or quartz)
5 Digital ground (0 V)
6 External AF input (E5)
7 Sound channel input AF2 (E2)
8 Sound channel input AF1 (E1)
9 External AF input (E4)
10 External AF input (E3)
11 Output A4 AF 2 output
12 Output A3 AF 2 output
13 Output A2 AF 1 output
13 Output A1 AF 1 output
15 Supply voltage V_P
16 Analogue ground (0 V)
17 Ripple rejection improvement
18 Mute input
19 Control port C2
20 Module address (MAD)

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

FUNCTIONAL DESCRIPTION (continued)

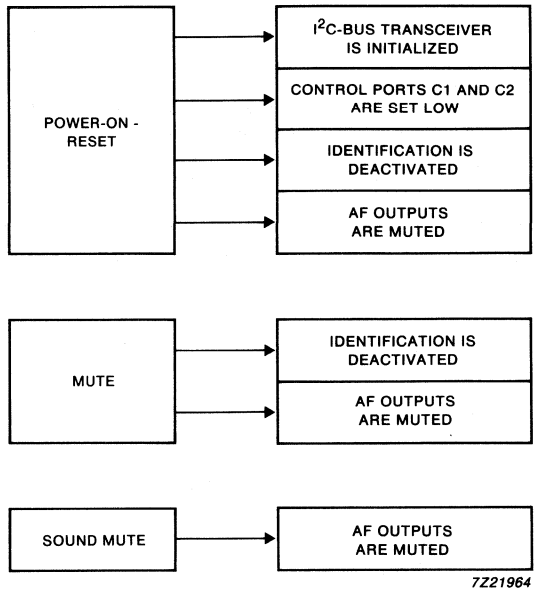


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8416 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

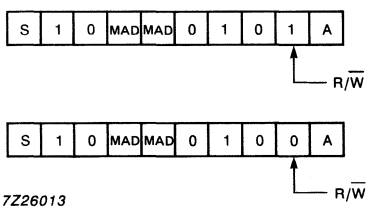
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8416

The TDA8416 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8416 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8416 is a slave transmitter)

Write to (TDA8416 is a slave receiver)

Where:

S = start bit
A = acknowledge bit
MAD = module address bit

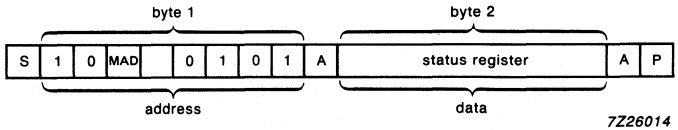
The MAD input (pin 20) allows the TDA8416 to operate from two different addresses:

MAD = LOW => A3 = A4 = 0 -> slave address = 1000 010
MAD = HIGH => A3 = A4 = 1 -> slave address = 1011 010

Fig.4 Address byte.

Reading the TDA8416

Reading the TDA8416 means reading the status register and the data stream will have the format as illustrated in Fig.5.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

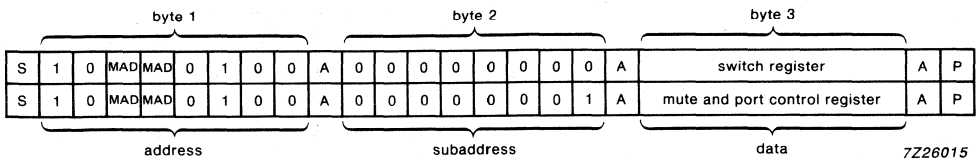
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8416

Writing to the TDA8416 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	E5	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	–	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	–	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	–	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	–	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	–	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	–	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	–	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	–	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	–	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)
	–	–	–	–	–	E5	E5	E5	E5	E5	1	0	0	0	0	0	0	0	(80)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 6 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA
MAD (pin 20)						
Input voltage LOW		V_{20-5}	–	–	2.0	V
Input voltage HIGH		V_{20-5}	3.0	–	–	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 6, 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

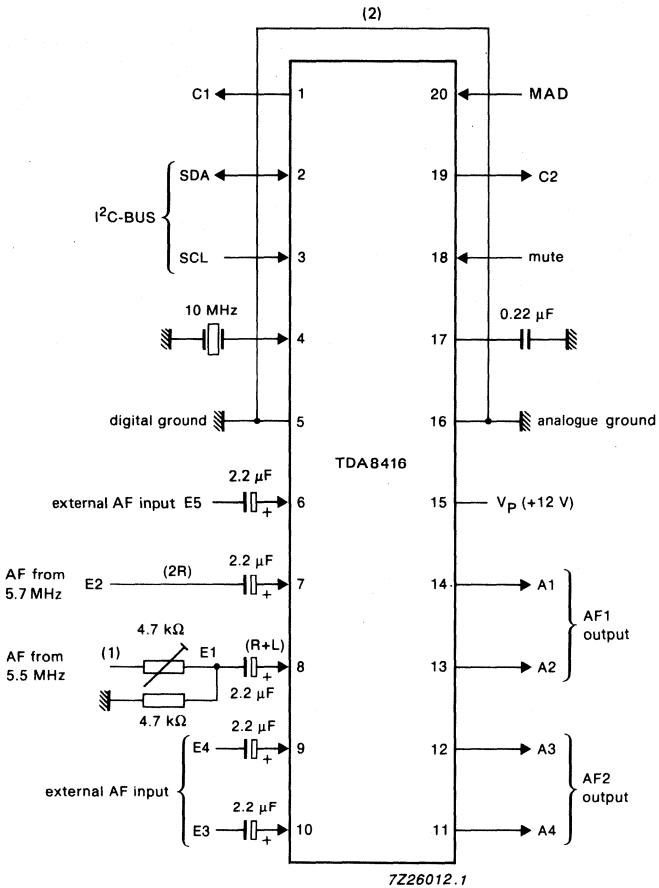
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; $R_L = 1$ MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. $V_o = 1$ V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

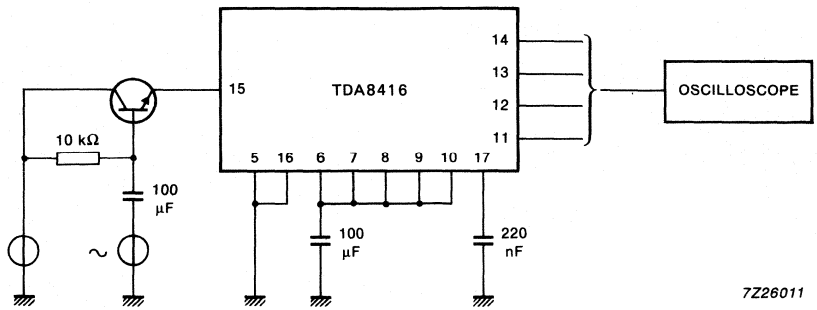
DEVELOPMENT DATA



(1) This potentiometer has to be adjusted to achieve the best stereo separation.

(2) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

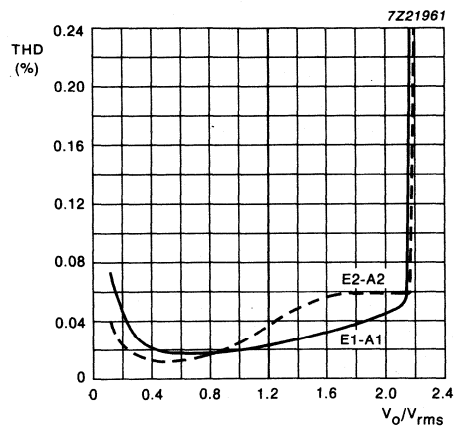


Fig.9 Total harmonic distortion diagram (stereo mode).

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8417 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8417 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation						
stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

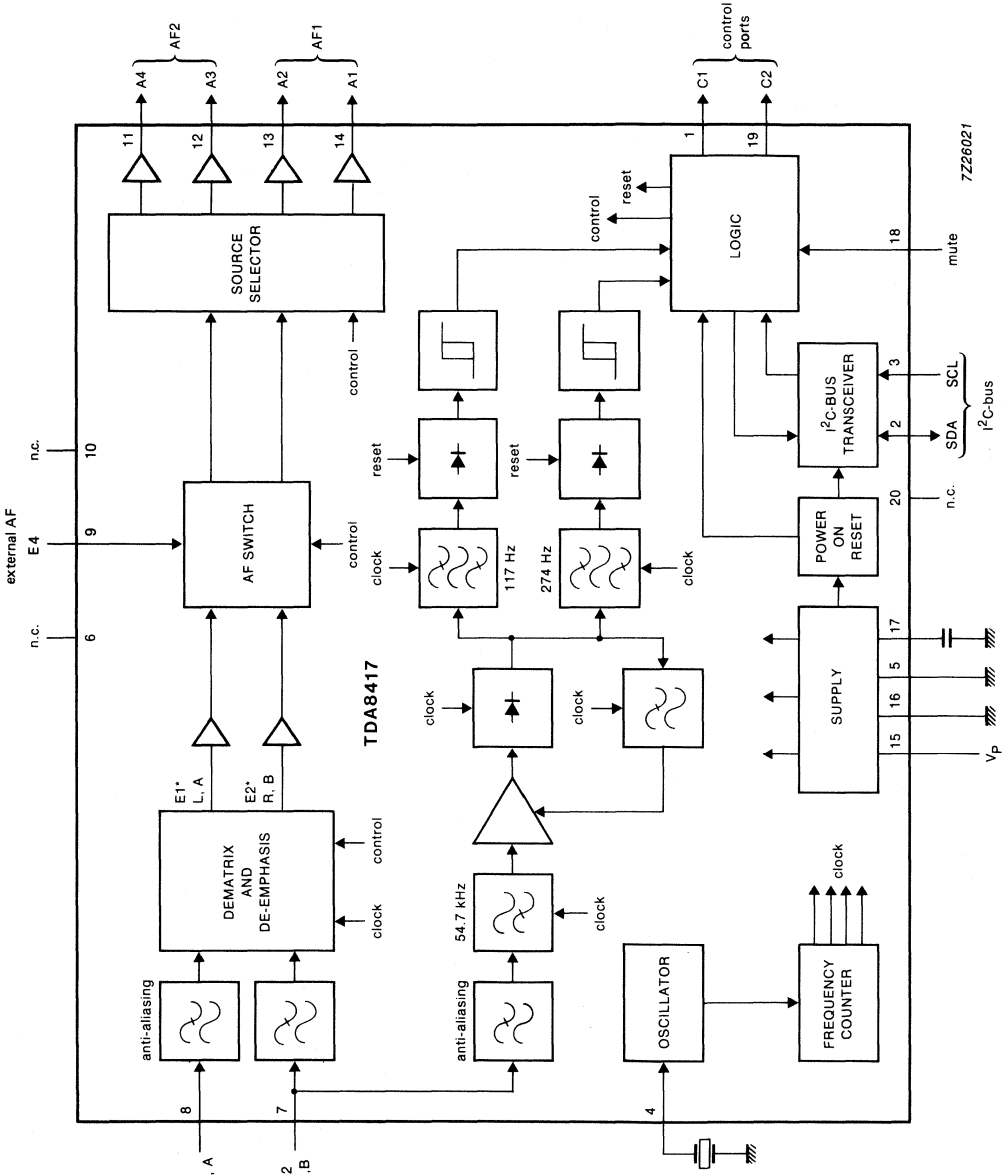


Fig.1 Block diagram.

DEVELOPMENT DATA

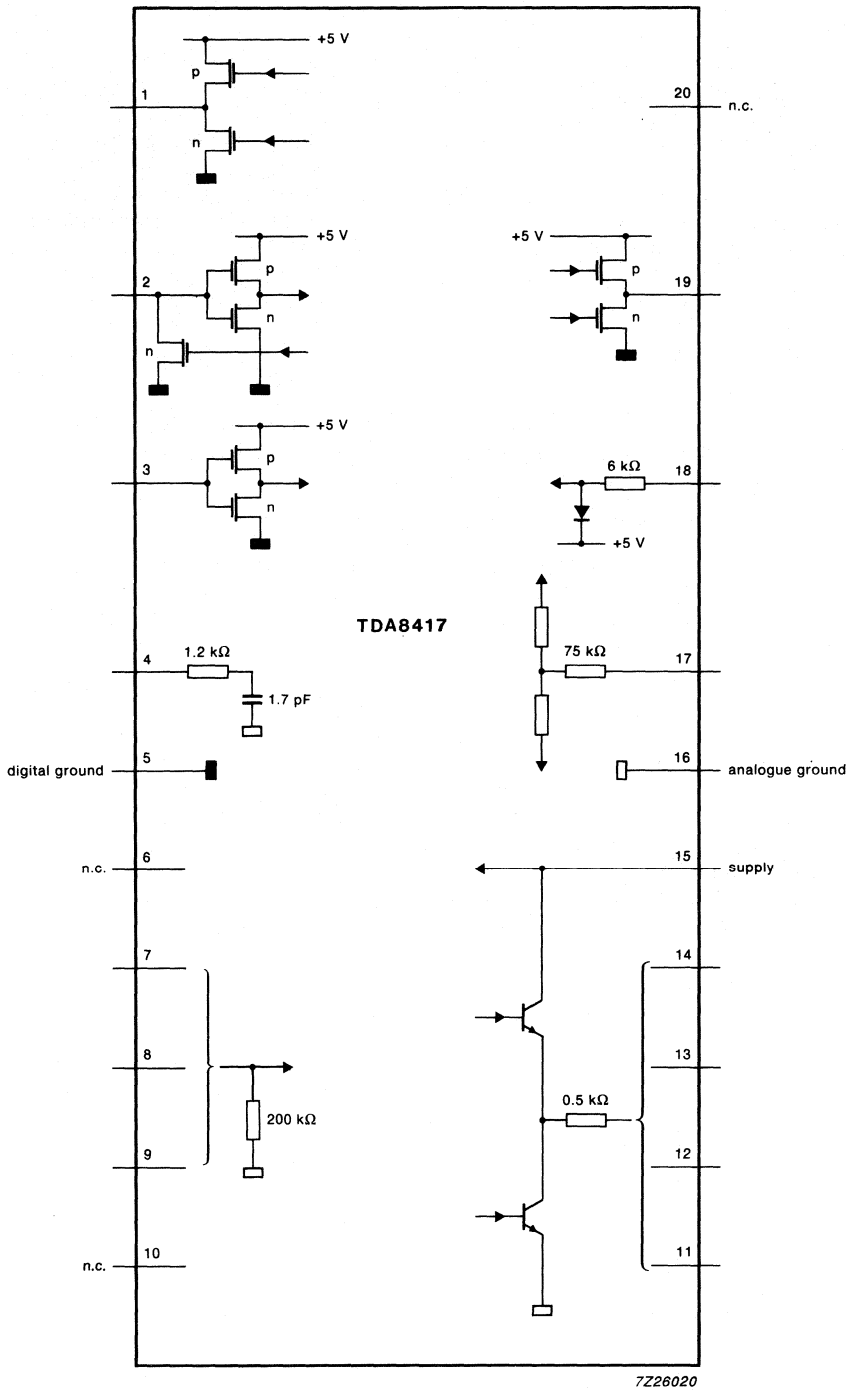


Fig.2 Input and output loading diagram.

PINNING

1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I^2C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I^2C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage V_P
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	Not connected, but reserved	20	Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

FUNCTIONAL DESCRIPTION (continued)

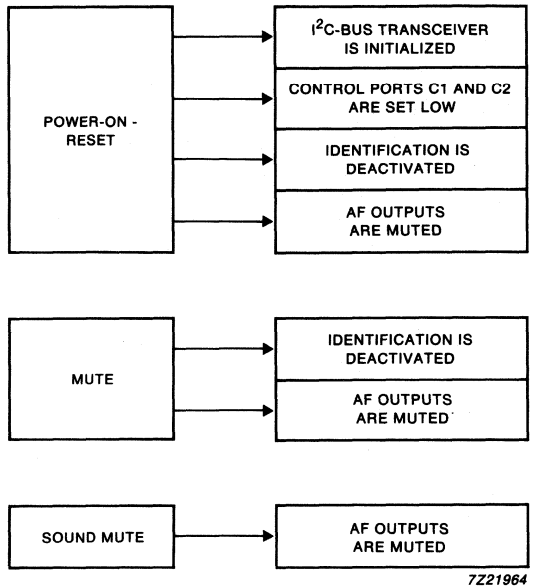


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8417 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

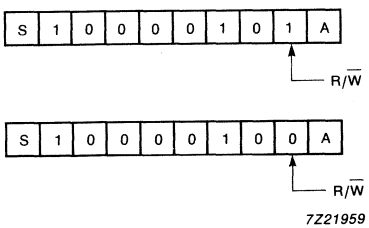
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8417

The TDA8417 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8417 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8417 is a slave transmitter)

Write to (TDA8417 is a slave receiver)

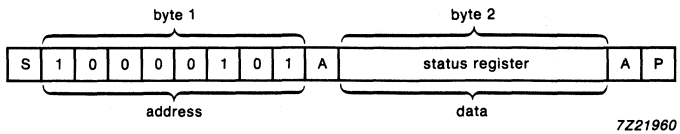
Where:

S = start bit
A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8417

Reading the TDA8417 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

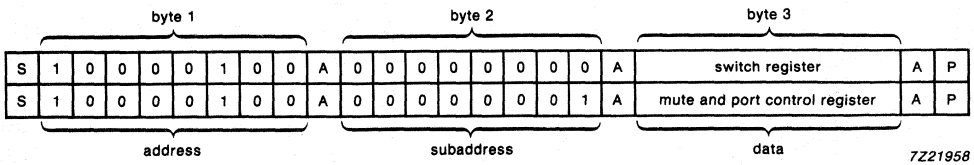
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8417

Writing to the TDA8417 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.6 Write format.

DEVELOPMENT DATA

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 9)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

DEVELOPMENT DATA

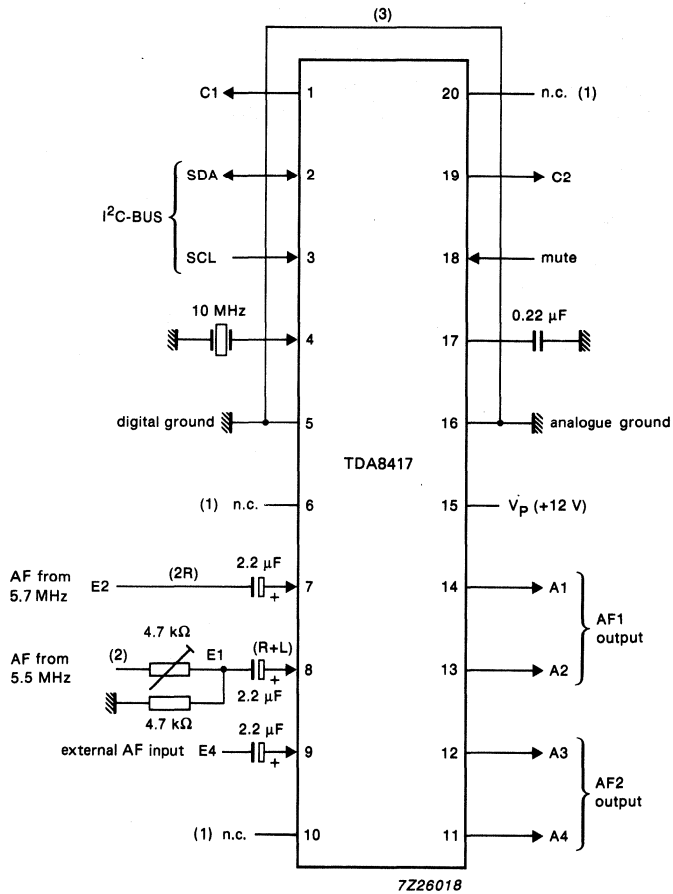
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; $R_L = 1$ MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. $V_O = 1$ V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

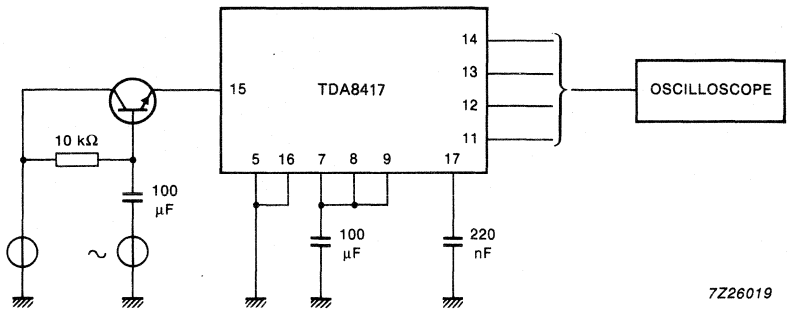


(1) These pins are not connected internally and should not be connected on the printed-circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

DEVELOPMENT DATA

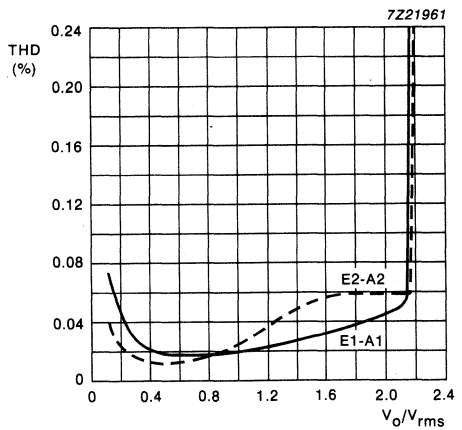


Fig.9 Total harmonic distortion diagram (stereo mode).

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8420 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−46	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

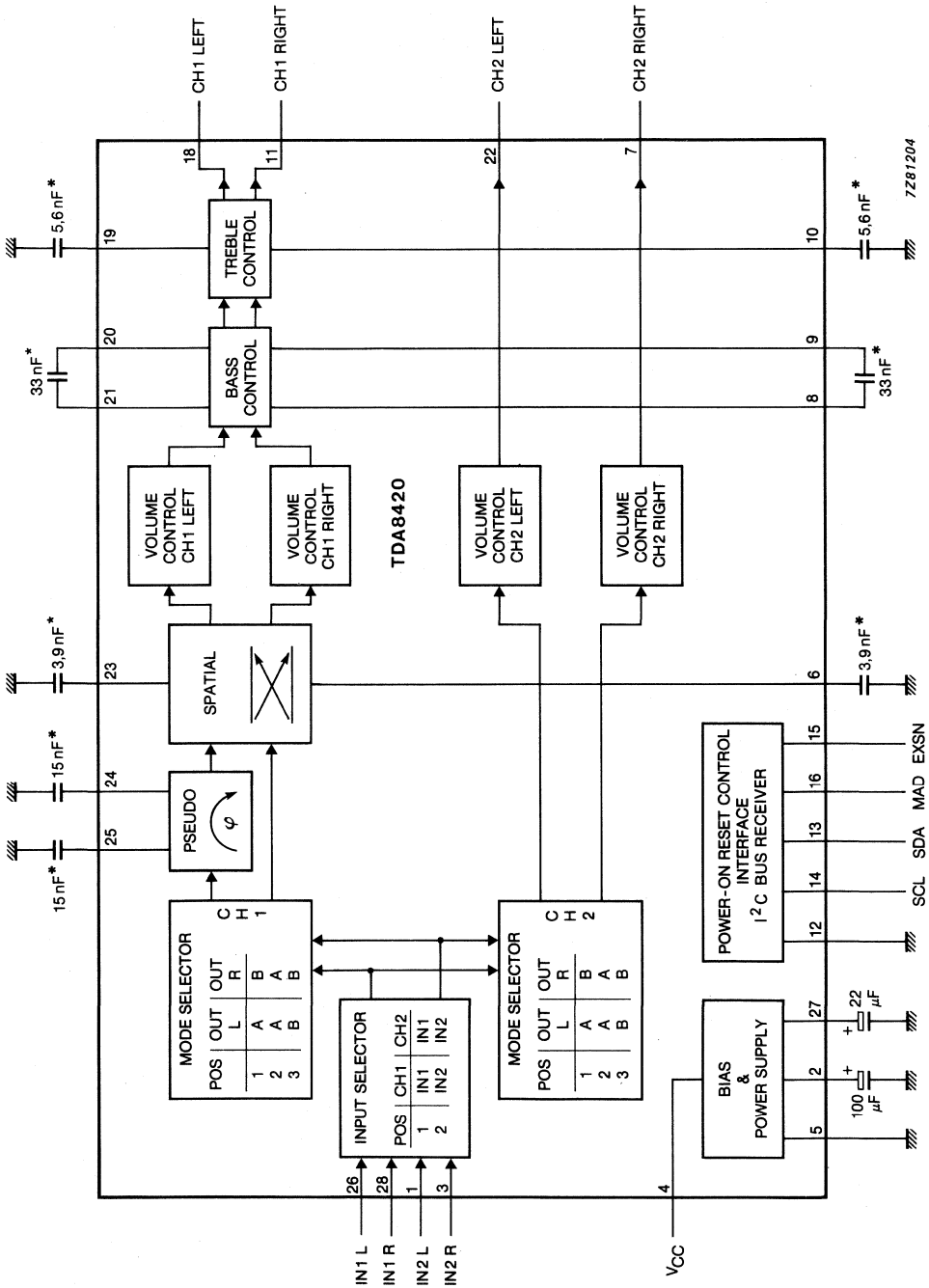


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

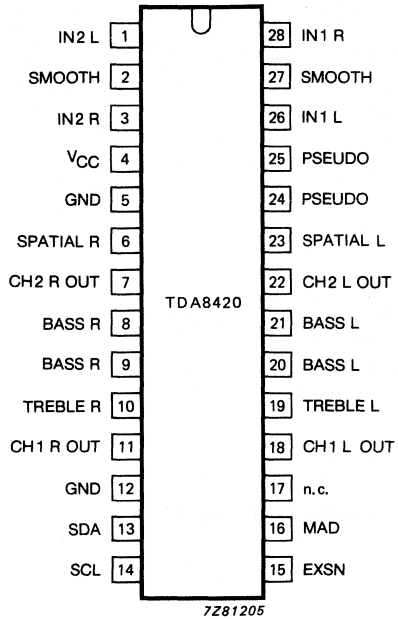


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8420 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8420 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8420 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8420 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8420s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8420. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8420. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Where: POR = Power-On Reset.

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	Vx5	Vx4	Vx3	Vx2	Vx1	Vx0
16	0	1	1	1	1	1	1
–46	–62	1	0	0	0	0	0
$\leqslant$ –90	$\leqslant$ –90	0	1	1	1	1	1
$\leqslant$ –90	$\leqslant$ –90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation $\geqslant$ 90 dB.

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

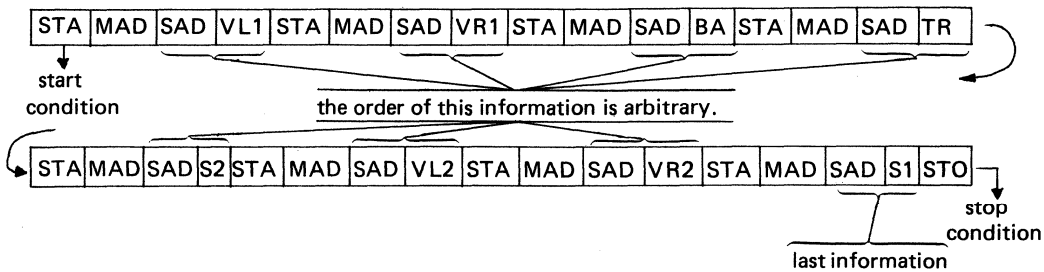


Fig. 4 Data transmission after a power-on reset.

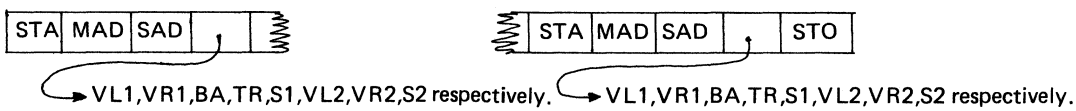


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Input voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I	0	V_{CC}	V
Output voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	150	°C

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Input voltage					
IN1 L, IN1 R, IN2 L, IN2 R					
DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage					
CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
External capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15)					
at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value)					
at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level					
weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = ⩽ −90 dB	V_n	–	15	–	μV
Total harmonic distortion					
(f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V;					
gain = + 16 dB to −30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V;					
gain = + 2 dB to −30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V;					
gain = −4 dB to −30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz					
gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB;					
bass and treble in linear position)					
f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic					
inputs to AF outputs (gain = 0 dB;					
bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–46 dB step)	G_{min}	–43	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –46 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for C_{10-5}; C_{19-5} = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for C_{8-9}; C_{20-21} = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift			(see Fig. 15)		

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ −90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to −30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to −30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = −4 dB to −30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.

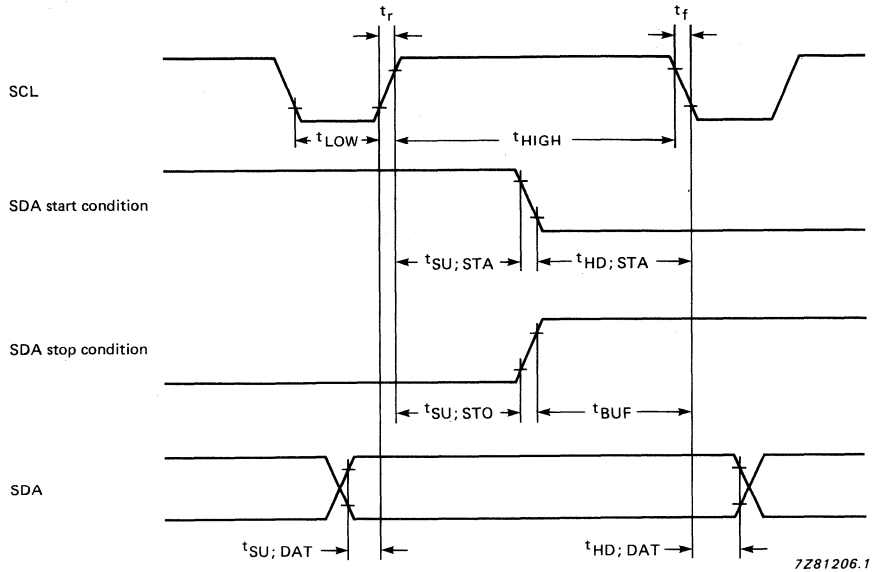


Fig. 6 Timing requirements for I^2C bus.

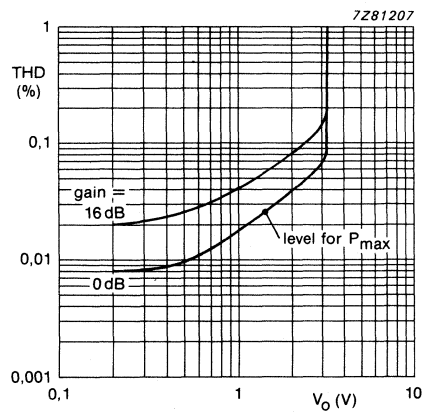


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

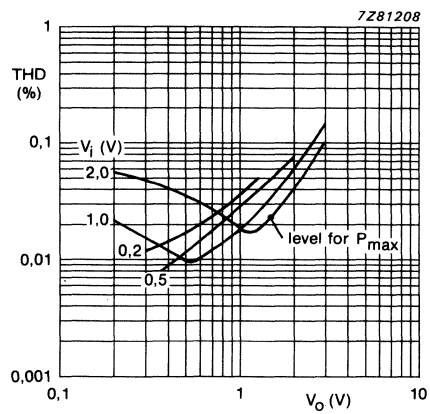


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

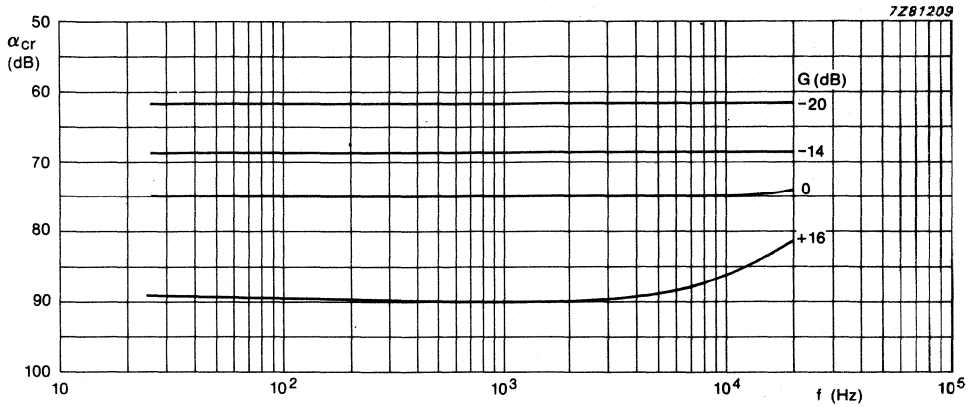


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

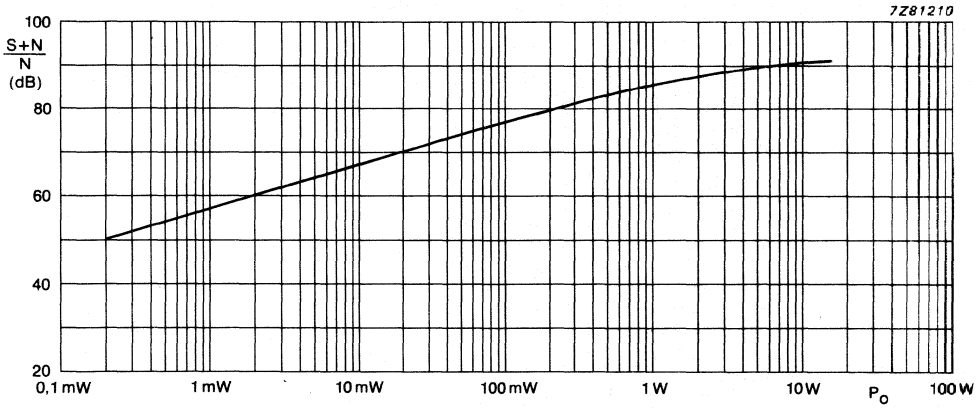


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

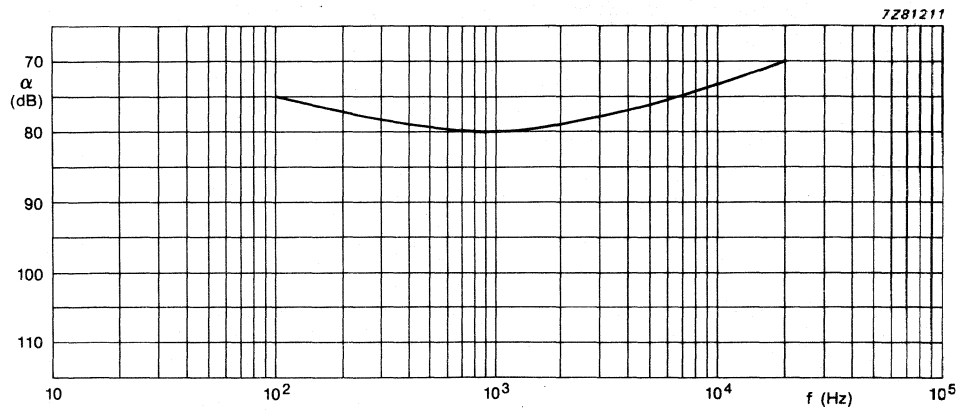


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

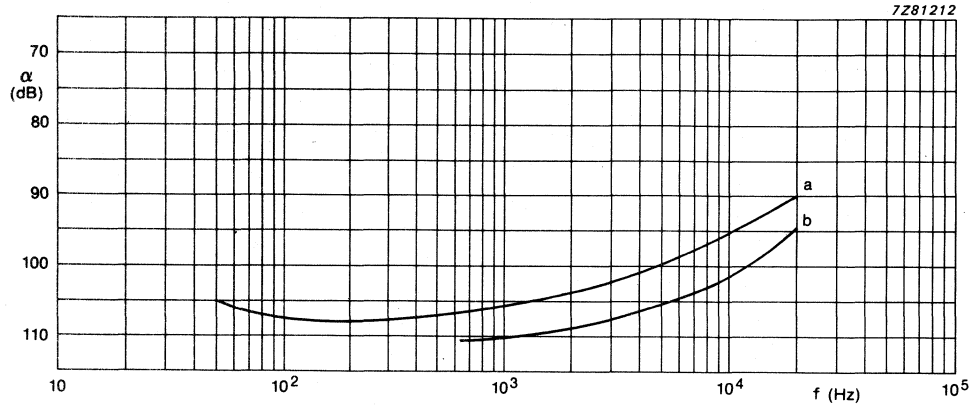


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

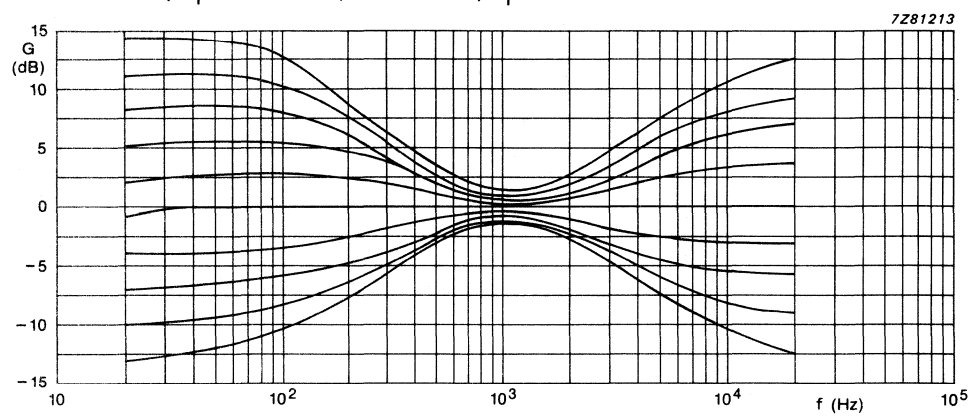


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

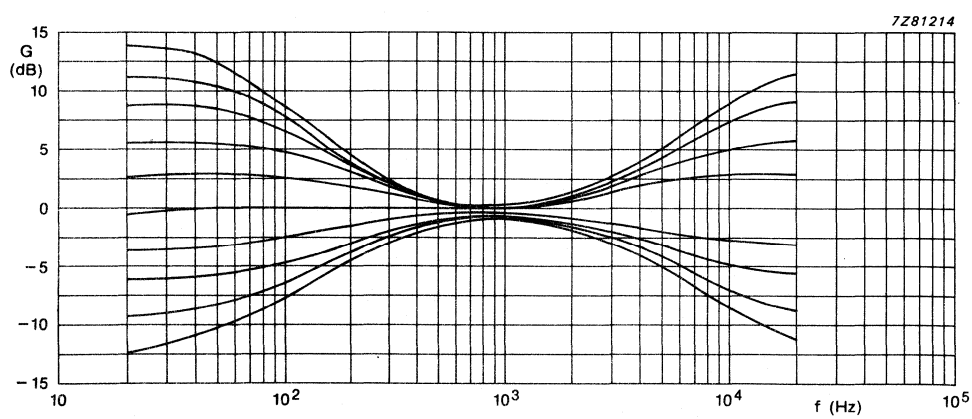
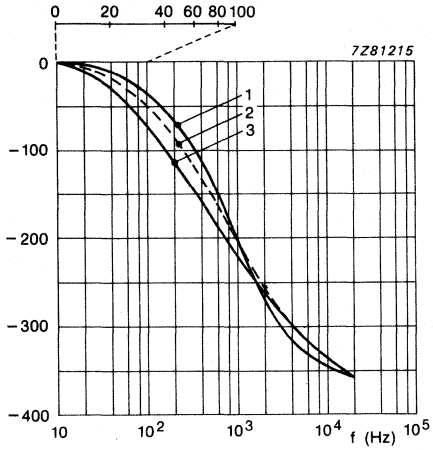


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	C_{24} (nF)	C_{25} (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

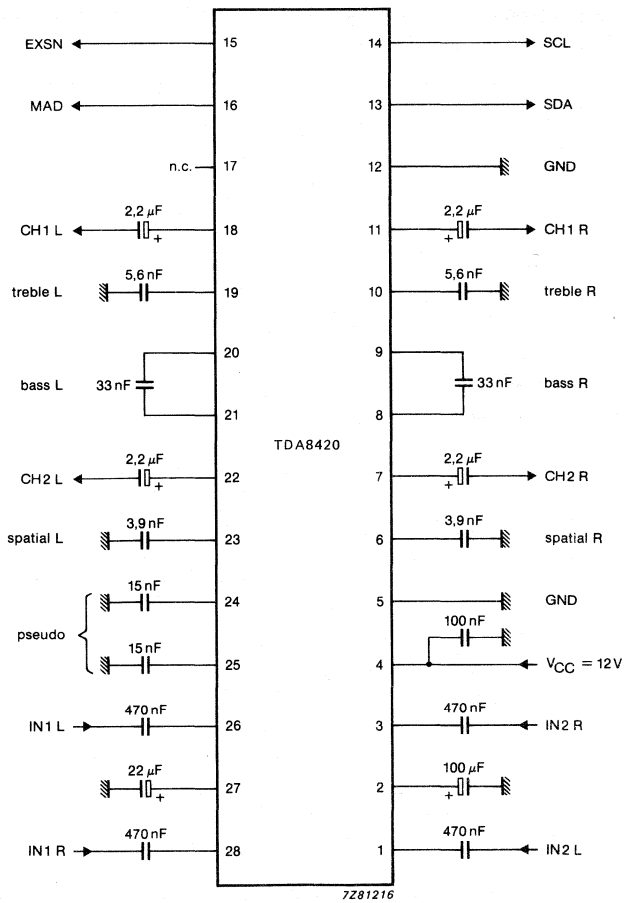
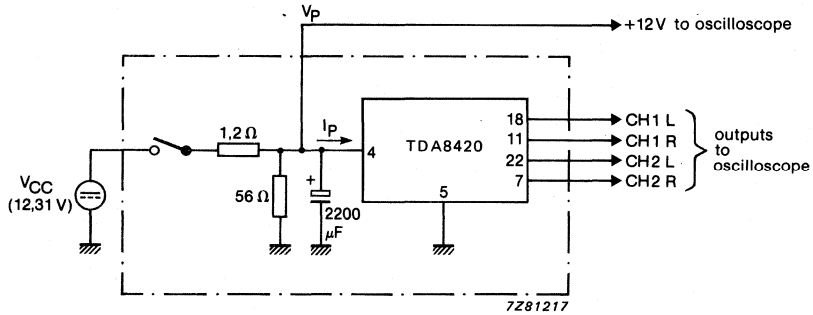


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

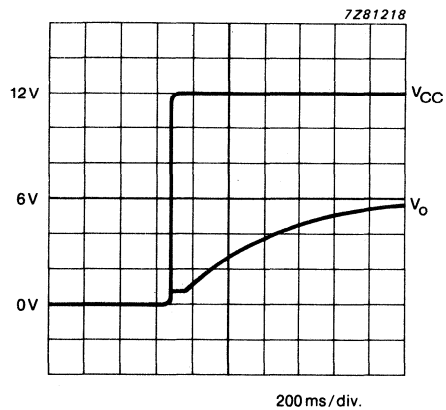


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

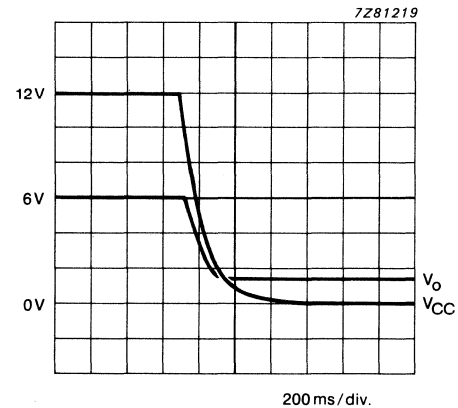


Fig. 19 Turn-off behaviour;
without modulation.

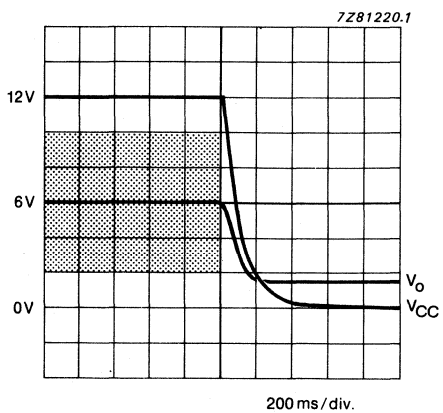


Fig. 20 Turn-off behaviour; with modulation (shaded area).

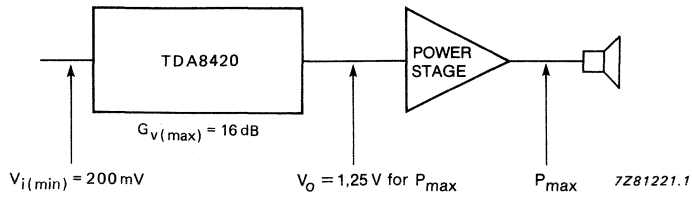


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

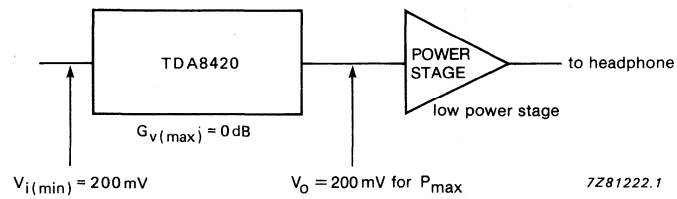


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

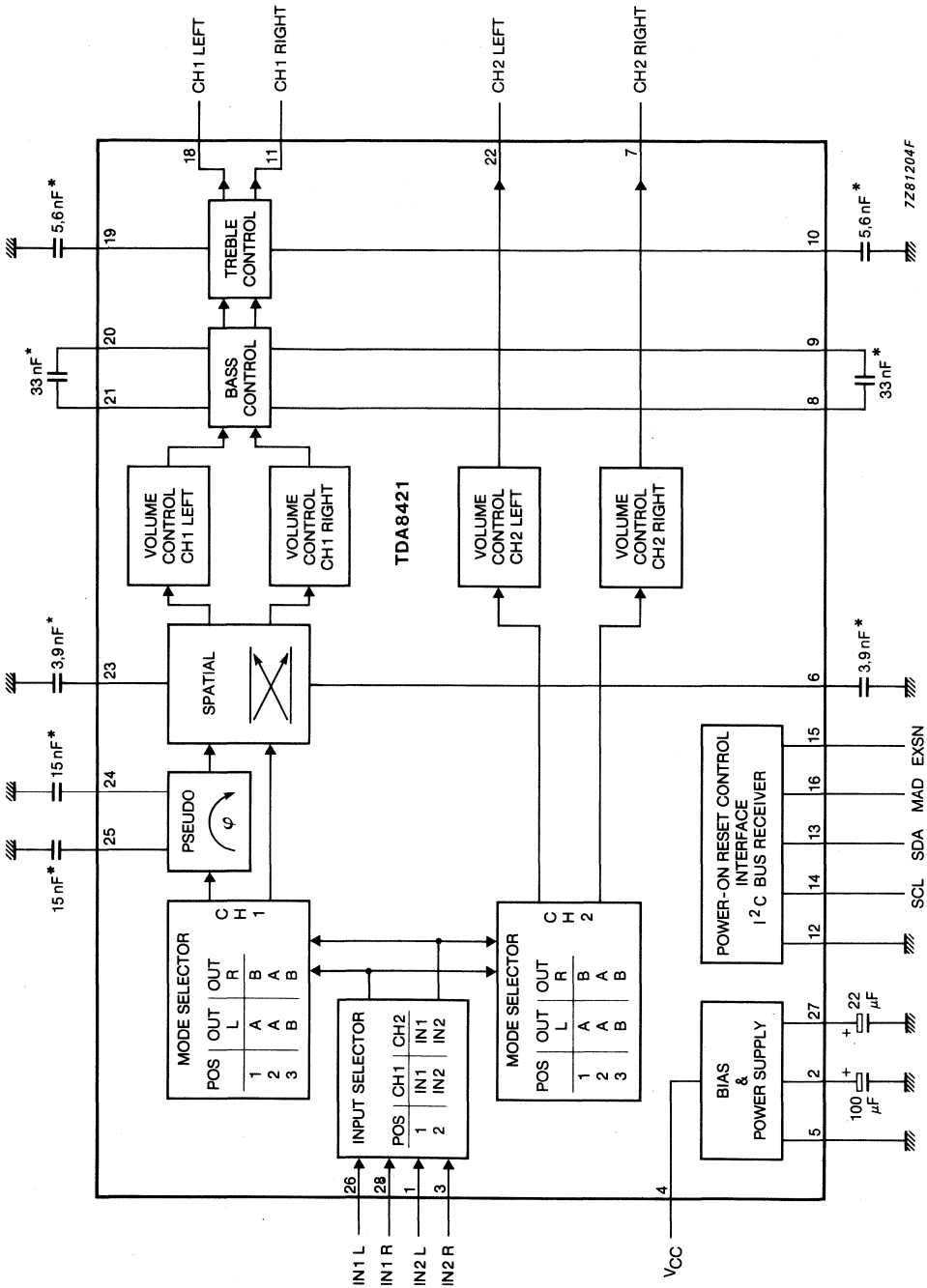


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

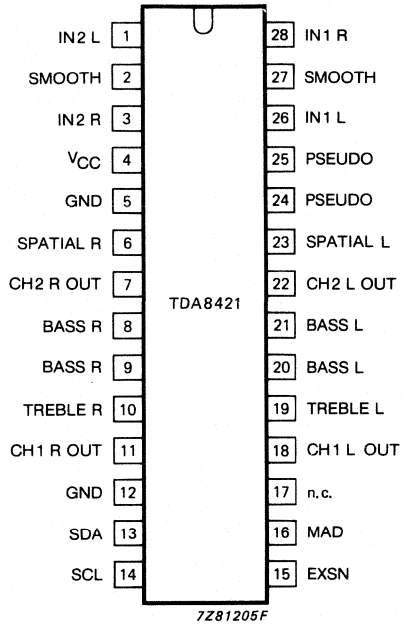


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

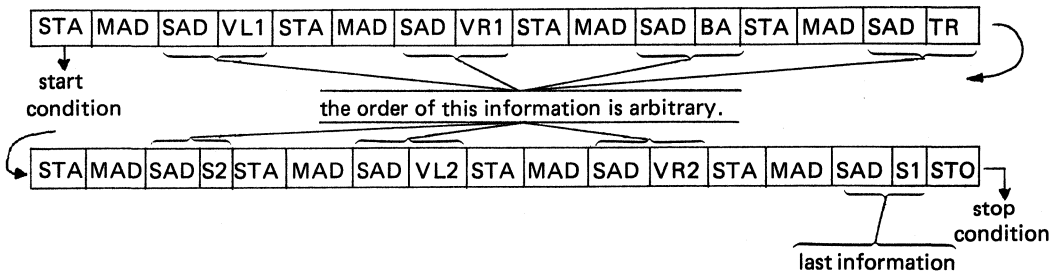


Fig. 4 Data transmission after a power-on reset.

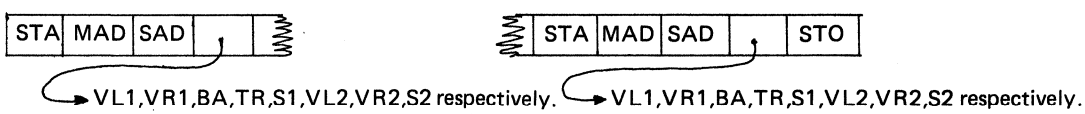


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−25	150	°C
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift (see Fig. 15)					

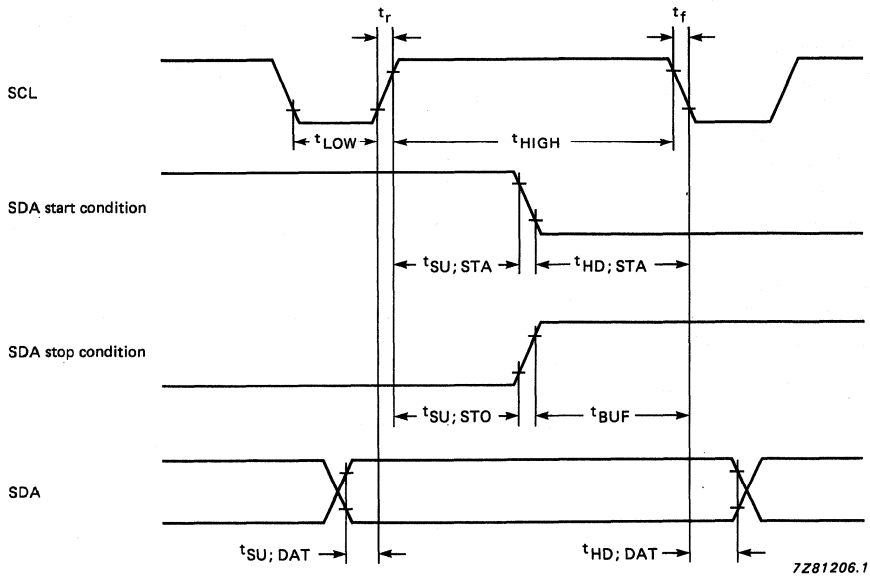
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = $\leqslant$ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time
t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

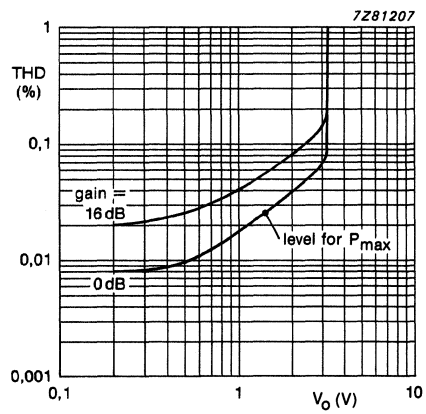


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

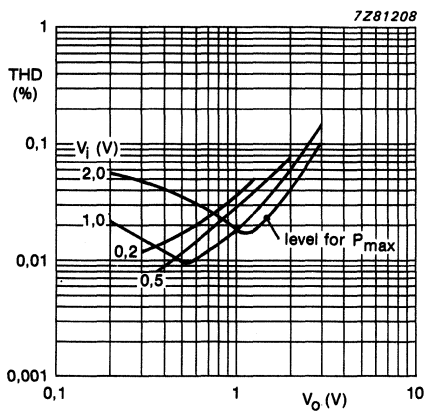


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

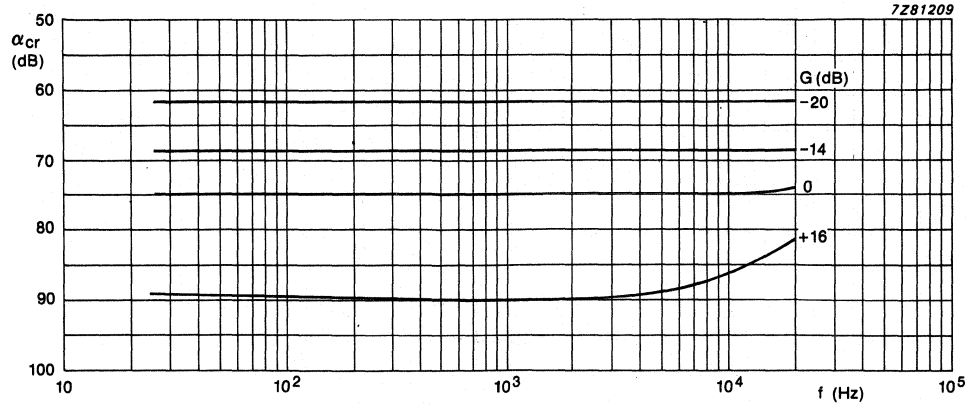


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

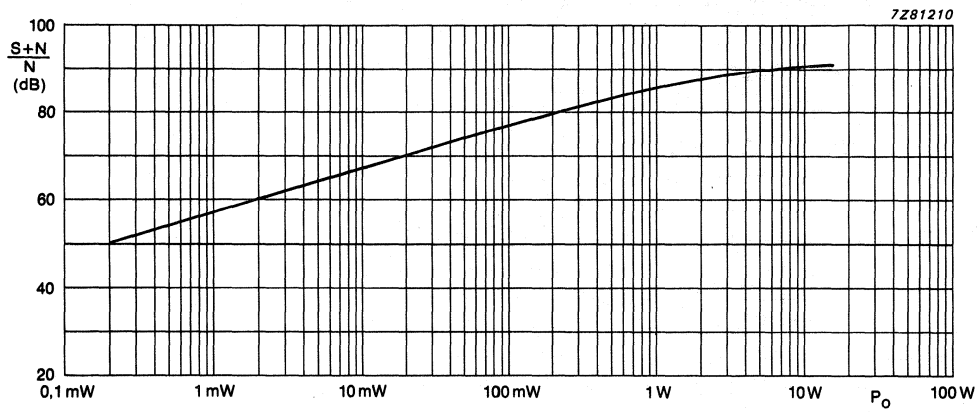


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

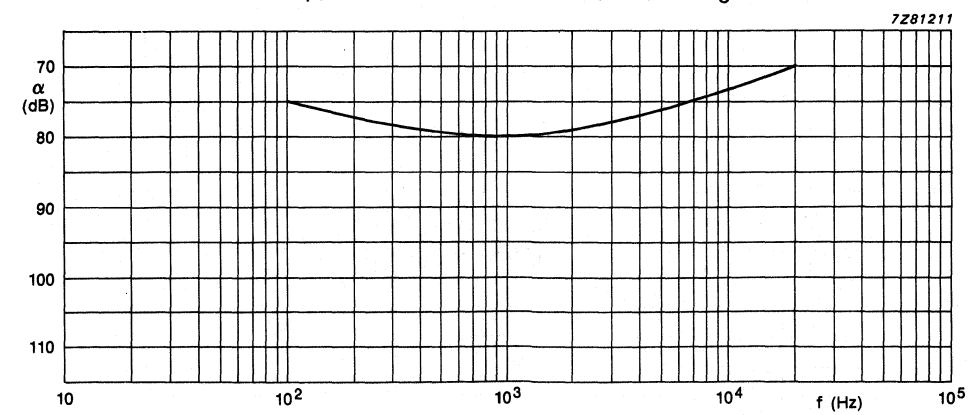


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

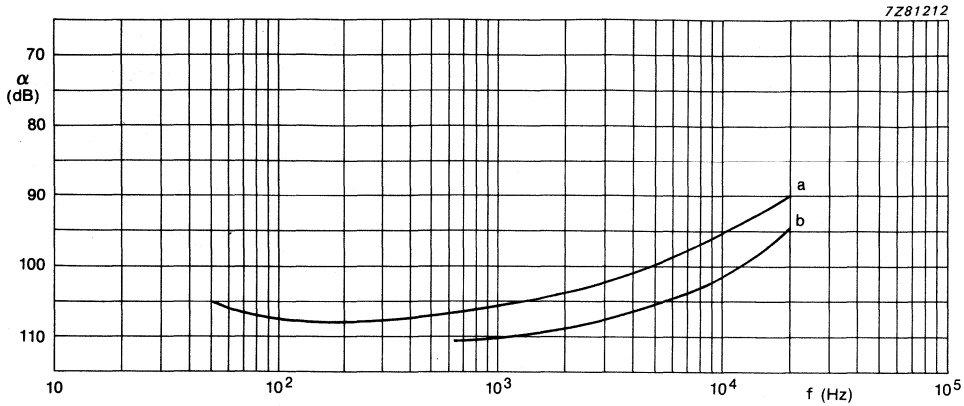


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

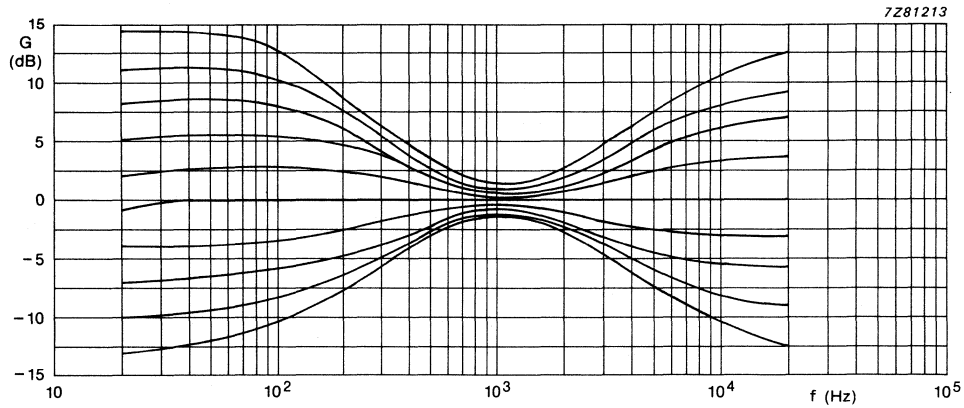


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

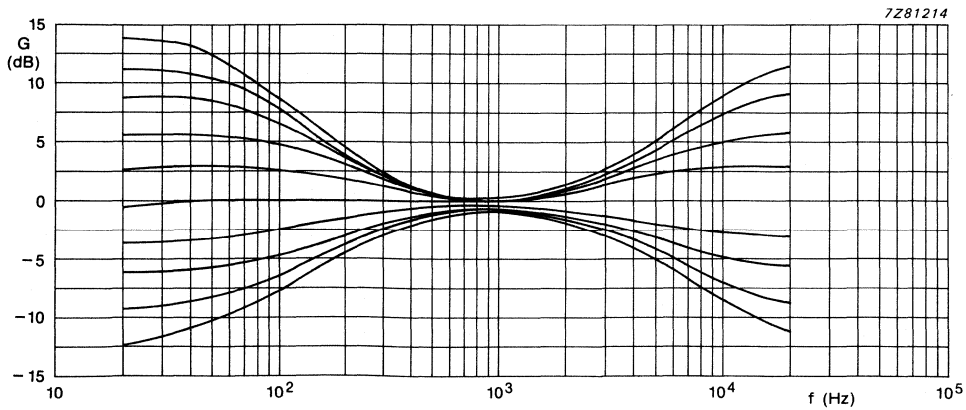
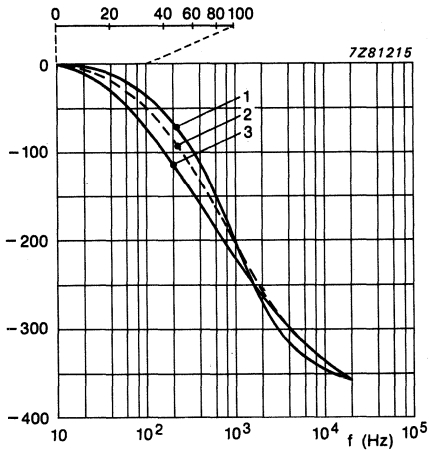


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

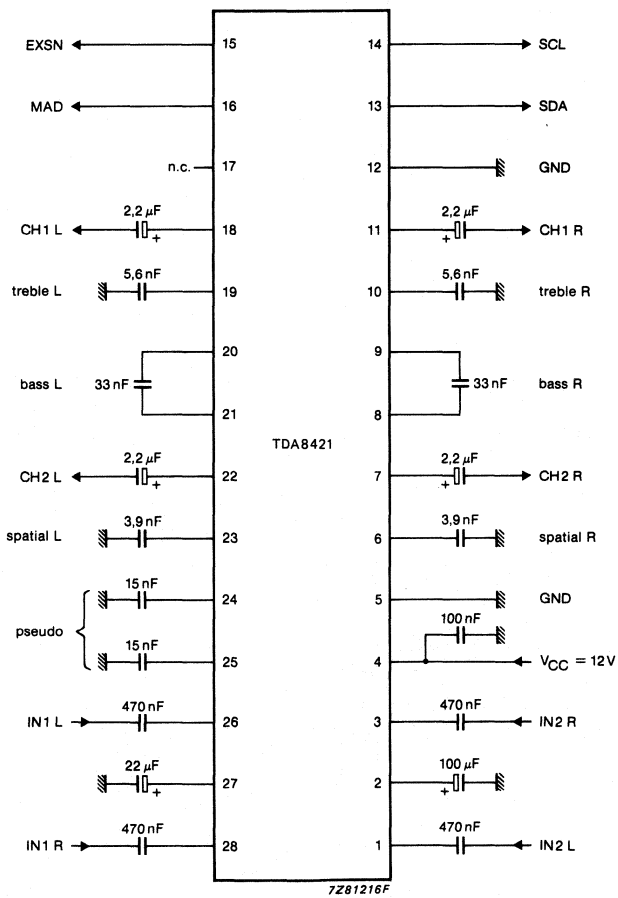
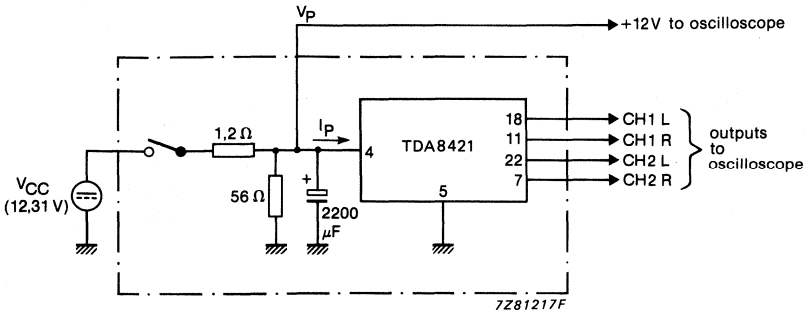


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

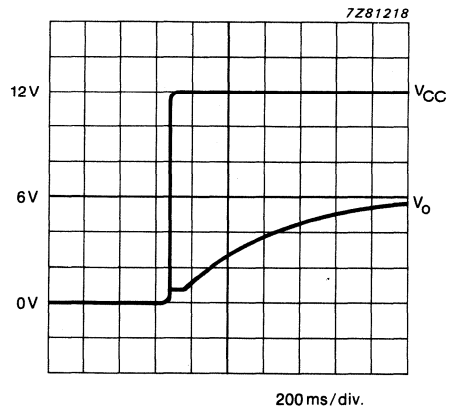


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

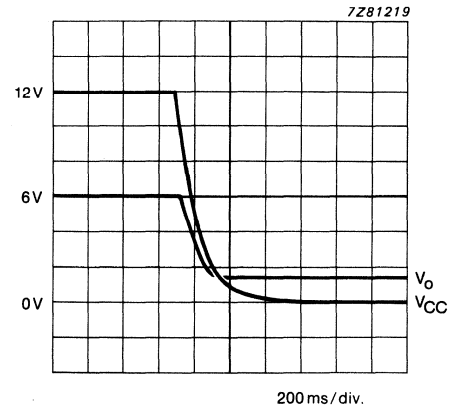


Fig. 19 Turn-off behaviour;
without modulation.

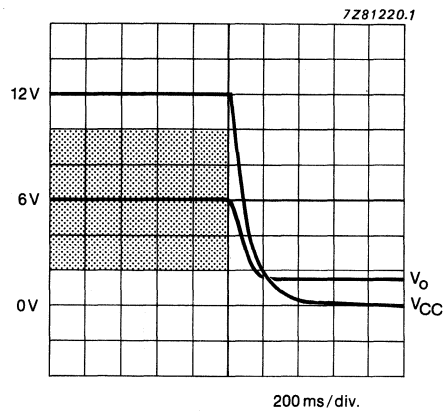


Fig. 20 Turn-off behaviour; with modulation (shaded area).

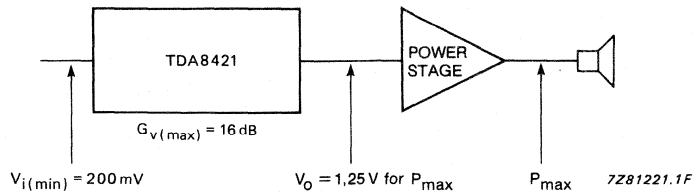


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

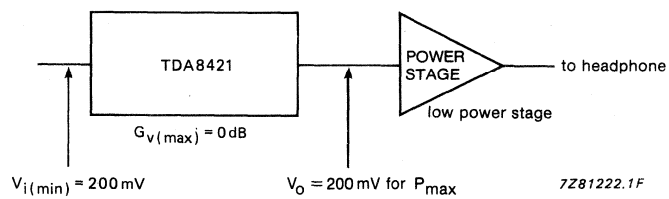


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	−64	–	6	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

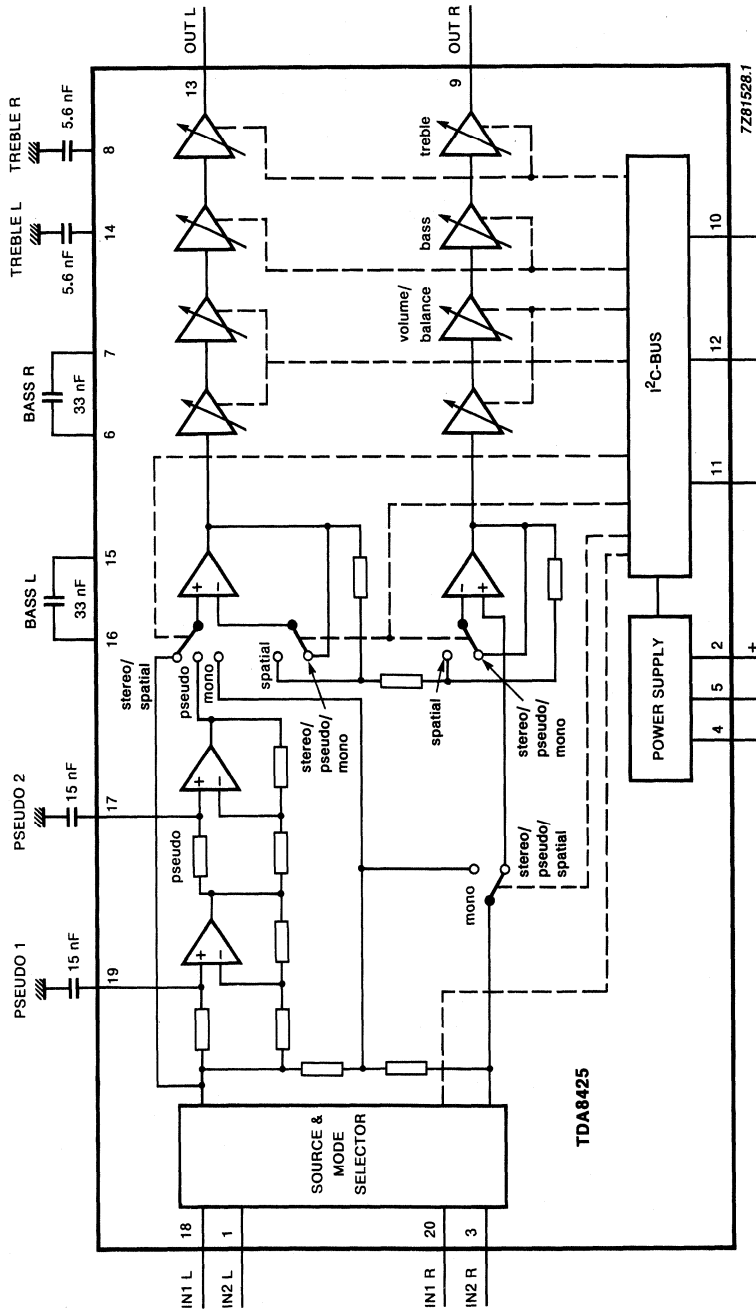


Fig. 1 Block diagram.

PINNING

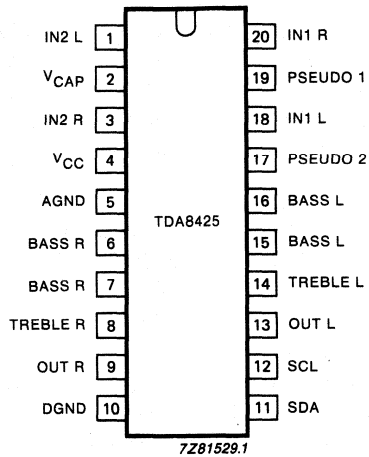


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of ⩾ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of 0.5 x V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

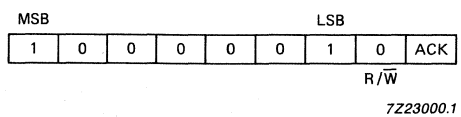


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
–62	0	1	1	1	0	1
–64	0	1	1	1	0	0
⩽ –80	0	1	1	0	1	1
⩽ –80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

DEVELOPMENT DATA

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

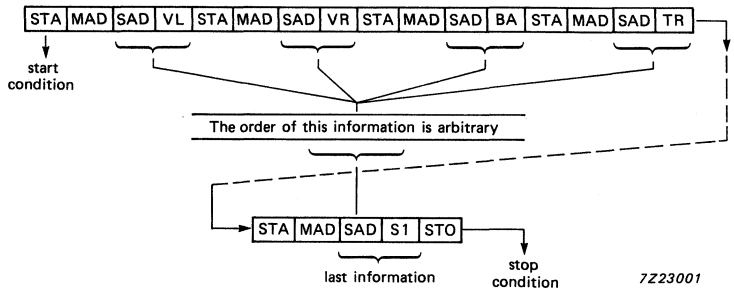


Fig. 4 Data transmission after a power-on reset.

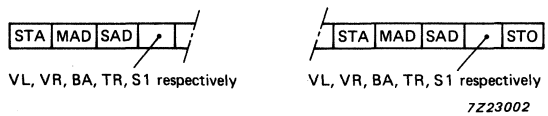


Fig. 5 Data transmission after a power-on reset with auto increment.

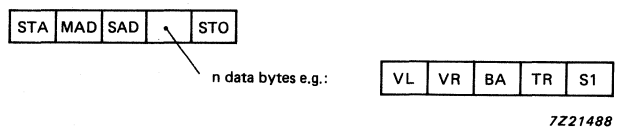


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C
Electrostatic handling, classification A*				

DEVELOPMENT DATA

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10$ kΩ; $C_L < 1000$ pF; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)}$ ⩽ 2 V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

AC CHARACTERISTICS (continued)

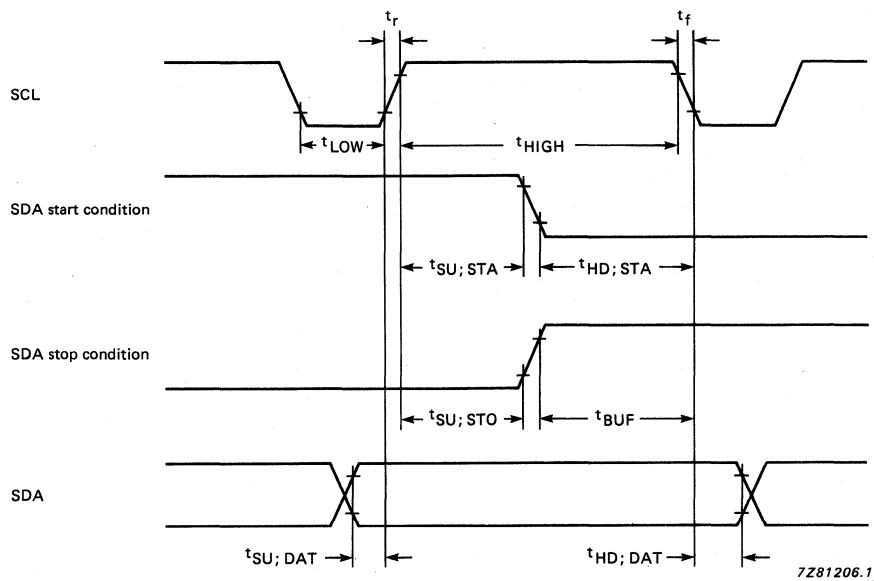
parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

DEVELOPMENT DATA

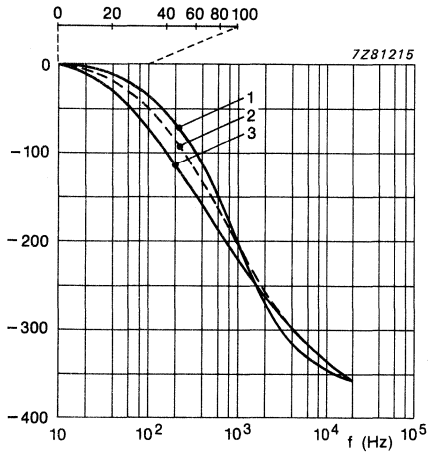
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

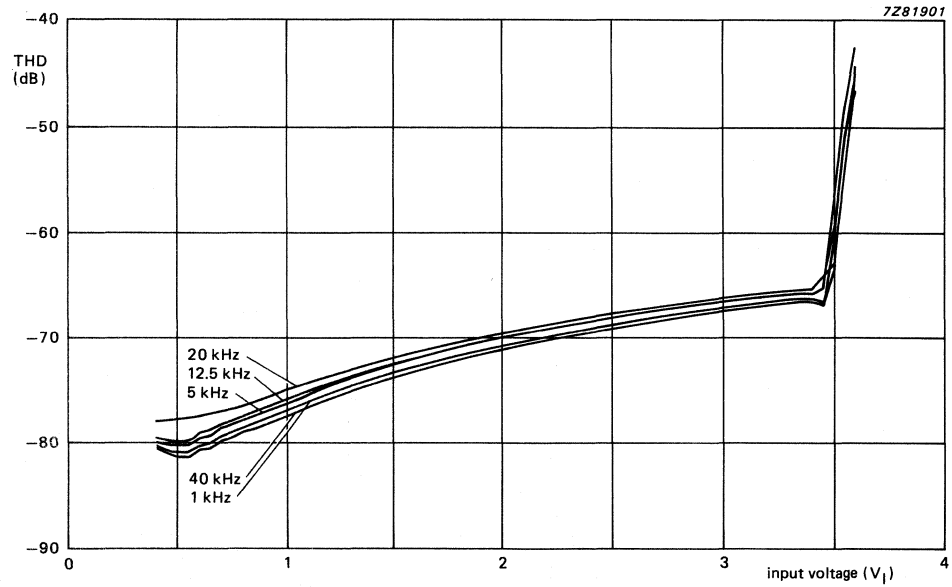


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

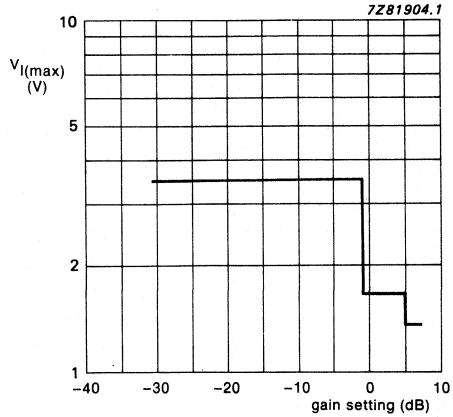


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

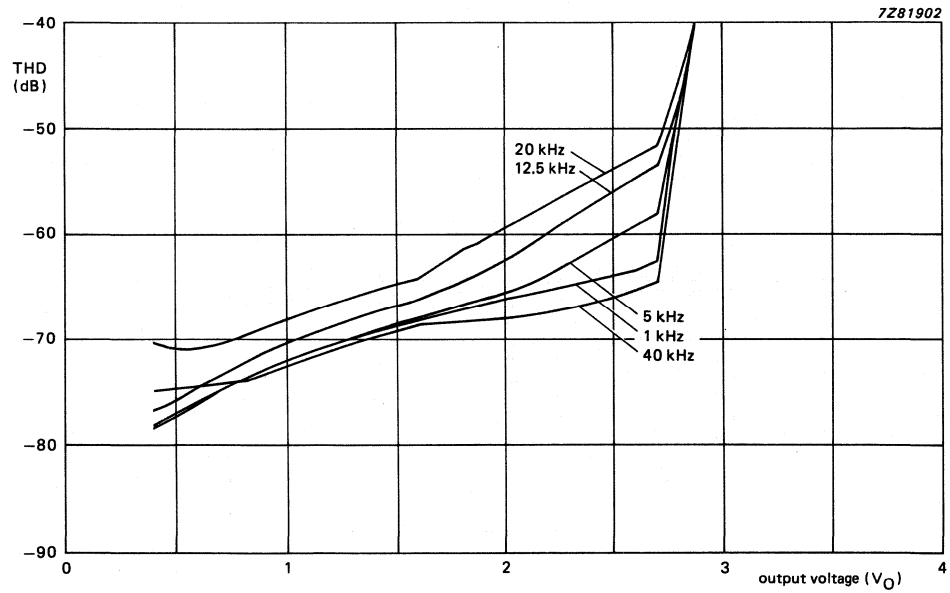


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

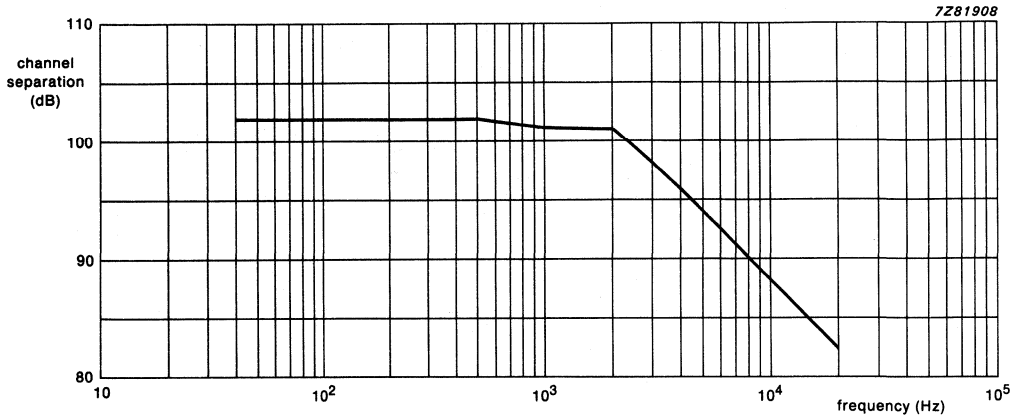
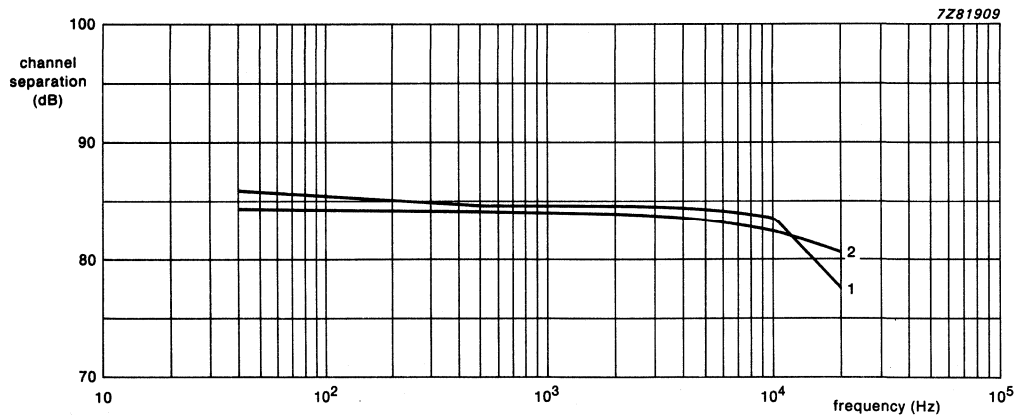


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

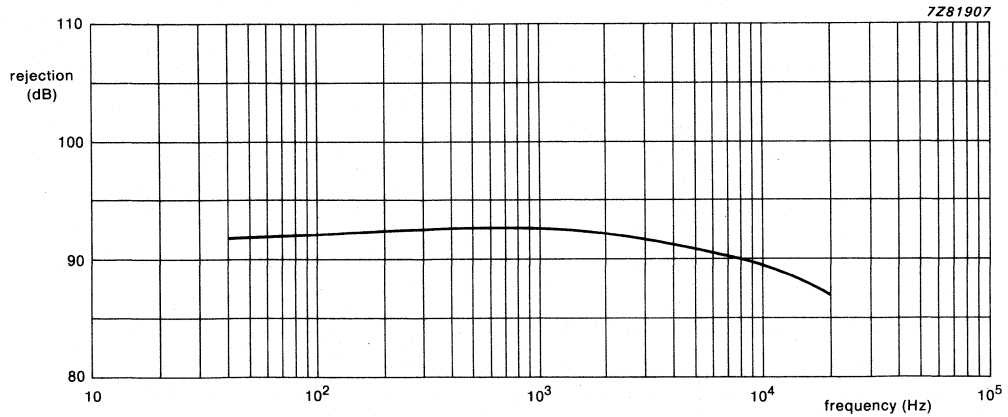


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

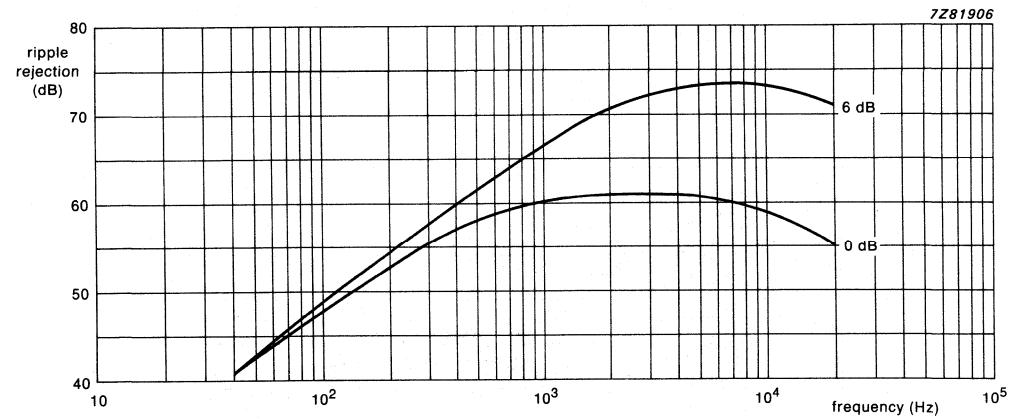


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

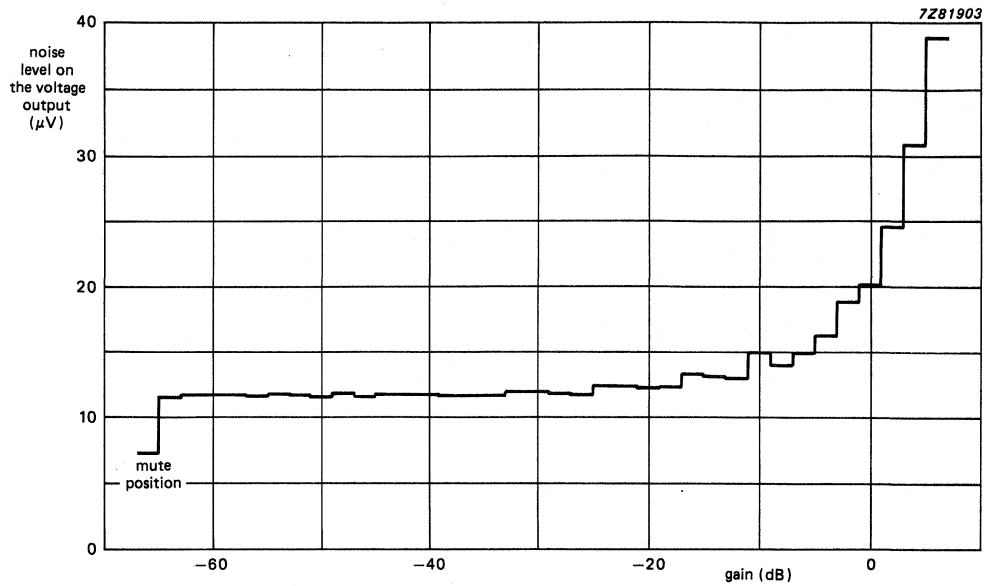


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

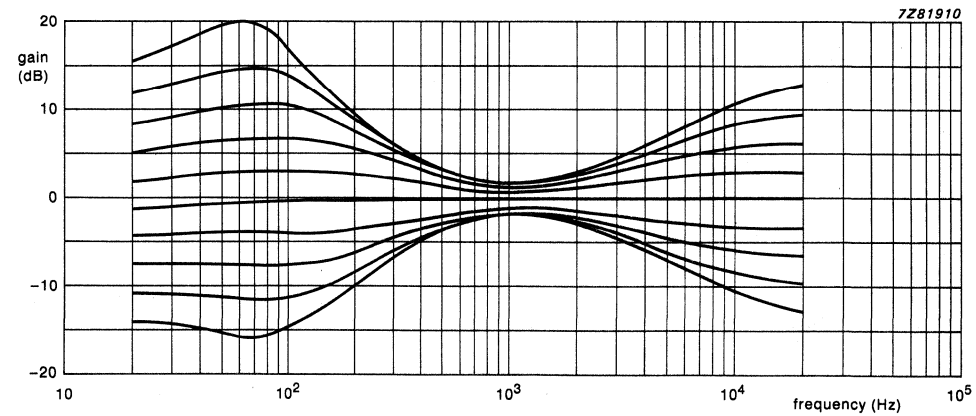


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{SG} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

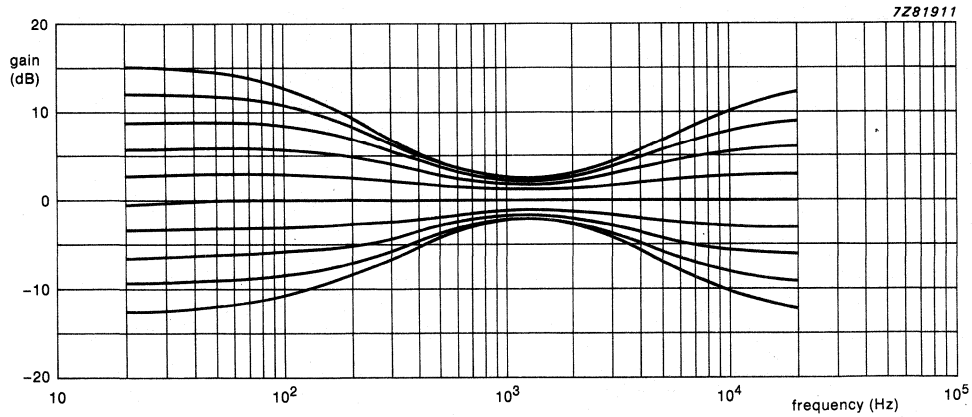


Fig. 18 Tone control with T-filter.

DEVELOPMENT DATA

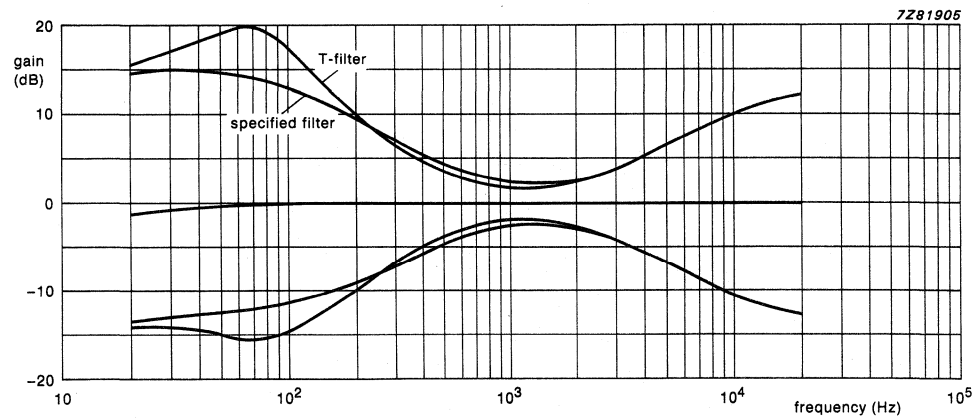


Fig. 19 Tone control.

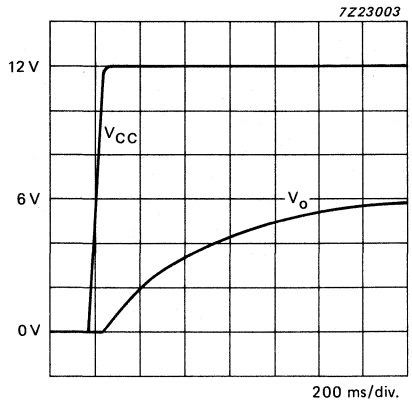


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

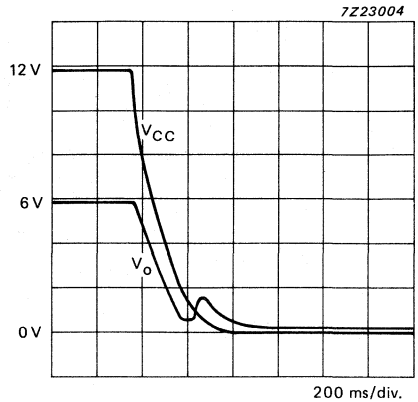


Fig. 21 Turn-off behaviour;
without modulation.

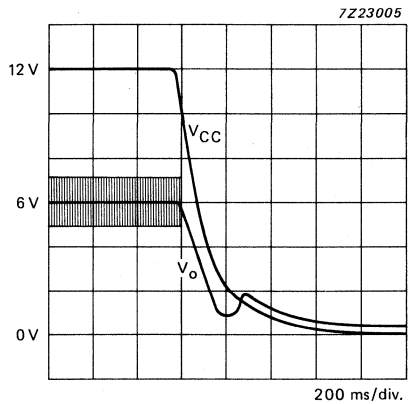
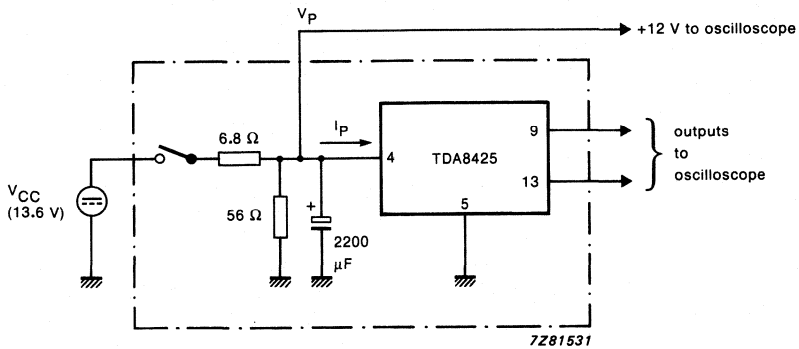


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

DEVELOPMENT DATA

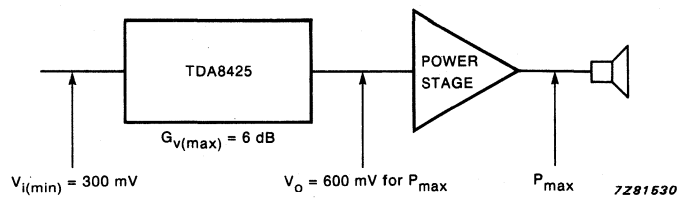


Fig. 24 Level diagram.

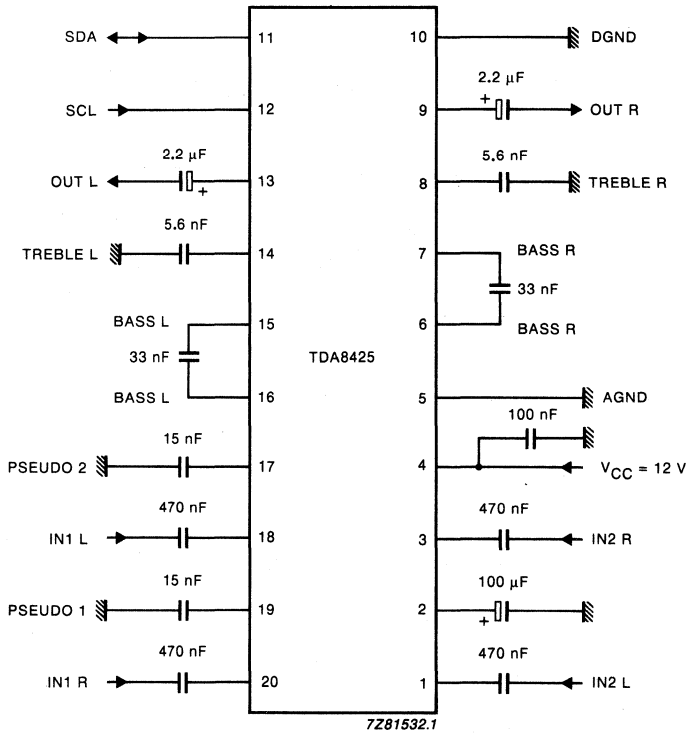


Fig. 25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8426 is a stereo sound circuit with a loudspeaker channel facility, digital controlled via the I²C-bus, for application in hi-fi audio and television sound. Reduced spatial antiphase crosstalk (30%) makes the device especially suitable for application in projection television receivers.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	−64	–	6	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

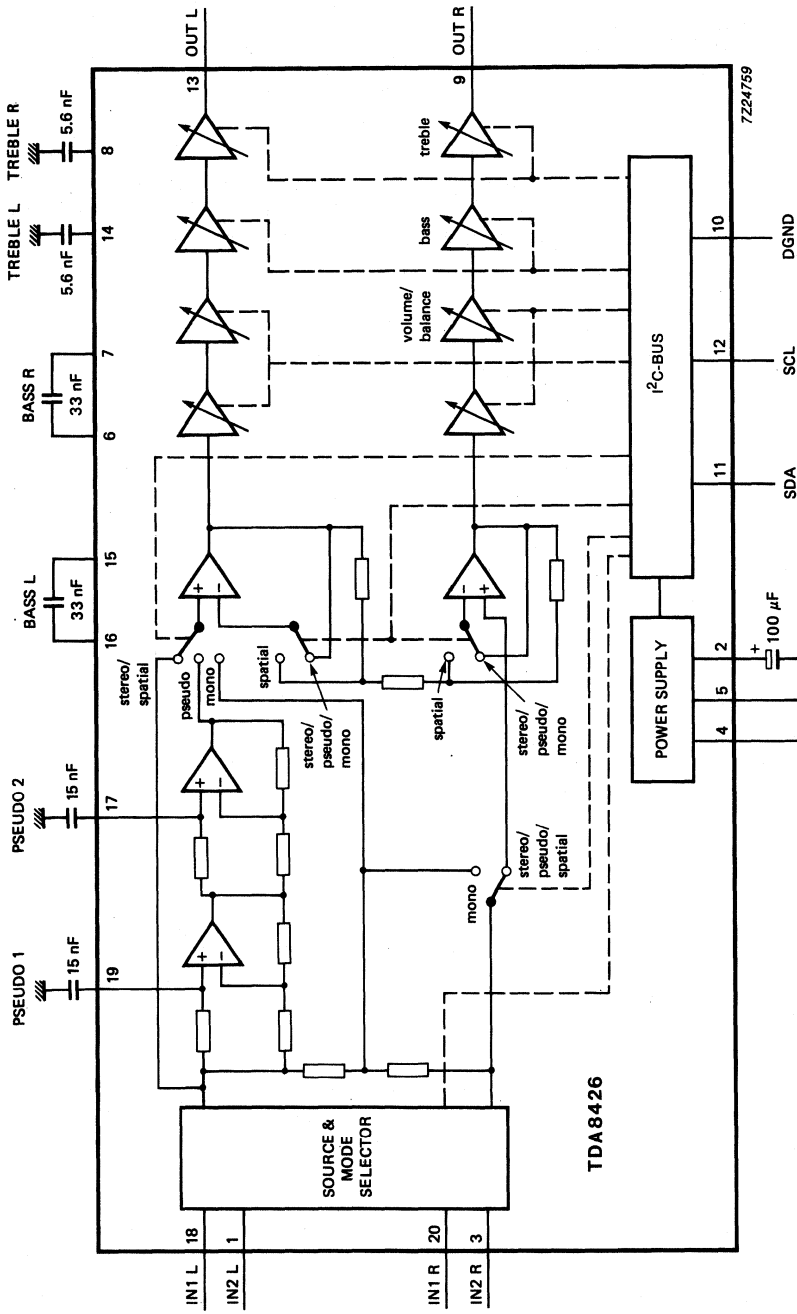


Fig.1 Block diagram.

PINNING

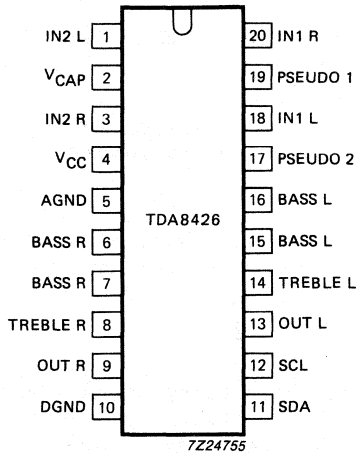


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8426 includes a bias and power supply stage, which generates a voltage of 0.5 x V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I²C-bus receiver and data handling

Bus specification

The TDA8426 is controlled via the 2-wire I²C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8426 starts with the module address MAD.

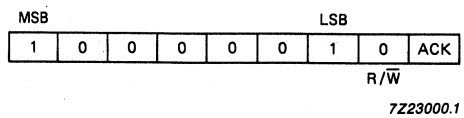


Fig. 3 TDA8426 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8426. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8426. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

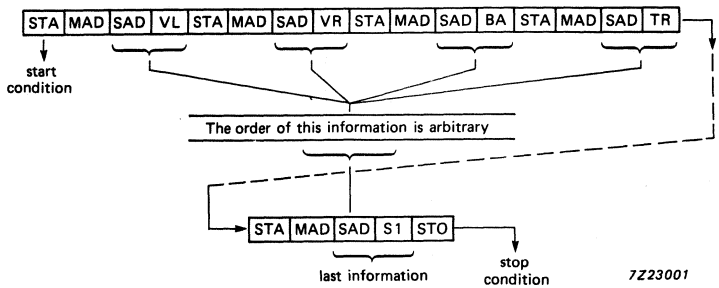


Fig. 4 Data transmission after a power-on reset.

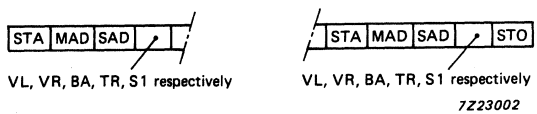


Fig. 5 Data transmission after a power-on reset with auto increment.

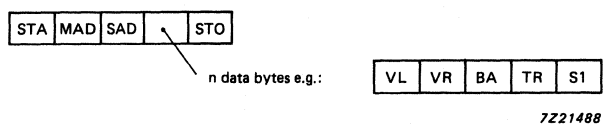


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70\ ^oC$	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	+ 150	^oC
Electrostatic handling, classification A*				

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{ref}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{ref}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{ref}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)}$ ⩽ 2 V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

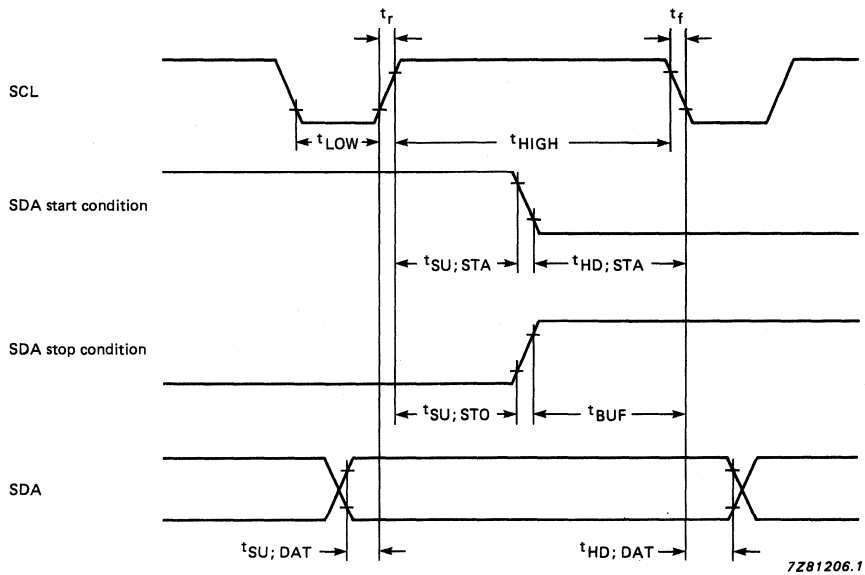
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	30	–	%
Pseudo: Phase shift (see Fig. 8)					

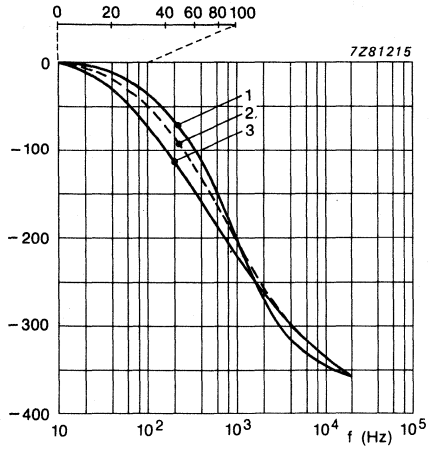
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

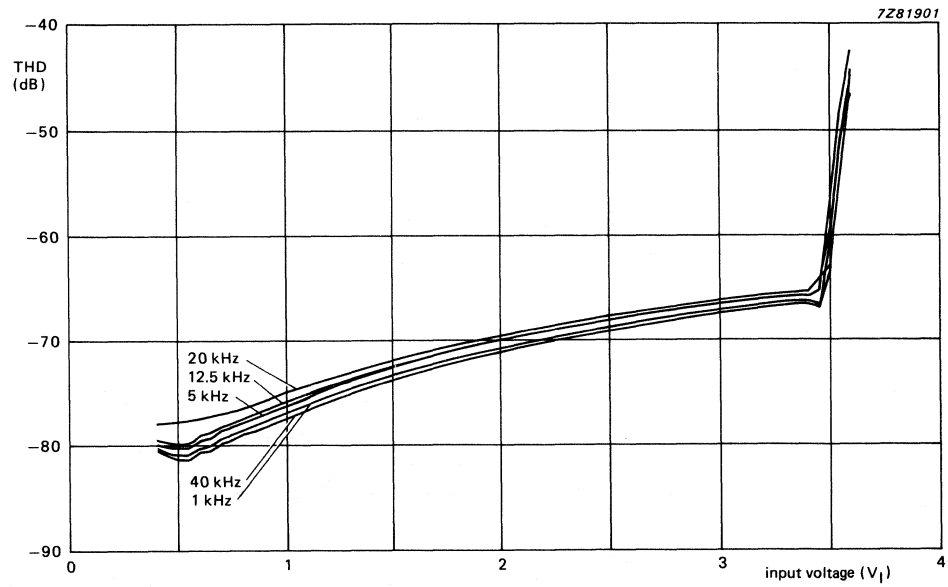


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

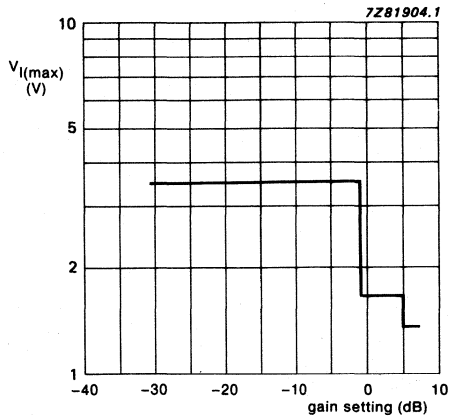


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

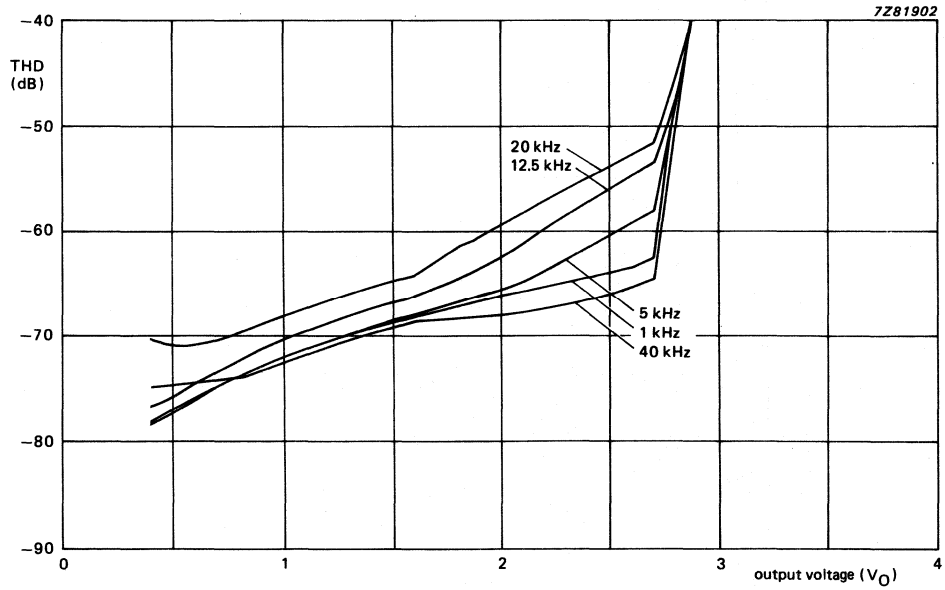


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

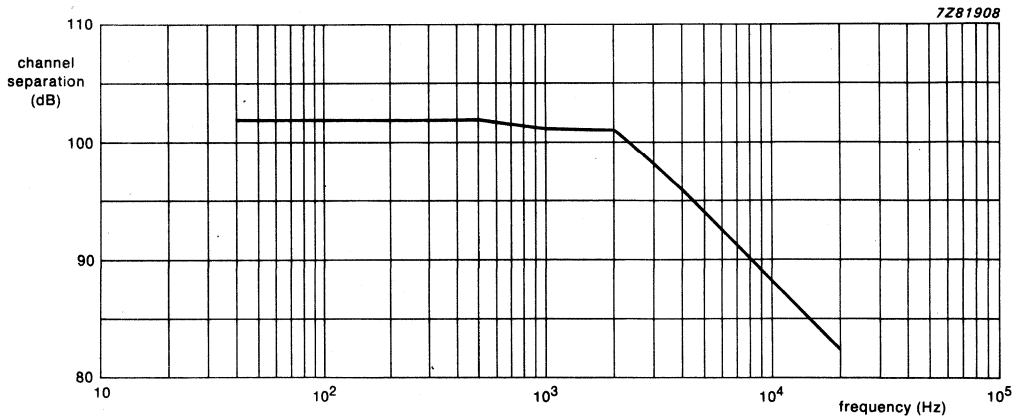
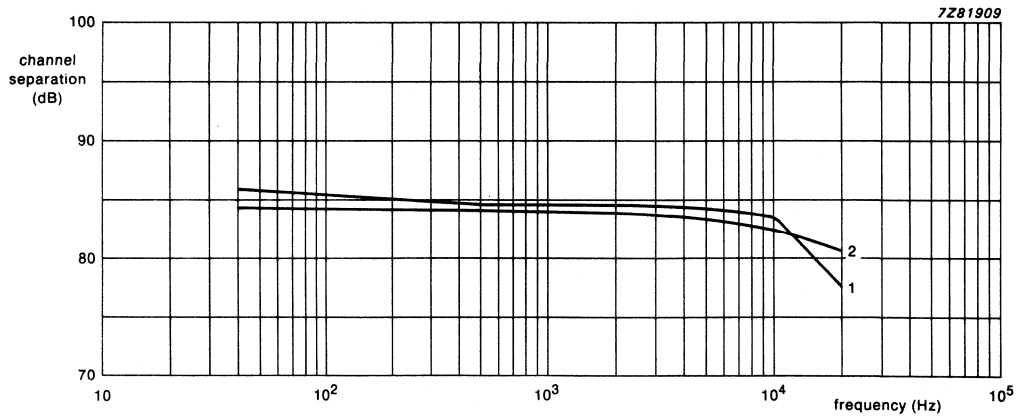


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

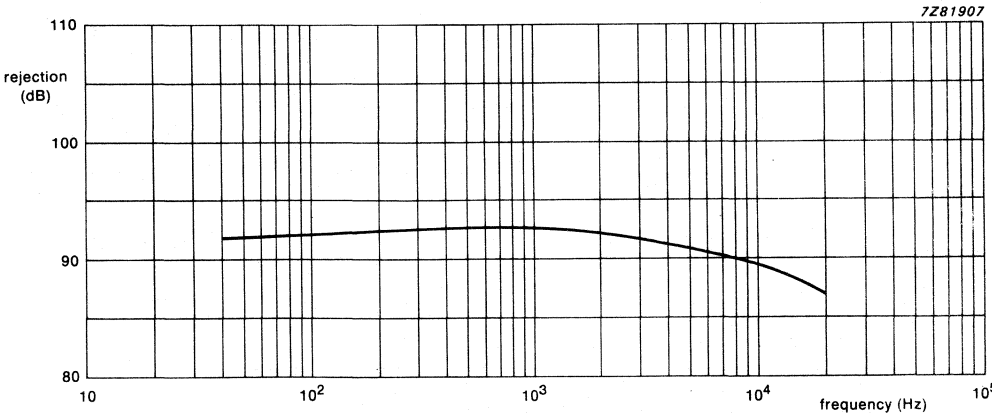


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

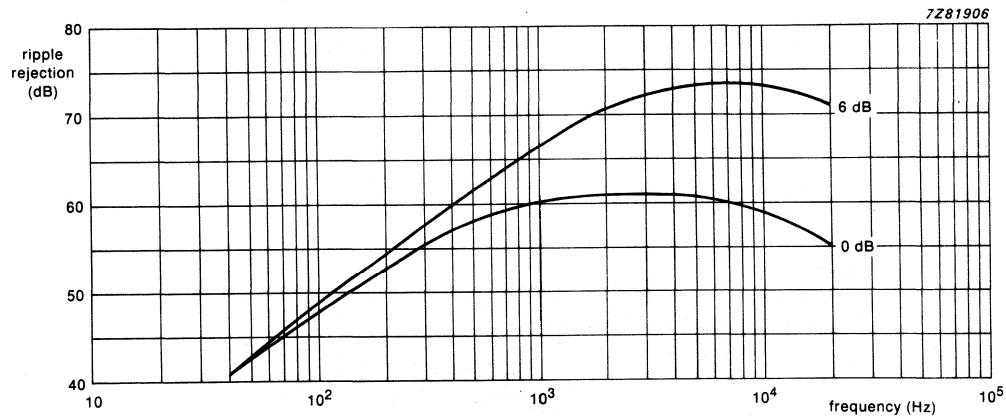


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

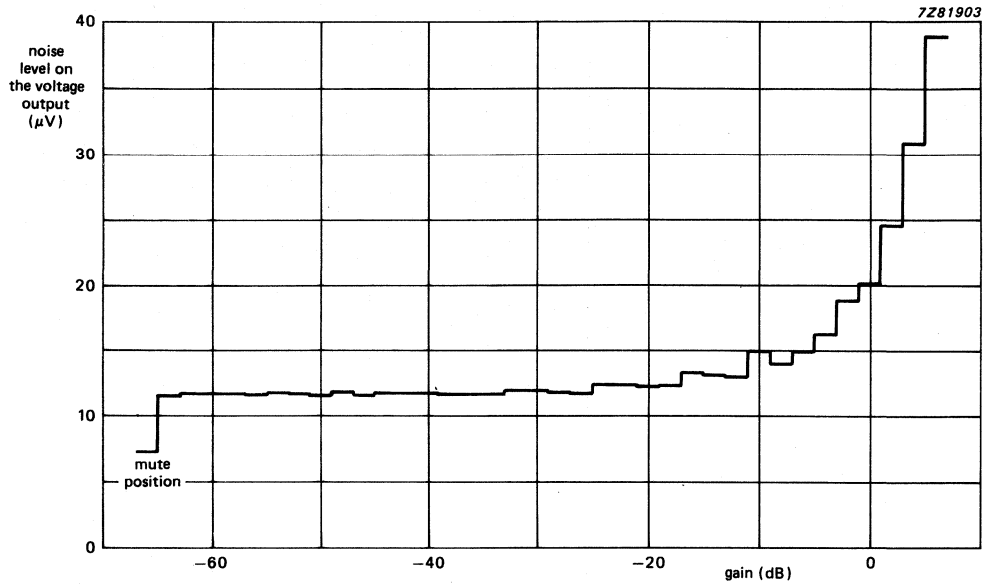


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

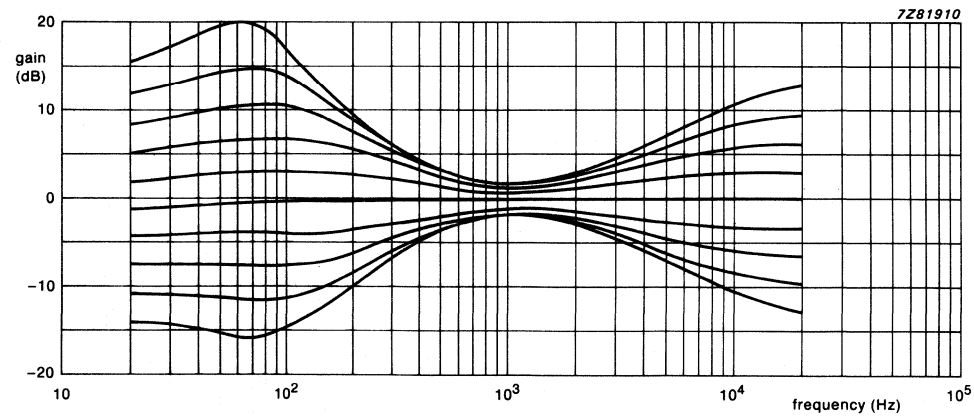


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

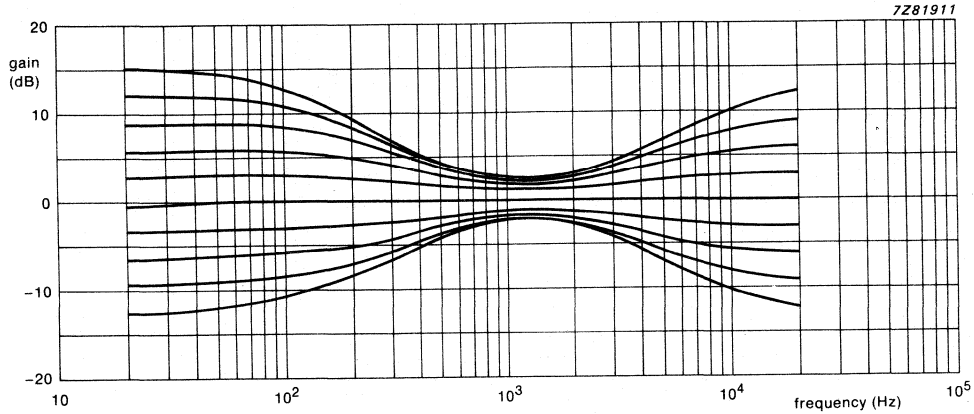


Fig. 18 Tone control with T-filter.

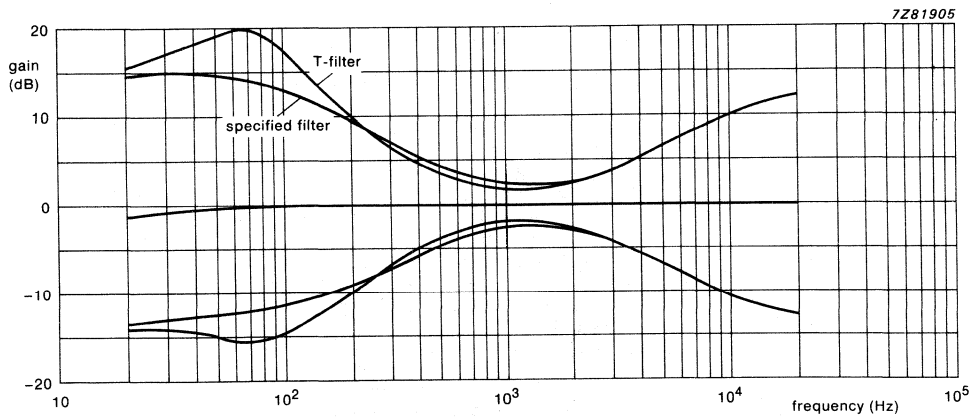


Fig. 19 Tone control.

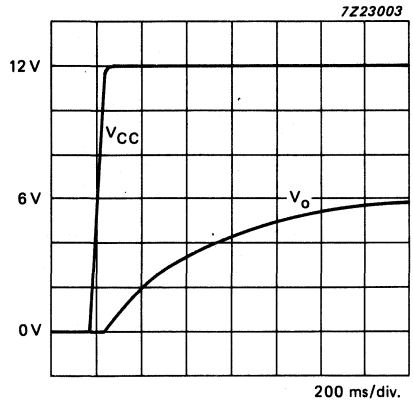


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

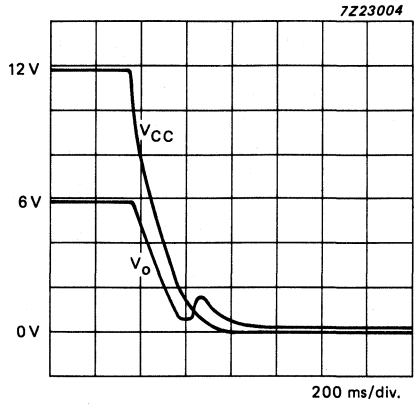


Fig. 21 Turn-off behaviour;
without modulation.

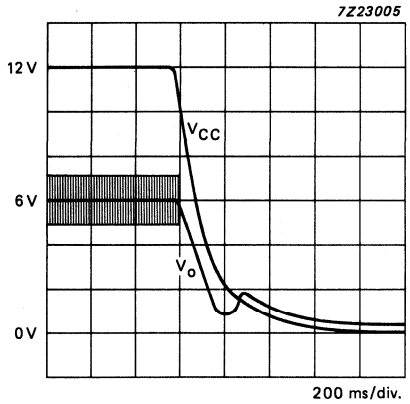
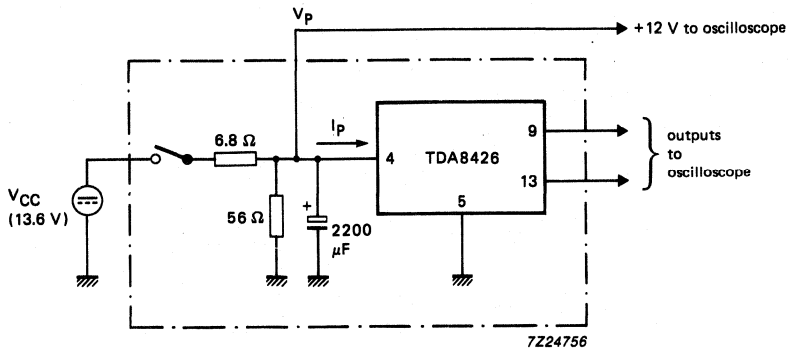


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig.23 Turn-on/off power supply circuit diagram.

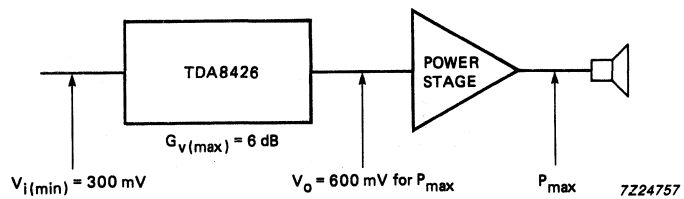


Fig.24 Level diagram.

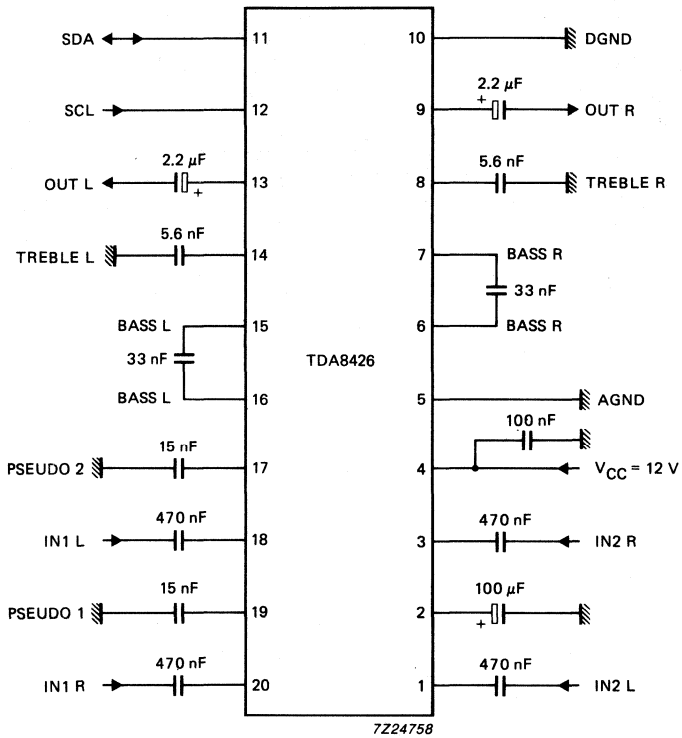


Fig.25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

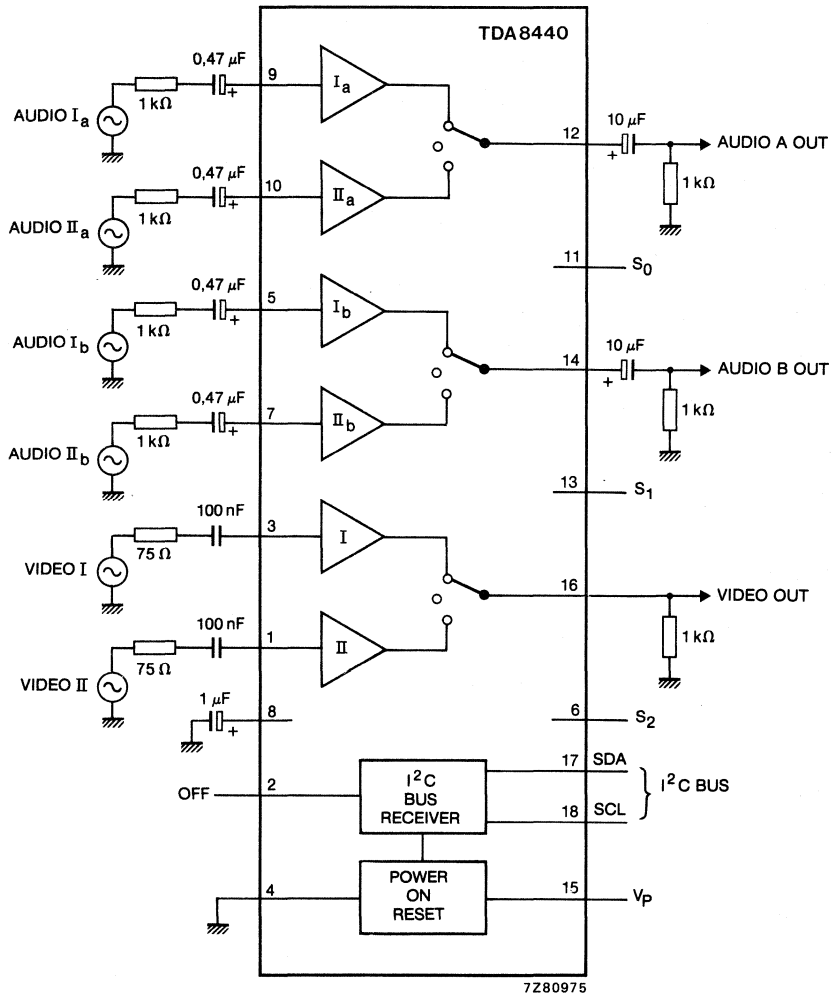
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I²C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I²C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

NON-I²C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I²C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
} Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	typ.	max.	unit
Supply voltage	pin 15	V_P	–	–	14	V
Input voltage range	pin 17	V_{SDA}	–0,3	–	V_P + 0,3	V
	pin 18	V_{SCL}	–0,3	–	V_P + 0,3	V
	pin 2	V_{OFF}	–0,3	–	V_P + 0,3	V
	pin 11	V_{S0}	–0,3	–	V_P + 0,3	V
	pin 13	V_{S1}	–0,3	–	V_P + 0,3	V
	pin 6	V_{S2}	–0,3	–	V_P + 0,3	V
Video output current	pin 16	$-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}		–	–	+ 125	°C
Operating ambient temperature range	T_{amb}		0	–	+ 70	°C
Junction temperature	T_j		–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$		=		50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{15-4}	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	A_{3-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{3-16}	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	A_{1-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{1-16}	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	V_{3-4}	–	–	4,5	V
Input video signal amplitude (gain times 1)	V_{1-4}	–	–	4,5	V
Output impedance	Z_{16-4}	–	7	–	Ω
Output impedance in 'OFF' state	Z_{16-4}	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	V_{16-4}	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	V_{16-4}	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9-4(rms)}$	–	–	2	V
	$V_{10-4(rms)}$	–	–	2	V
	$V_{5-4(rms)}$	–	–	2	V
	$V_{7-4(rms)}$	–	–	2	V
Input impedance	Z_{9-4}	50	100	–	kΩ
	Z_{10-4}	50	100	–	kΩ
	Z_{5-4}	50	100	–	kΩ
	Z_{7-4}	50	100	–	kΩ
Output impedance	Z_{12-4}	–	–	10	Ω
	Z_{14-4}	–	–	10	Ω
Output impedance (off state)	Z_{14-4}	100	–	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL, HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

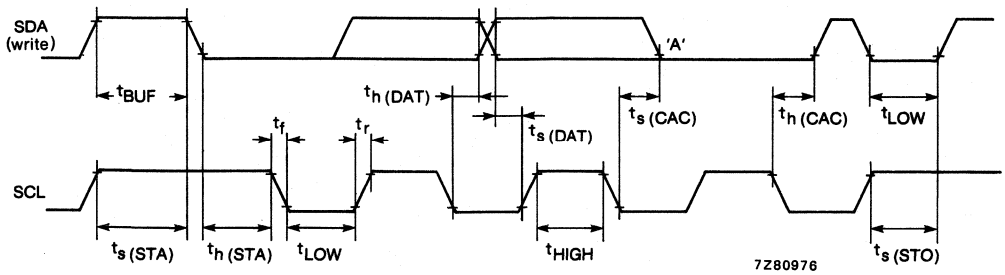


Fig. 2 Timing diagram I²C bus.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

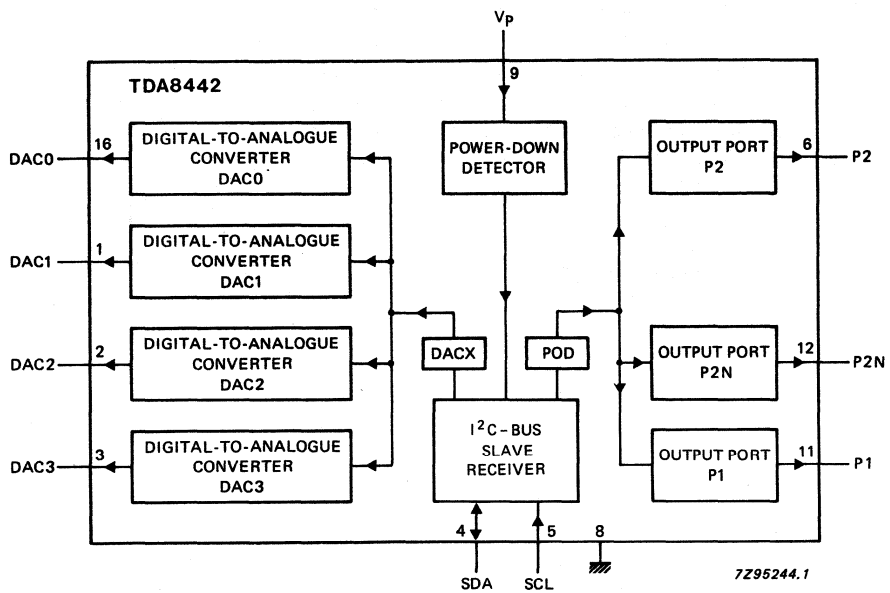


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

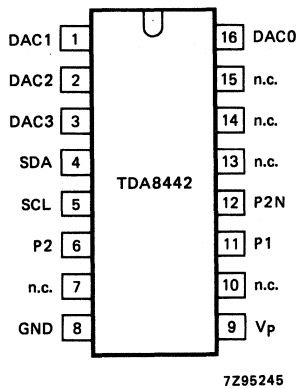


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

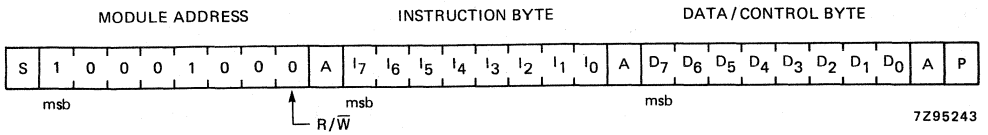


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

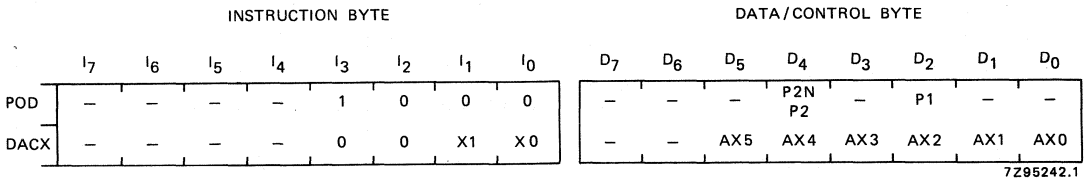


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	−	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	−	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH	note 1	I_{IH}	−	−	10	μA
Input current LOW	note 1	I_{IL}	−	−	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
Maximum output sink current		I_{OL}	3	5	−	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

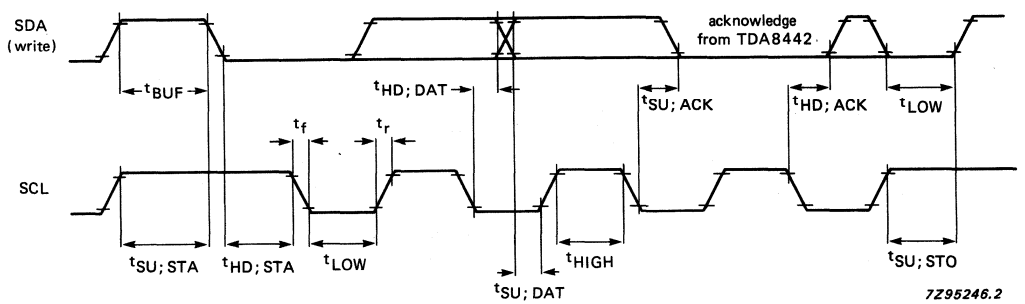
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

I²C-BUS CONTROLLED YUV/RGB SWITCH

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.
The IC ic controlled via I²C-bus by seven different addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages.

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I²C-bus or non-I²C-bus mode
- Address selection for 7 devices
- Fast switching

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 18)		$V_P = V_{18-22}$	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+/–3 dB	mode 1	B	–	10	–	MHz
Maximum output amplitude of YUV signals (peak-to-peak)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

24-lead DIL; plastic with internal heat spreader (SOT101B).

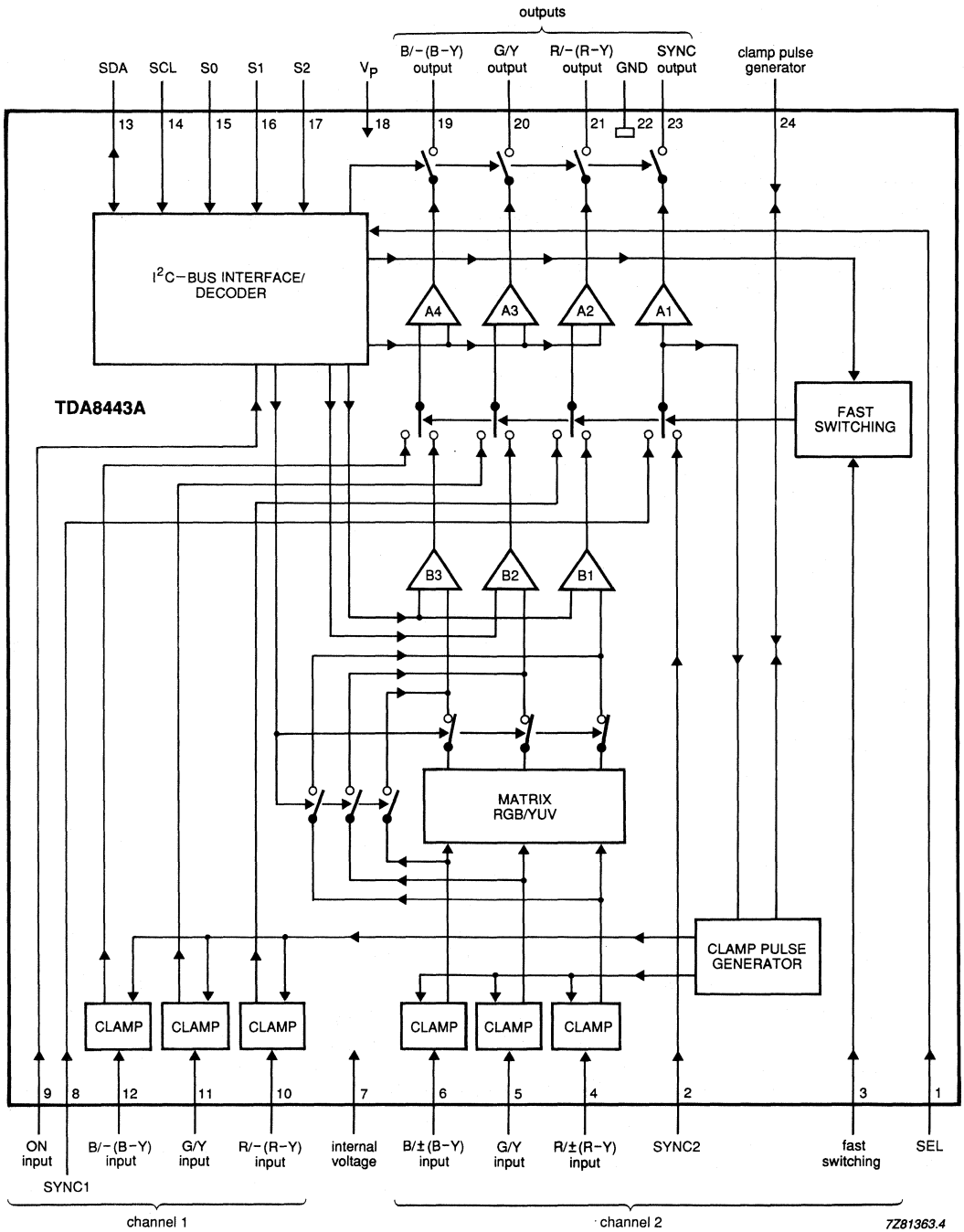


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

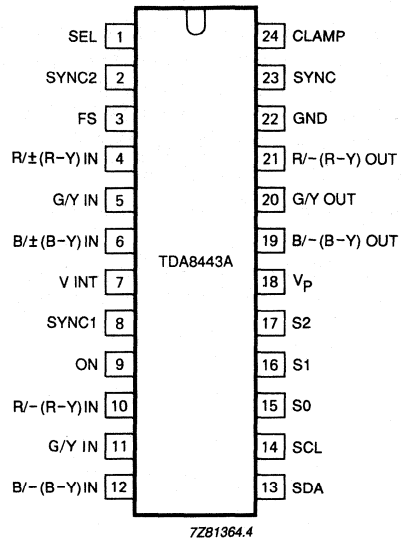


Fig.2 Pinning diagram.

1	SEL	select input (non-I²C-bus mode only)	
2	SYNC2	synchronization input for channel 2	
3	FS	fast switching input	
4	R/± (R-Y) IN	R or (R-Y) signal input	
5	G/Y IN	G or Y signal input	
6	B/± (B-Y) IN	B or (B-Y) signal input	
7	V INT	internal voltage supply	
8	SYNC1	synchronization input for channel 1	
9	ON	ON input	
10	R/−(R-Y) IN	R or −(R-Y) signal input	
11	G/Y IN	G or Y signal input	
12	B/−(B-Y) IN	B or −(B-Y) signal input	
13	SDA	serial data input/output	I²C-bus
14	SCL	serial clock input	I²C-bus
15	S0	address selection inputs	I²C-bus
16	S1	address selection inputs	I²C-bus
17	S2	address selection inputs	I²C-bus
18	V_P	positive supply voltage	
19	B/−(B-Y)	B or −(B-Y) signal output	
20	G/Y OUT	G or Y signal output	
21	R/−(R-Y)	R or −(R-Y) signal output	
22	GND	ground	
23	SYNC	synchronization output	
24	CLAMP	clamping pulse generator input/output	

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

RGB signals of channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I^2C-bus mode).

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.

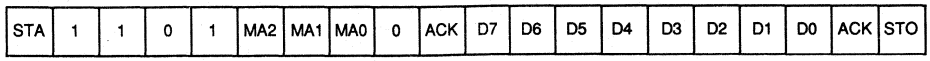


Fig.3 I²C-bus protocol.

Where:

STA : start condition
MA2, MA1, MA0 : address selection bits, see Table 1
ACK : acknowledge bit
D7 : channel selection bit, see Table 2
D6 : matrix selection bit, see Table 2
D5, D4, D3 : gain control bits, see Table 3
D2 : fast switching priority bit, see Table 4
D1, D0 : output state control bits, see Table 5
STO : stop condition

DEVELOPMENT DATA

Table 1 Address selection

address select pins			address select bits		
S2 pin 17	S1 pin 16	S0 pin 15	MA2	MA1	MA0
L	L	L	*	*	*
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Where:

L = input voltage LOW
H = input voltage HIGH
* = non-I²C-bus operation

Table 2 Mode control bits D7, D6

mode	D7	D6	function
0	0	0	channel 2 selected, no matrix
1	0	1	channel 2 selected, matrix active
2	1	0	channel 1 selected
–	1	1	not allowed

I²C-bus mode (continued)

Table 3 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	−1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed			
0	1	1	1	1	−1	0.45
1	0	0	2	2	−1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	−1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3\ R + 0.59\ G + 0.11\ B$
$R\text{-}Y = 0.7\ R - 0.59\ G - 0.11\ B$
$B\text{-}Y = -0.3\ R - 0.59\ G + 0.89\ B$

Table 4 Priority/fast switching bit D2

D2	fast switching pin 3	mode
0	X	0 to 2, depending on D7, D6
1	0.4 V	2

Where:
X = don't care

Table 5 Output state control bits

D1	D0	pin 9	function
0	X	X	OFF
1	0	L	OFF
1	0	H	ON
1	1	X	ON

Where:
X = don't care

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

DEVELOPMENT DATA

Timing specifications

I²C-bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4.7	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	μs
SCL and SDA LOW time	t_{LOW}	4.7	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	μs
SCL and SDA rise time	t_r	–	1.0	μs
SCL and SDA fall time	t_f	–	0.3	μs
Data set-up time (write)	$t_{SU;DAT}$	250	–	ns
Data hold time (write)	$t_{HD;DAT}$	1.0	–	μs
Acknowledge set-up time	$t_{SU;ACK}$	–	2	μs
Acknowledge hold time	$t_{HD;ACK}$	0	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	μs

Note

Timing $t_{HD;DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

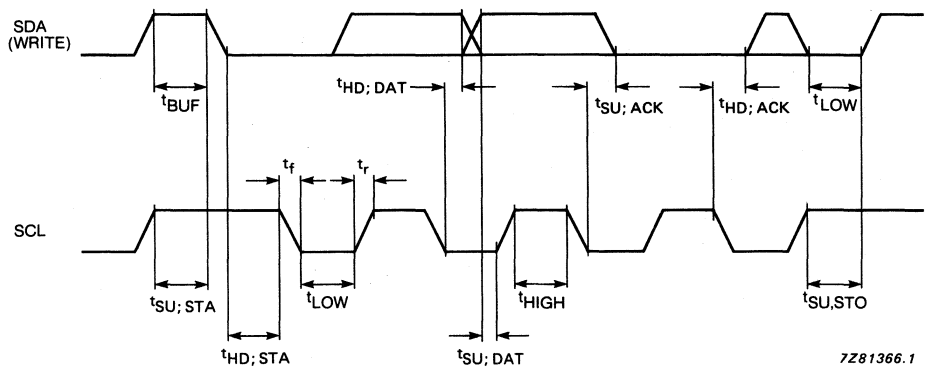


Fig.4 I²C-bus timing diagram.

Non-I²C-bus mode

Table 6 Non-I²C-bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings			
pin 13	pin 14	pin 1	by FS (pin 3)	A1	A4, A3, A2	B1, B3	B2
L	L	L	2/0	1	1	1	1
L	L	H	2/0	1	2	1	1
L	H	L	2/1	1	1	−1	0.45
L	H	H	2/0	1	1	−1	0.45
H	L	L	2/0	2	1	1	1
H	L	H	2/0	2	2	1	1
H	H	L	2/1	2	1	−1	0.45
H	H	H	2/0	2	1	−1	0.45

Table 7 Fast switching input (pin 3)

FS	mode selected
⩽ 0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 8 ON input (pin 9)

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in Table 6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 18)	V_P	–	14	V
Input voltage range				
SDA (pin 13)	V_I	−0.3	14	V
SCL (pin 14)	V_I	−0.3	14	V
any other pin	V_I	−0.3	V_P + 0.3	V
Maximum output current	I_O	–	20	mA
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C
Maximum junction temperature	T_j	–	+ 125	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 18)		V_P	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference (programmed value)			–	0	10	%
Relative gain difference						
between Y output and the (R-Y) and (B-Y) channel inputs			–	0	10	%
between any two other channels			–	0	5	%
Input current		I_I	–	0.5	1.0	μA
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
±3 dB	mode 1	B	–	10	–	MHz
Mutual time difference at output	all inputs of one source connected together		–	–	25	ns
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Crosstalk between	note 1					
inputs of same source	f = 5 MHz	α	–	–	–30	dB
different sources		α	–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		50	–	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Differential gain at nominal output signals (peak-to-peak value)	R-Y = 1.05 $V_{(p-p)}$		–	–	10	%
	B-Y = 1.33 $V_{(p-p)}$		–	–	10	%
	Y = 0.34 $V_{(p-p)}$		–	–	10	%
Signal-to-noise ratio nominal input	note 2 B = 5 MHz	S/N	50	–	–	dB
Supply voltage ripple rejection	note 3	RR	30	–	–	dB
DC output levels during clamping		V_O	–	5.3	–	V
Synchronization channels						
Gain difference (programmed value)			–	–	10	%
Bandwidth						
–3 dB		B	–	50	–	MHz
+ 3 dB gain x 1		B	–	20	–	MHz
+ 3 dB gain x 2		B	–	13	–	MHz
Input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		$V_{I(p-p)}$	0.2	–	2.5	V
Output impedance (pin 23)		$\lvert Z_{23-22} \rvert$	–	20	30	Ω
Maximum undistorted output amplitude (pin 23) (peak-to-peak value)		$V_{O(p-p)}$	2.5	–	–	V
DC output level on top of sync pulse		V_O	1.5	1.9	2.4	V
I²C-bus inputs						
SDA, SCL						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
I²C-bus output						
SDA (open collector)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

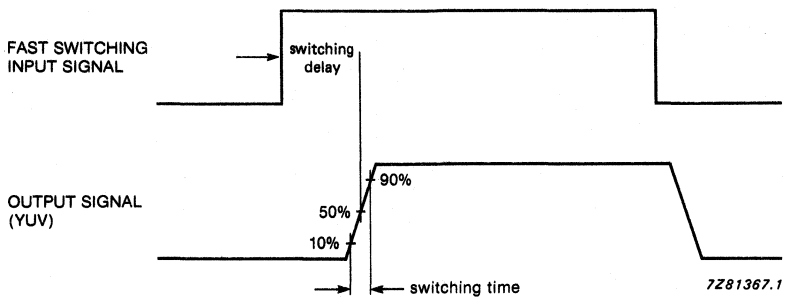
parameter	conditions	symbol	min.	typ.	max.	unit
Address selection inputs						
S0, S1, S2						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
Fast switching input						
Input voltage HIGH		V_{IH}	1	–	3	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	500	μA
Input current LOW		I_{IL}	−100	–	–	μA
Switching time	see Fig.5	t	–	10	–	ns
Switching delay	see Fig.5	t_d	–	20	–	ns
Select input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
ON input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.

2. Signal-to-noise ratio = $20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (RMS) } B = 5 \text{ MHz}}$

3. Supply voltage ripple rejection = $20 \log \frac{V_{RR} \text{ supply}}{V_{RR} \text{ on the output}}$



Input = 0 V (input 1; Mode 2)
Input = 0.75 V (RGB; Mode 1)

Fig.5 Fast switching signal diagram.

DEVELOPMENT DATA

APPLICATION INFORMATION

Table 9 Application information

input 1	input 2	output	mode	G2	G1	G0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	1	1
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	1	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	0	0
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	0	0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	0	1
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	0	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	1	0
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	1	0

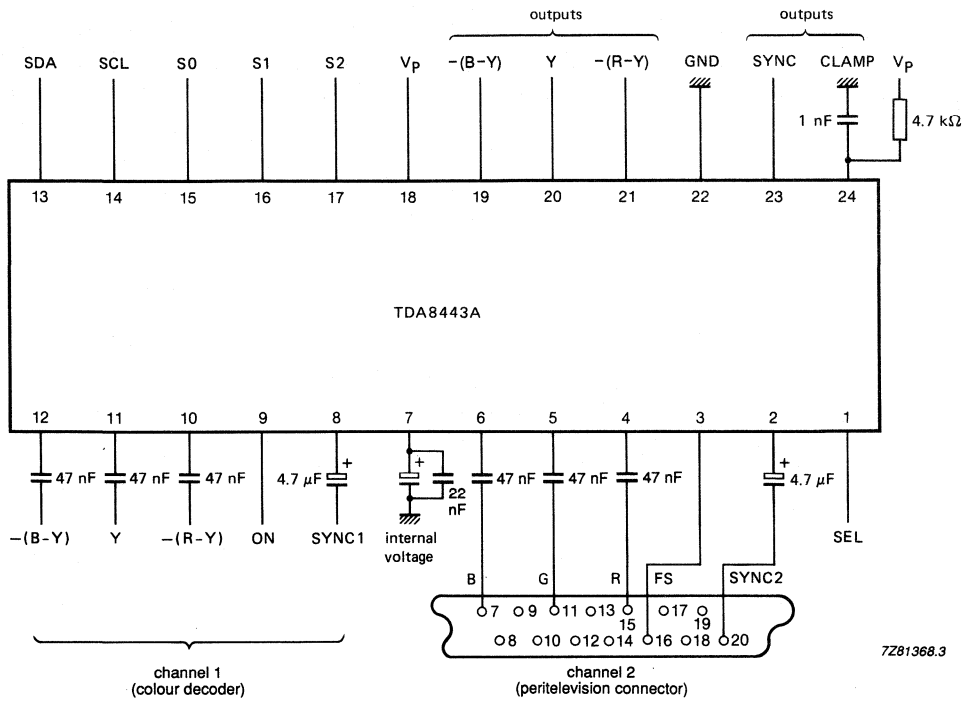


Fig.6 Application diagram (example).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

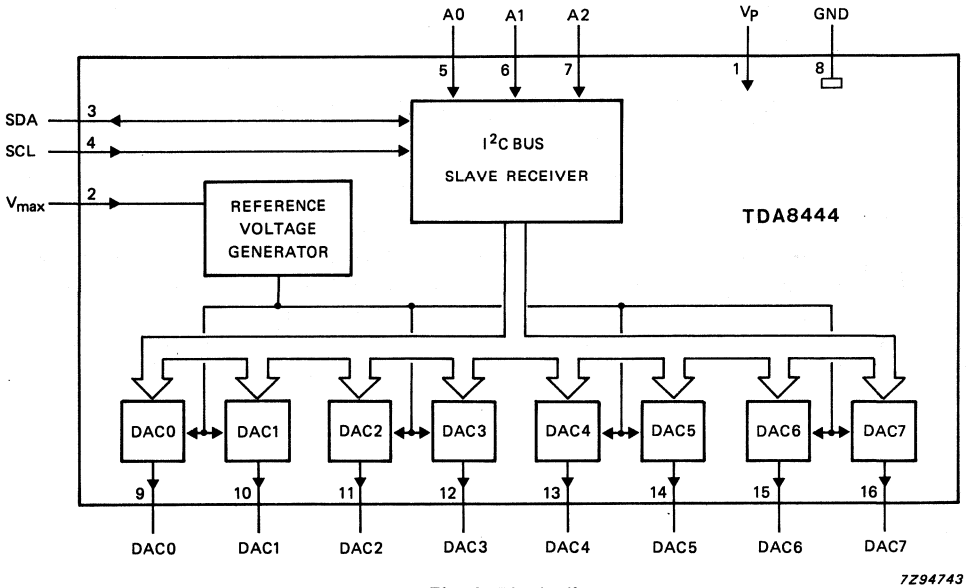


Fig. 1 Block diagram.

PINNING

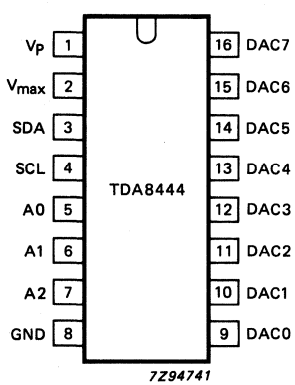


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care

A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	75 K/W

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}	see note			V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

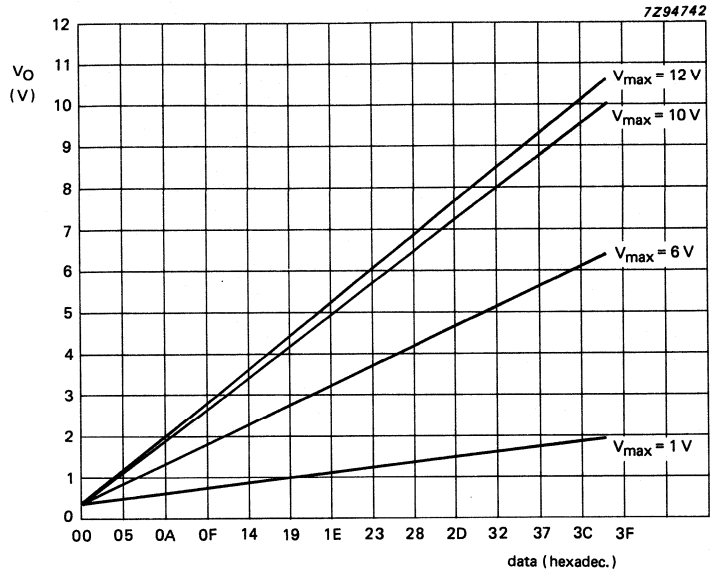


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

SECAM DECODER

GENERAL DESCRIPTION

The TDA8490 is a monolithic integrated SECAM decoder. This circuit is intended to be used in conjunction with TDA8390 or TDA8461 (PAL decoder), TDA8451 (delay) and TDA8452 (filter). In this application the TDA8490 is placed in parallel with the demodulation circuit of the PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply current		$I_P = I_9$	40	55	70	mA
Chrominance amplifier and demodulator						
Input signal (peak-to-peak value)	SECAM with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
Identification						
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Sandcastle detector and clamp pulse generator						
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heat spreader (SOT102).

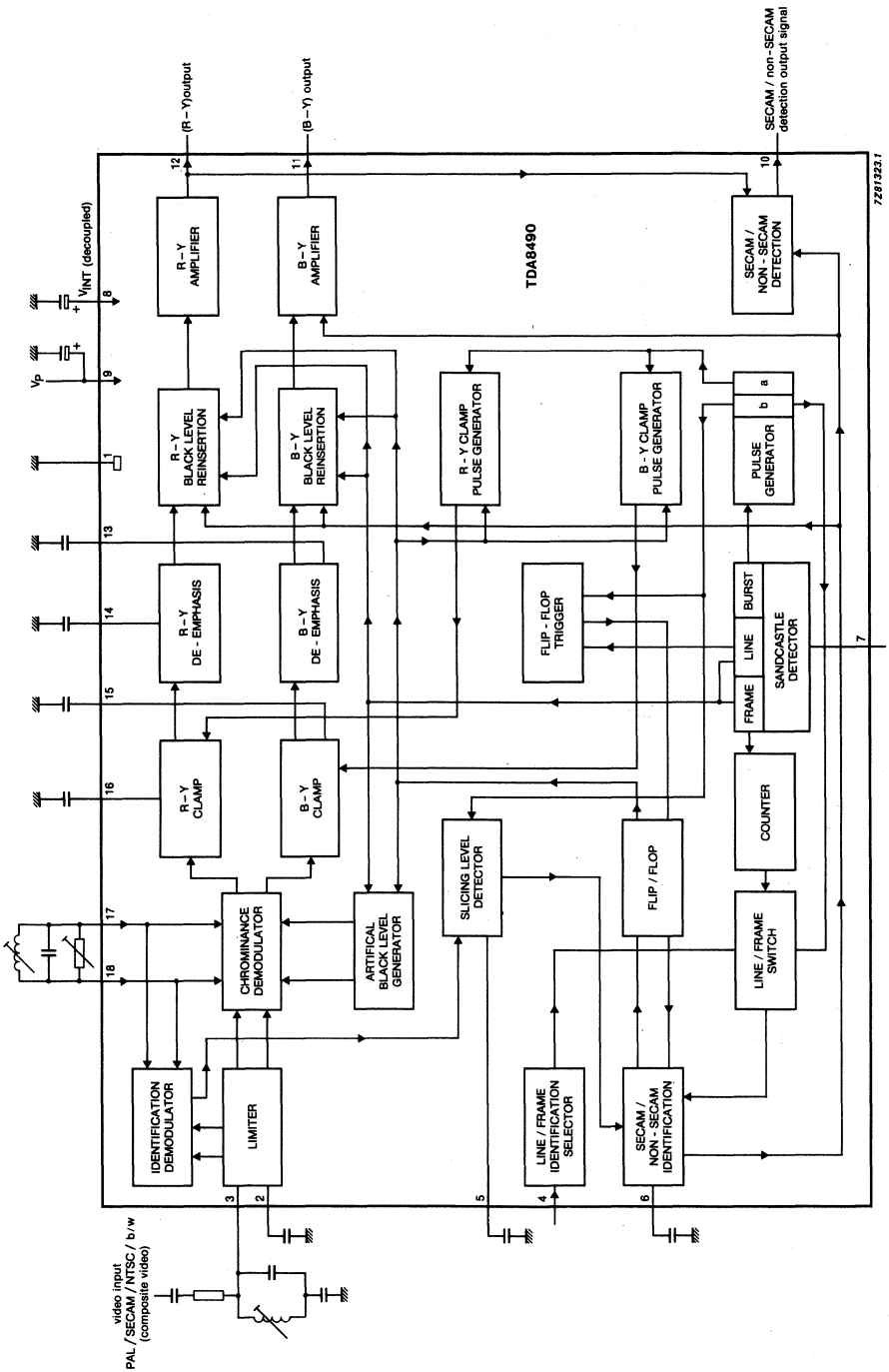


Fig. 1 Block diagram.

PINNING

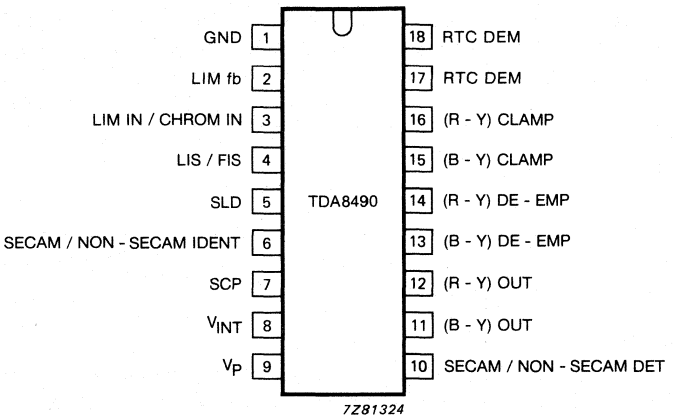


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	GND	ground	9	V_P	supply voltage
2	LIM fb	limiter feedback	10	SECAM/NON-SECAM DET	SECAM/non-SECAM detection circuit
3	LIM IN/ CHROM IN	limiter input/ chrominance input	11	(B-Y)OUT	(B-Y) signal output
4	LIS/FIS	line identification selector/ frame identification selector	12	(R-Y)OUT	(R-Y) signal output
			13	(B-Y)DE-EMP	(B-Y) de-emphasis circuit
5	SLD	slicing level detector	14	(R-Y)DE-EMP	(R-Y) de-emphasis circuit
6	SECAM/NON-SECAM IDENT	SECAM/non-SECAM identification circuit	15	(B-Y)CLAMP	(B-Y) clamping circuit
			16	(R-Y)CLAMP	(R-Y) clamping circuit
7	SCP	sandcastle pulse input	17	RTC DEM	reference tuned circuit demodulator
8	V_{INT}	internal supply voltage (decoupled)	18	RTC DEM	reference tuned circuit demodulator

FUNCTIONAL DESCRIPTION

Demodulation

The TDA8490 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 3 (applied via a bandpass filter with a bell-shaped response) is SECAM or non-SECAM (NTSC, PAL or black-and-white).

When the SECAM signal is detected, it is applied to a limiter/amplifier after which it is demodulated. The (R-Y) and (B-Y) signals are applied sequentially, therefore, only one demodulator is required. After demodulation the signals are applied to the (R-Y) and (B-Y) clamp circuits, where the black levels are clamped to the same DC level.

Artificial black levels are inserted during line blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signal (necessary in case there are no line burst signals available). The inserted signals may not be identical to the detected black levels, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

R-Y and B-Y output signals

The R-Y and B-Y signals are available every other line. A new black level is reinserted during blanking and timing b (Fig. 5). If a non-SECAM signal is present the R-Y output will generate a DC level of approximately 3,8 V (the same as the black level generated during normal SECAM condition on both outputs). The B-Y output generates a DC level of approximately 0,8 V in this condition.

SECAM or non-SECAM signals may also be identified by the information at pin 10:

- 2,6 V indicates a SECAM signal.
- 0 V indicates a non-SECAM signal.

The SECAM or non-SECAM signals can be identified by using the (B-Y) demodulator output level at pin 11. Depending on the PAL decoder used in conjunction with this device, the information can be passed to the microcomputer via the I^2C bus.

Priority identification

The two chrominance outputs of TDA8490 are connected to the chrominance outputs of the PAL decoder TDA8461 or TDA8390. The output signal of the TDA8490 and PAL decoder alternately determine the priority of the overall system. In the event of a clash on these outputs, caused by a reflected PAL signal being detected as a SECAM signal by TDA8490, the total system will default to PAL priority.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For line identification this comparison occurs during the internally generated pulse 'B' (Fig. 3). Only SECAM signals provide voltage difference from line to line during comparison. If the phase relationship between both the signals is incorrect, the flip-flop will receive an extra input pulse.

The identification (as above) occurs when the line identification system is active. When the frame identification system is switched on (pin 4), the system only compares the demodulator output voltage during a 4-line gate pulse, which is present during frame blanking. The 4-line gate pulse starts 10 burst gate pulses after the start of the vertical blanking part of the sandcastle signal. The operation is identical to the line identification. Timing of the 4-line gate pulse is shown in Fig. 4.

Sandcastle detector

The sandcastle pulse detector requires a 3-level sandcastle pulse. It detects the various blanking and gating pulses and generates the correct drive pulses for the clamping circuits (Fig. 3).

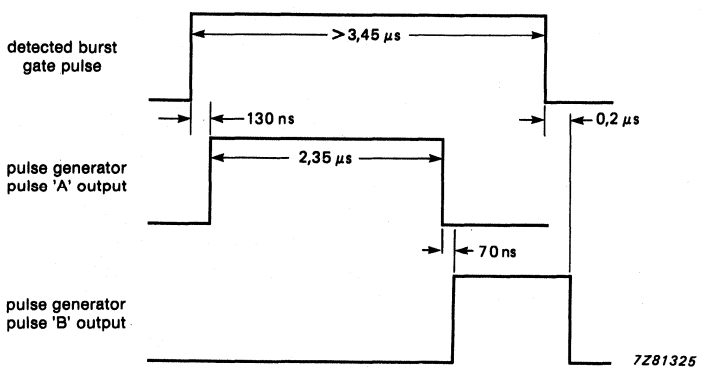


Fig. 3 Burst and derived pulses.

Note

The separated burst pulse is divided into two parts (Fig. 3). Required burst gate pulse: $> 3{,}45\ \mu s$.

Pulse 'A':

- timing R-Y clamp (only present during a red line)
- timing B-Y clamp (only present during a blue line)

Pulse 'B':

- SECAM line identification timing

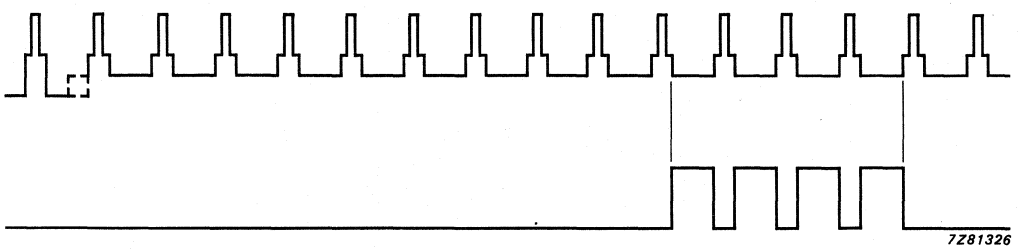


Fig. 4 above: Sandcastle signal during frame period (even and odd).

below: 4-line gate pulse.

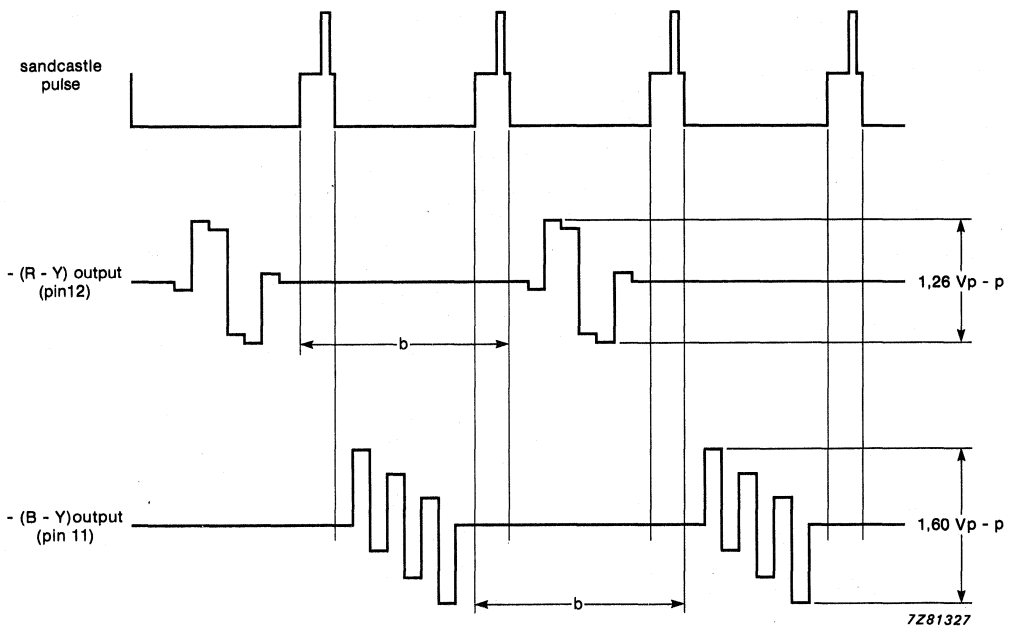


Fig. 5 $-(R\text{-}Y)$ and $-(B\text{-}Y)$ output signals compared to the sandcastle input signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 9	V_P	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	–25	+ 150	°C
Operating ambient temperature range		T_{amb}	–25	+ 65	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply voltage	decoupled, pin 8	$V_{INT} = V_{8-1}$	10,6	11,8	13,0	V
Supply current		$I_P = I_9$	40	55	70	mA
Total power dissipation		P_{tot}	–	660	840	mW
Thermal resistance from junction to ambient		$R_{th\ j\text{-}a}$	–	50	–	K/W
External capacitance	pin 8	$C_o = C_{8-1}$	–	–	4,7	µF
Chrominance amplifier and demodulator	note 1					
Input signal (peak-to-peak value)	non-SECAM signal	$V_{3-1(p-p)}$	–	–	1,1	V
Input signal (peak-to-peak value)	SECAM signal with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
Input resistance	pin 3	R_{3-1}	9,5	11,8	14,1	kΩ
Input capacitance	pin 3	C_{3-1}	–	–	5	pF
Input resistance	between pins 17 and 18	R_{17-18}	2,9	3,6	4,3	kΩ
Input capacitance	between pins 17 and 18	C_{17-18}	–	12	–	pF
De-emphasis output resistance	pins 13 and 14	R_{13-1} R_{14-1}	1,45	1,75	2,05	kΩ
Zero point stability of chrominance demodulator	note 2 pins 11 and 12	$f_{11, 12}$	–	5	–	kHz
(B-Y)/(R-Y) gain ratio	note 7		1,38	1,55	1,73	

parameter	conditions	symbol	min.	typ.	max.	unit
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
B-Y output signal level	SECAM		3,5	3,8	4,1	V
B-Y output signal level	non-SECAM		–	0,8	1,1	V
R-Y output signal level			3,5	3,8	4,1	V
R-Y signal linearity	note 3		88	95	102	%
B-Y signal linearity	note 4		85	92	99	%
Inserted black levels (demodulated)	function of temperature, note 6		–	0,22	–	kHz/K
Output impedance	pin 12	$\|Z_{12-1}\|$	–	30	–	Ω
Output impedance	pin 11	$\|Z_{11-1}\|$	–	30	–	Ω
Identification	SECAM, non-SECAM					
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Input current	pin 4	I_4	–	–5	–25	μA
Voltage at pin 6	during non-SECAM	V_{6-1}	–	10,2	–	V
Voltage at pin 6	during SECAM	V_{6-1}	–	7,7	–	V
Identification level at pin 6		V_{6-1}	10,5	10,8	11,0	V
Internal colour 'OFF' (pin 6)	SECAM to non-SECAM	V_{6-1}	9,7	10,0	10,3	V
Internal colour 'ON' (pin 6)	non-SECAM to SECAM	V_{6-1}	8,9	9,2	9,5	V
Colour 'ON' to colour 'OFF' hysteresis	non-SECAM to SECAM	V_{6-1}	0,5	0,8	1,0	V
Voltage at pin 10	during non-SECAM	V_{10-1}	–	1,6	0,5	V
Voltage at pin 10	during SECAM	V_{10-1}	2,1	2,6	3,1	V
Output impedance at pin 10	during SECAM	$\|Z_{10-1}\|$	1,35	1,60	1,85	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle detector and clamp pulse generator	pin 7					
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V
Input current	V_{7-1} = 0,7 V	I_7	–	–30	–100	μA
Pulse width	see Fig. 3 pulse A		1,85	2,35	2,85	μs
Required pulse width	note 5, see Fig. 3 pulse B		0,6	–	–	μs

Notes to the characteristics

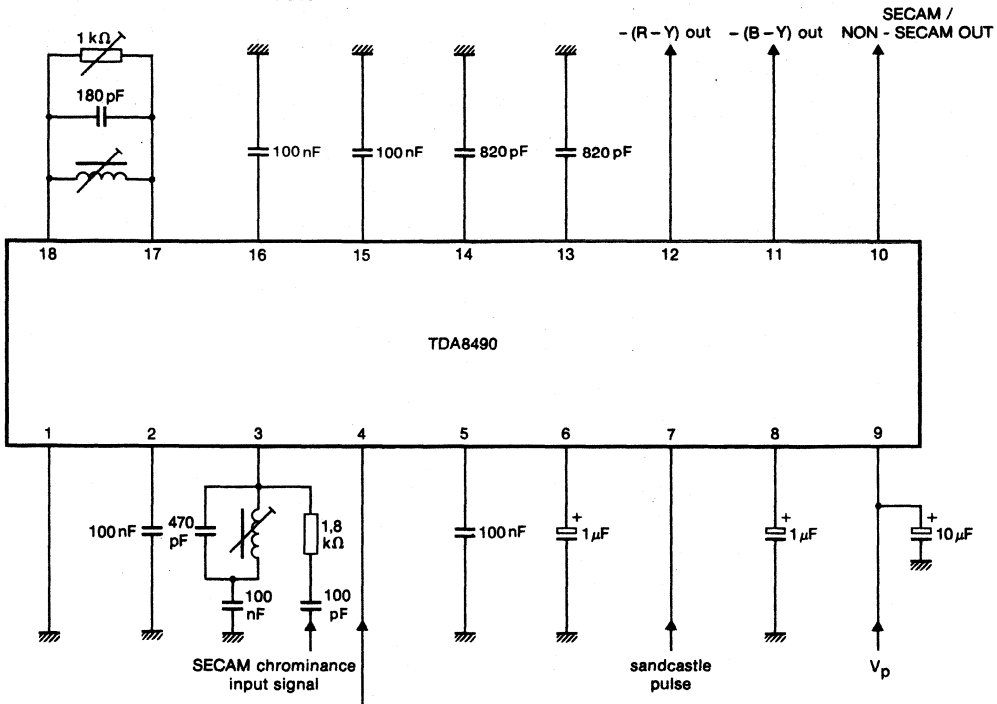
1. For alignment of the reference tuned circuit the input signal on pin 3 must be a SECAM signal at 100 mV(p-p) without deviation during a red and a blue line (black colour information, SECAM). The reference tuned circuit must be aligned to generate a colour output which corresponds to the new reinserted black level information.
2. If the input signal of the limiter is changed from 300 mV(p-p) to 15 mV(p-p), the zero point of the chrominance FM demodulator (f_o is typically 4,33 MHz) will typically shift by 5 kHz.
3. Definition of R-Y linearity = $V_{out\ cyan}/V_{out\ red}$:
   - $f_{nom\ cyan}$ = 4,68 MHz
   - $f_{nom\ red}$ = 4,12 MHz
4. Definition of B-Y linearity = $V_{out\ yellow}/V_{out\ blue}$:
   - $f_{nom\ yellow}$ = 4,02 MHz
   - $f_{nom\ blue}$ = 4,48 MHz
5. The burst gate pulse width must be larger than (2,85 + 0,6)=3,45 μs.
6. Demodulated black level at temperature X = A and at temperature Y = B.
   Artifical black level at temperature X = C and at temperature Y = D.
   Demodulated output signal ($f_o - \Delta f$) at temperature X = E1 and at temperature Y = F1.
   Demodulated output signal ($f_o + \Delta f$) at temperature X = E2 and at temperature Y = F2.

   $$E = \frac{E1 - E2}{2} \text{ and } F = \frac{F1 - F2}{2}$$

   $$\text{specification result} = \frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y\text{-}X} \times \Delta f\ (kHz)/^{o}C)$$

   for B-Y $f_o = f_{ob}$ = 4,25 MHz and Δf = 230 kHz.
   for R-Y $f_o = f_{or}$ = 4,40625 MHz and Δf = 280 kHz.
7. Due to different deviations (230 or 280 kHz) and correction figures (1,9 or 1,5 x) the total B-Y signal path needs a gain, which is 1,55 x higher than the R-Y path.

APPLICATION INFORMATION



$V_{4-1} < 3V$: frame identification.
$V_{4-1} > 4V$: line identification.
sandcastle pulse : line and frame identification.

Fig. 6 Application diagram.

DEVELOPMENT DATA

Philips Semiconductors

Data sheet	
status	Preliminary specification
code	
date of issue	March 1991

TDA8702/TDA8702T

8-bit video digital-to-analog converter

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ Z_L = 75 Ω	−1.45 −0.72	−1.60 −0.80	−1.75 −0.88	V V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		30	-	-	MHz
B	−3 dB bandwidth	f_{CLK} = 30 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38GE1
TDA8702T	16	SO16	plastic	SOT162A

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

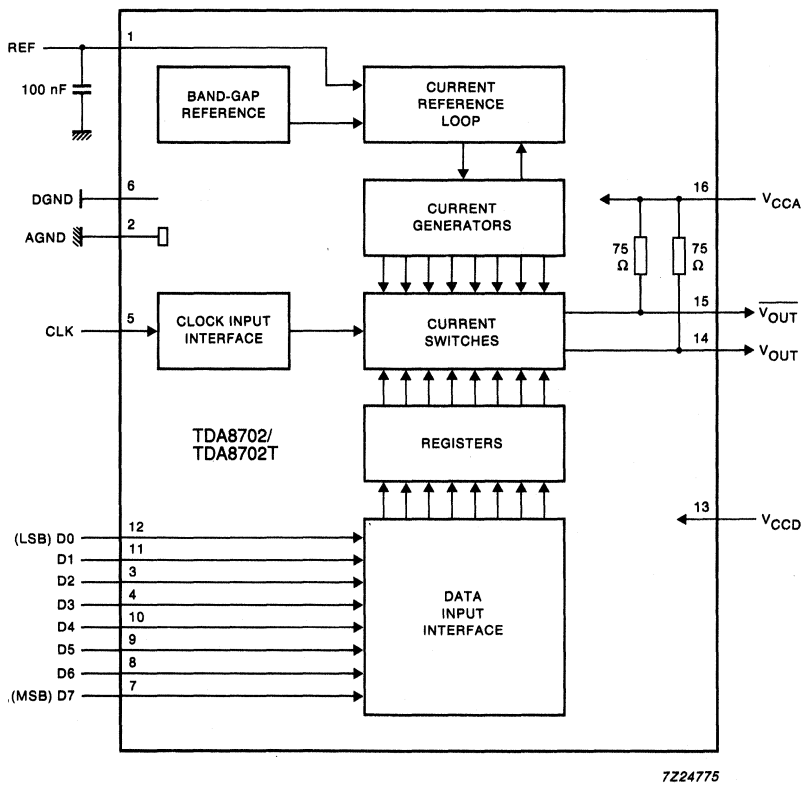


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDA8702/TDA8702T

PIN CONFIGURATION

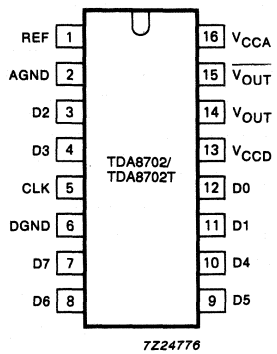


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	− 0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	− 0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	− 0.5	+ 0.5	V
AGND – DGND	ground voltage differential	− 0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	− 0.3	V_{CCD}	V
I_{14}/I_{15}	total output current range (pins 14 and 15)	− 5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	junction temperature	-	+125	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT38GE1	+ 85	K/W
$R_{th\ j\text{-}a}$	SOT162A	+110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to 70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	+0.1	V
Inputs DIGITAL INPUTS (D7 – D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		30	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
	(peak- to-peak value)	$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; f_{CLK} = 30 MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3 4 and 5)						
$t_{SU;\,DAT}$	data set-up time		−0.3	-	-	ns
$t_{HD;\,DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\,DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

CODE	BINARY INPUT DATA (D7 – D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT} (V)	$V_{\overline{OUT}}$ (V)	V_{OUT} (V)	$V_{\overline{OUT}}$ (V)
0	000 00 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	.....				
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	.....				
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

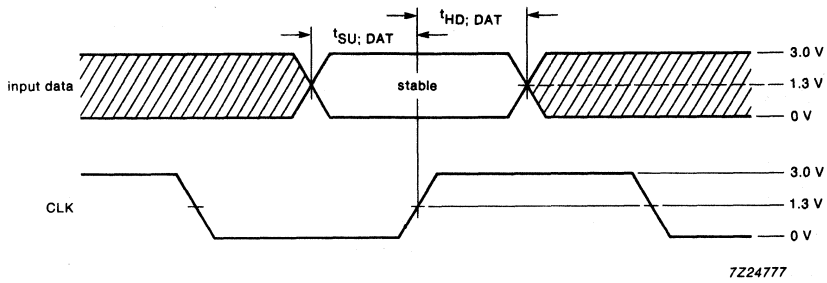


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; –0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

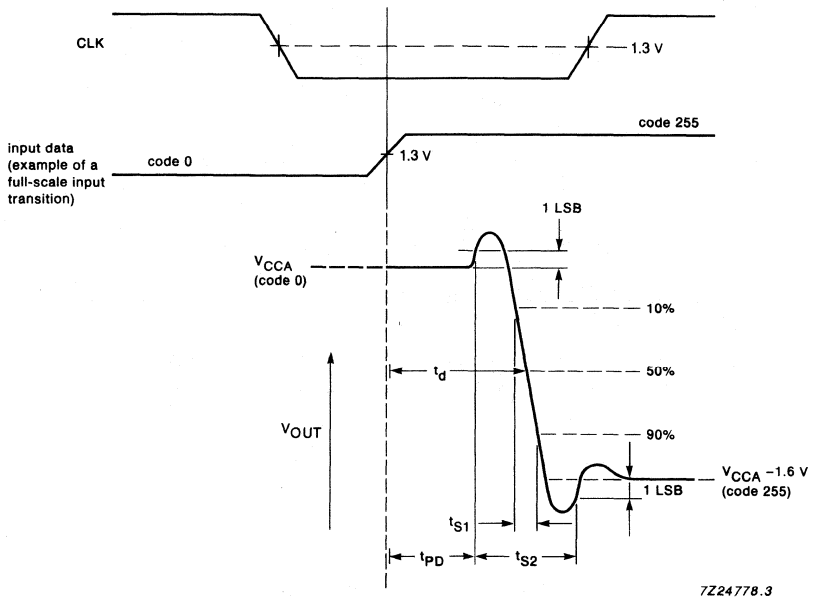


Fig.4 Switching characteristics.

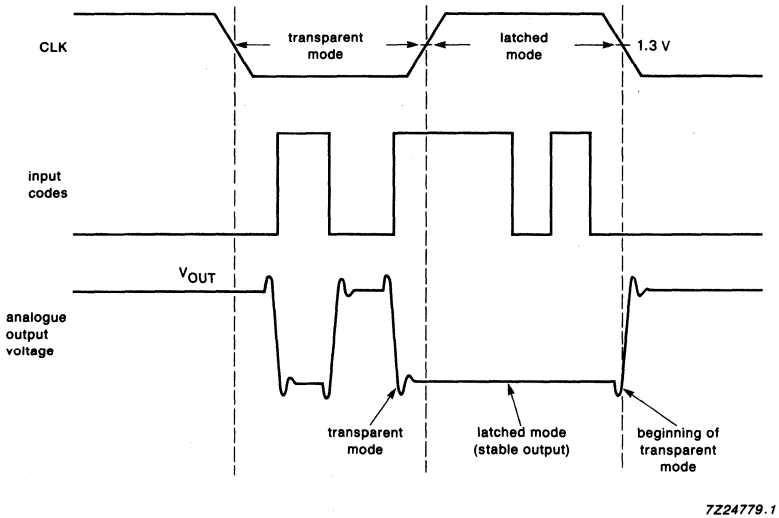


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

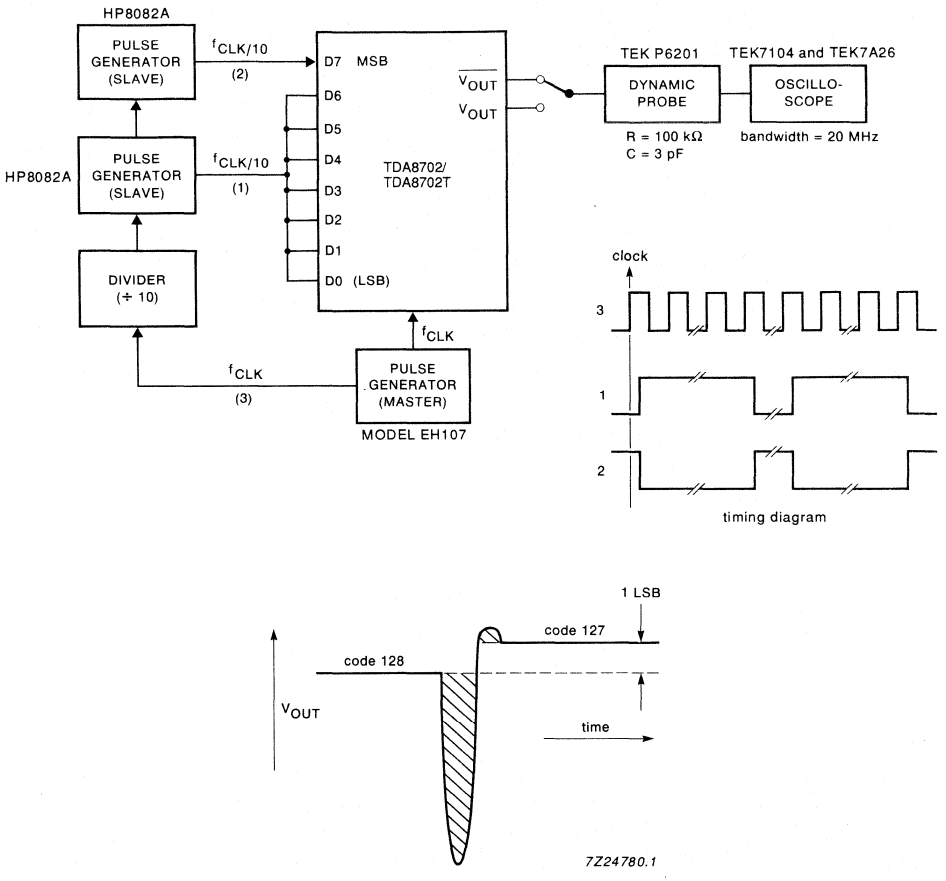


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

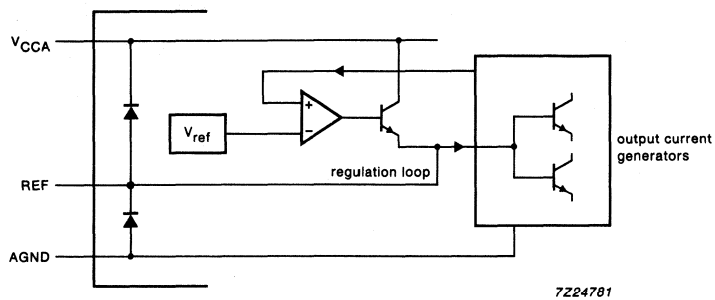


Fig. 7 Reference voltage generator decoupling.

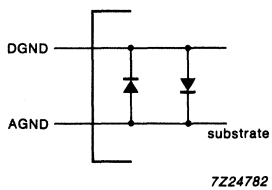


Fig.8 AGND and DGND.

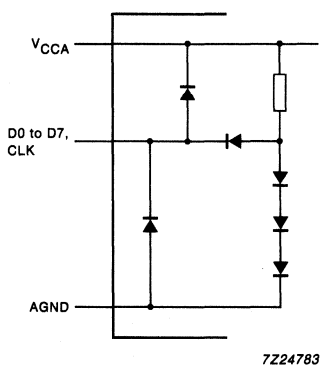


Fig.9 D7 to D0 and CLK.

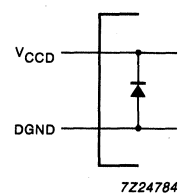


Fig.10 Digital supply.

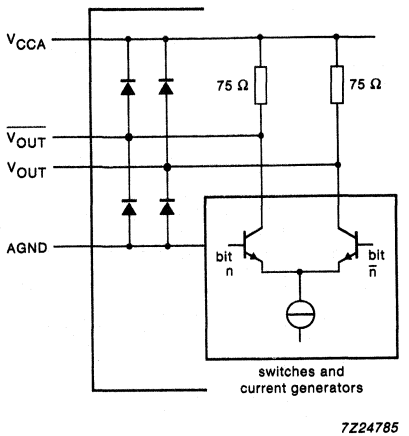


Fig.11 Analog outputs.

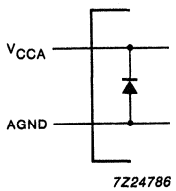


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

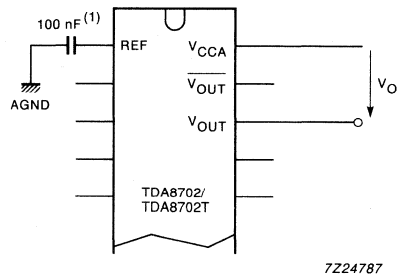


Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).

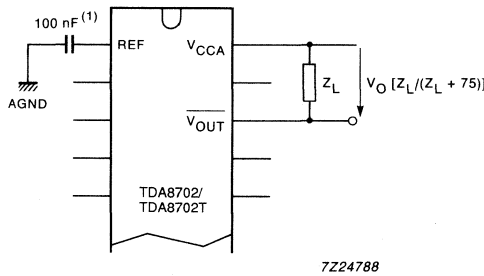


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

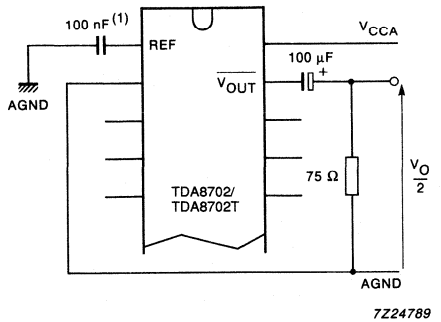


Fig.15 Analog output with AGND as reference.

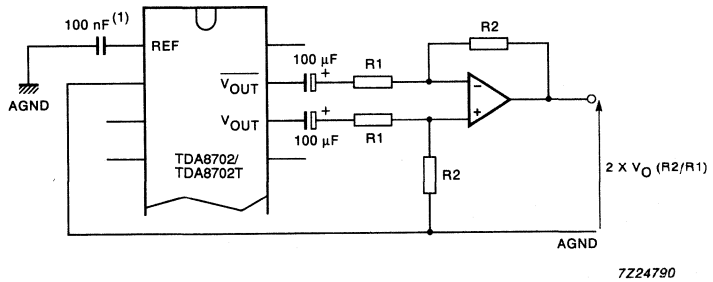


Fig.16 Differential mode (improved supply voltage ripple rejection).

Note to Figs 13, 14,15 and 16

1. This is a recommended value for decoupling pin 1.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	March 1991

TDA8703/TDA8703T

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

General purpose video signal decoder

DESCRIPTION

The TDA8703 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		-	28	36	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 1	-	-	± 2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

8-bit high-speed analog-to-digital converter TDA8703/TDA8703T

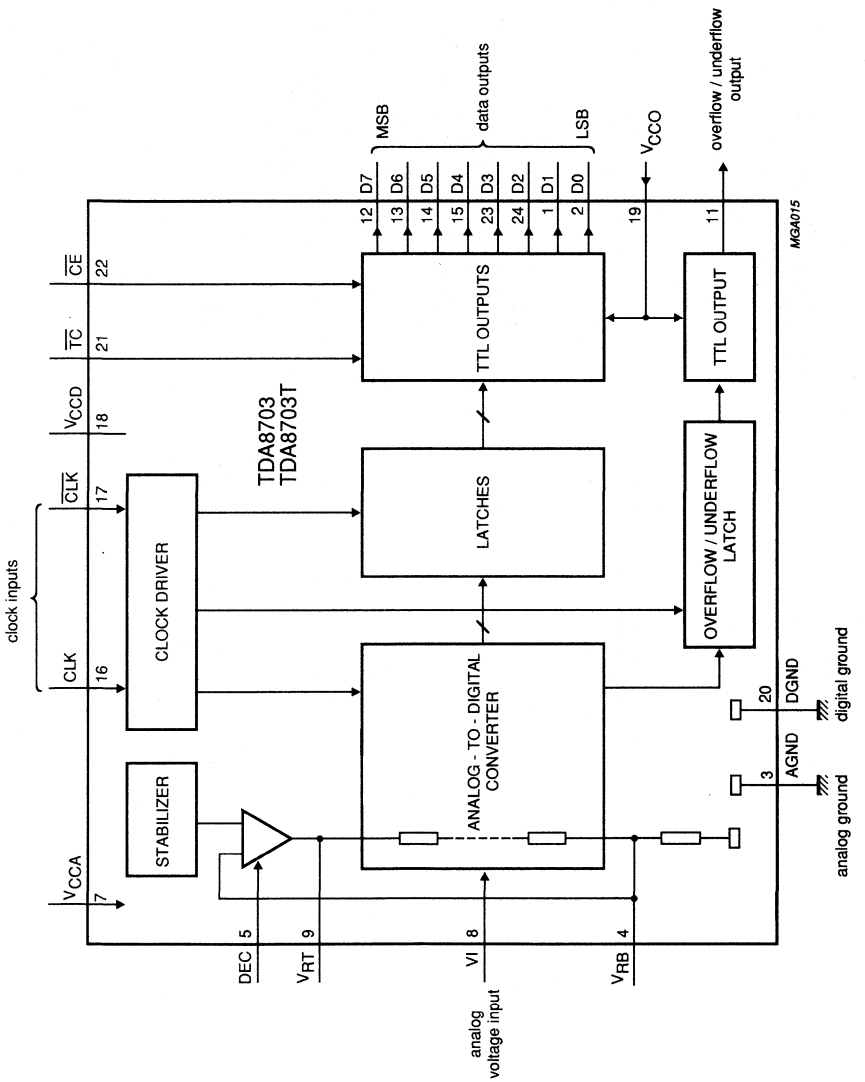


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDA8703/TDA8703T

PIN CONFIGURATION

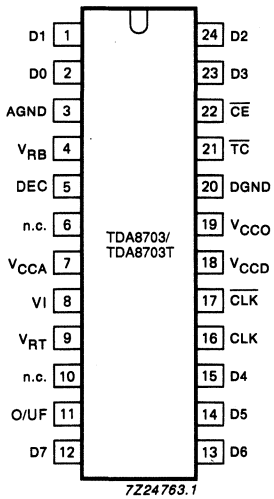


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range		−0.3	7.0	V
V_{CCD}	digital supply voltage range		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}$/ $V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	see note; referenced to DGND	-	2.0	V
I_O	output current		-	+ 10	mA
T_{stg}	storage temperature range		−55	+ 150	°C
T_{amb}	operating ambient temperature range		0	+ 70	°C
T_j	junction temperature		-	+ 125	°C

Notes to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j-a}$	SOT101	+ 55	K/W
$R_{th\ j-a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		-	28	36	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs CLOCK INPUT $\overline{CLK}$ AND CLK (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}}$ = 0.4 V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}}$ = 0.4 V $V_{CLK}/V_{\overline{CLK}}$ = V_{CCD}	- -	- -	100 300	µA µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}}$ = 10 MHz	-	4	-	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}}$ = 10 MHz	-	4.5	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.47	1.57	1.66	V
V_{OS}	offset voltage	$V_{VI(0)} - V_{VI(B)}$	0.14	-	0.18	V
$V_{VI(T)}$	input voltage (top)		3.2	3.37	3.52	V
$V_{VI(255)}$	input voltage	output code = 255	3.16	3.33	3.47	V
V_{OS}	offset voltage	$V_{VI(T)} - V_{VI(255)}$	0.04	-	0.05	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.72	1.79	1.85	V
I_{IL}	input current LOW	$V_{VI} = 1.4$ V	-	0	-	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	input current HIGH	V_{VI} = 3.6 V	60	120	180	µA
Z_o	input impedance	f_i = 1 MHz	-	10	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	14	-	pF
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	-	220	-	Ω
Outputs DIGITAL OUTPUTS (D7 – D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	-	20	µA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		40	-	-	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	–3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.6	-	%
ϕ_d	differential phase	note 4	-	0.8	-	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	-	-	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	-	–55	-	dB
SVR1	supply voltage ripple rejection	note 5	-	–28	–25	dB
SVR2	supply voltage ripple rejection	note 5	-	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 6	-	-	± 2	LSB
	effective bits	f_i = 4.43 MHz	-	7.1	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: $SVR1 = 20 \log (\Delta V_{VI(127)} \div \Delta V_{CCA})$
   - SVR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: $SVR2 = \{\Delta[V_{VI(0)} - V_{VI(255)}] \div [V_{VI(0)} - V_{VI(255)}]\} \div \Delta VCCA$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus, it is recommanded that acquisition of this data is made after the falling edge of the clock, instead of after the max (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND)

			BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.65	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.65	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.45	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.45	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 – D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where:

X = don't care.

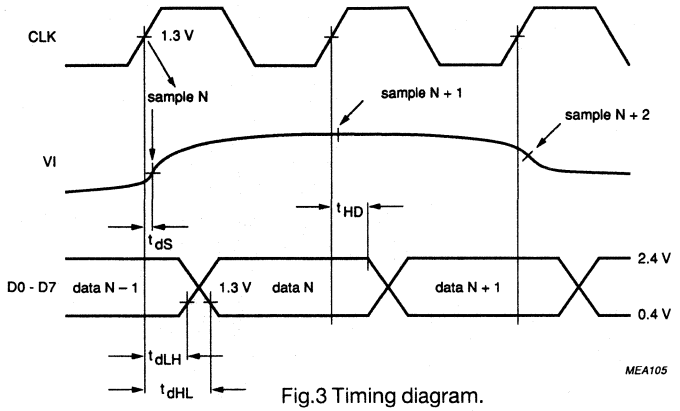


Fig.3 Timing diagram.

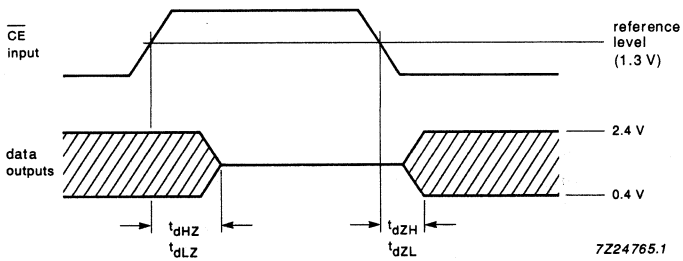


Fig.4 3-state delay timing diagram.

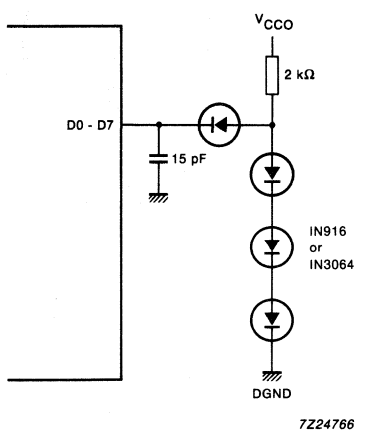


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

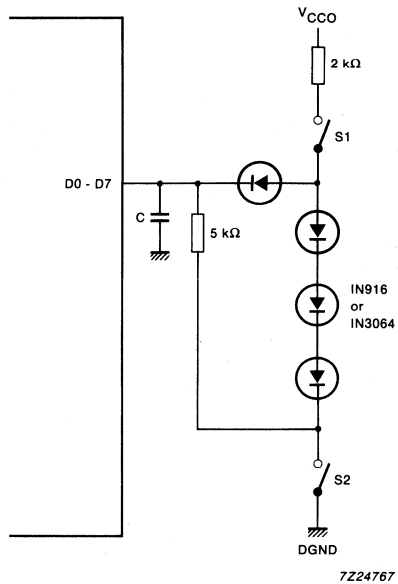


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

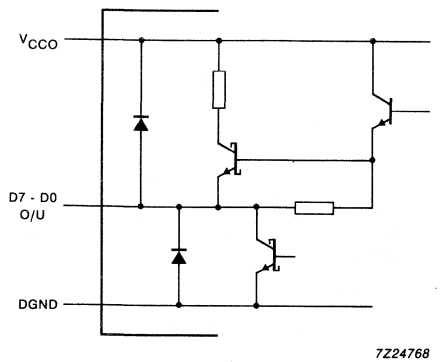


Fig.7 TTL data and overflow/underflow outputs.

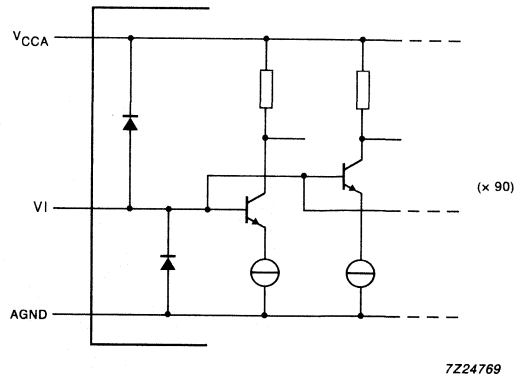


Fig.8 Analog inputs.

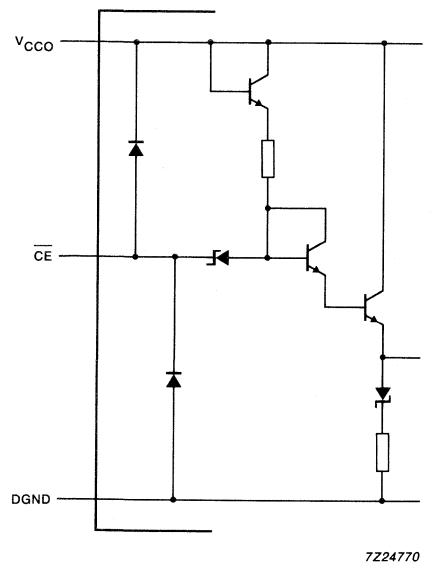


Fig.9 $\overline{CE}$ (3-state) input.

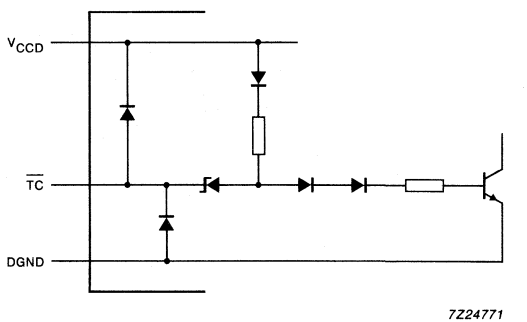


Fig.10 $\overline{TC}$ (two's complement) input.

INTERNAL PIN CONFIGURATIONS (continued)

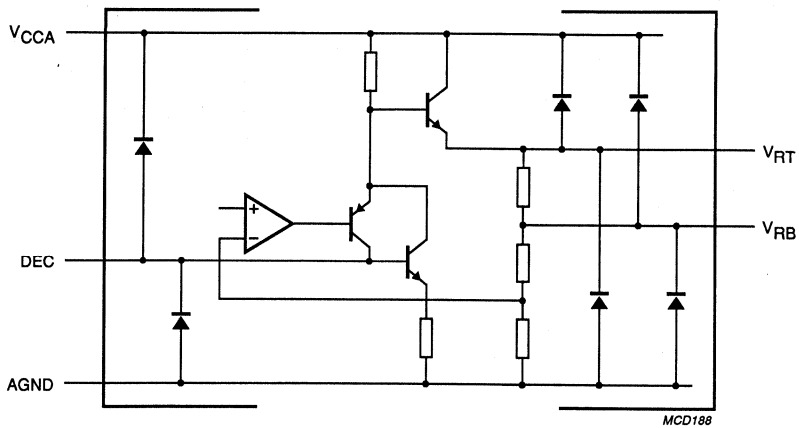


Fig.11 V_{RB}, V_{RT} and DEC.

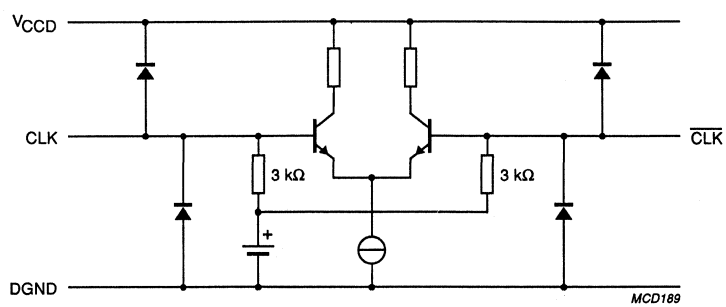


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

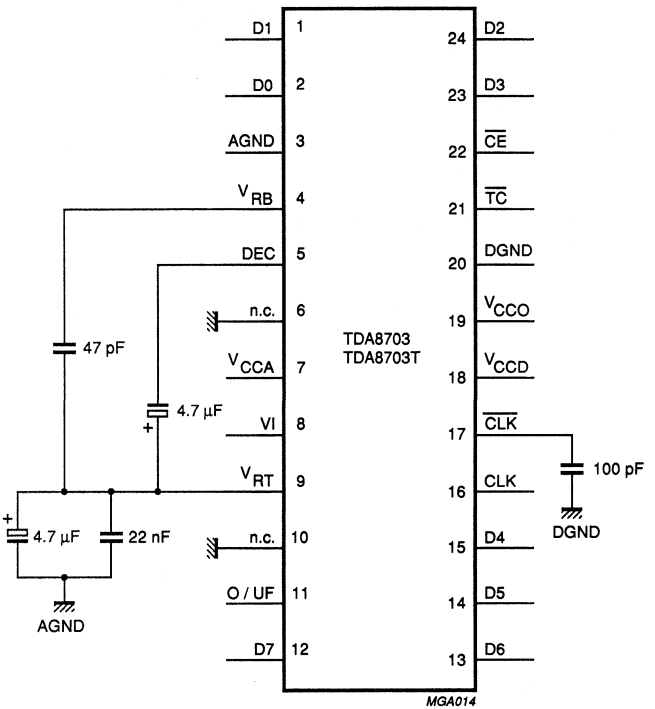


Fig.13 Application diagram.

Notes to Fig.13

1. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

Video analog input interface TDA8708

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS signal
- No sample-and-hold circuit required

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing

DESCRIPTION

The TDA8708 is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.5	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708	28	DIL	plastic	SOT117
TDA8708	28	SO28	plastic	SOT136A

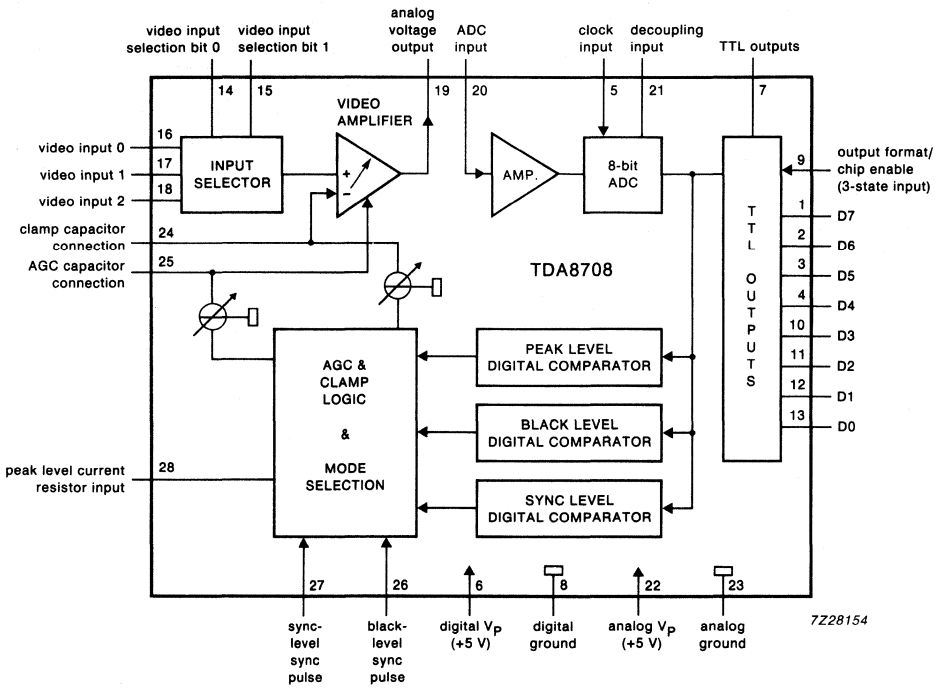


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

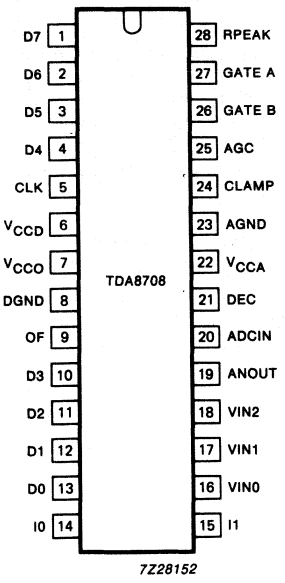


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

FUNCTIONAL DESCRIPTION

The TDA8708 provides a simple interface for decoding video signals.

The TDA8708 operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708 automatically switches to configuration mode 2.

When the TDA8708 is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 240, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	125	–	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55	-	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136)	70	-	K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.5$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current		–	12	16	mA
Video amplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.45	1.0	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
RPEAK INPUT (PIN 28)						
I_{28}	minimum peak level current	$R_{28} = 0\ \Omega$	–	80	150	µA
AGC INPUT (PIN 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
CLAMP INPUT (PIN 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
I_{19}	internal current source		2.0	2.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ANOUT OUTPUT (PIN 19)						
V_{19}	output DC voltage for black level	note 1	–	V_{CCA} –2.95	–	V
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1 V(p-p); V_{25} = 3.6 V	–	1.0	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
	crosstalk between VIN inputs		–	–60	–55	dB
G_d	differential gain		–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 2	60	–	–	dB
SVRR	supply voltage ripple rejection	note 3	–	45	–	dB
ΔG	gain range		–4.5	–	6.0	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	input current HIGH	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state) (see Table 4)						
V_{IL}	input voltage LOW		0	–	0.2	V
V_{IH}	input voltage HIGH		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	input current LOW		–370	–300	–	μA
I_{IH}	input current HIGH		–	360	450	μA
ADCIN INPUT (PIN 20) (SEE TABLE 5)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_L	output voltage LOW	I_O = 2 mA	0	–	0.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIGITAL OUTPUTS D(0-7)						
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz)						
B	–3 dB bandwidth	note 4	–	12	–	MHz
G_d	differential gain	note 5; Fig.3	–	2	–	%
ϕ_d	differential phase	note 5; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 5	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43MHz; note 5	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 6	–	1	5	%/V
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 7	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz) (see Fig.6)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{ds}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable	see Fig.7	–	19	25	ns
t_{dDZ}	3-state delay time - output disable	see Fig.7	–	14	20	ns

Notes to the characteristics

1. Control mode 2 is selected.
2. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT}(p\text{–}p)}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

3. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$ for V_i = 1 V (peak-to-peak), 100 kHz gain = 1 and 1 V supply variation.

4. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
5. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).

Notes to the characteristics

6. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] \div [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

7. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 µA I_{PEAK}	1
0	X	output < 240 output > 240	0 I_{PEAK}	2
1	0	output < 0 0 < output < 240 output > 240	+2.5 µA −2.5 µA I_{PEAK}	2

Note

Where; X = don't care

Table 3 CLAMP output current

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	I_{PEAK} −2.5 µA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 µA −50 µA	2

Note

Where; X = don't care

Table 4 OF input coding

OF	D0 TO D7
0	active, two's complement
1	high impedance
open (see note)	active, binary

Note

Use C ≥ 10 pF to DGND

Table 5 ADC output current

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

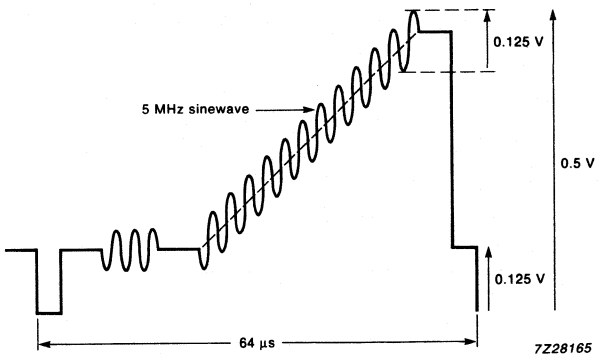


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

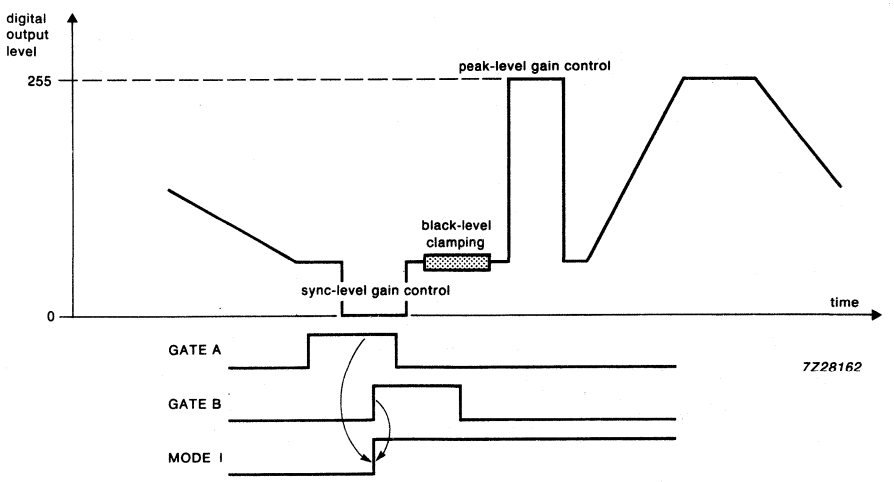


Fig.4 Control mode 1.

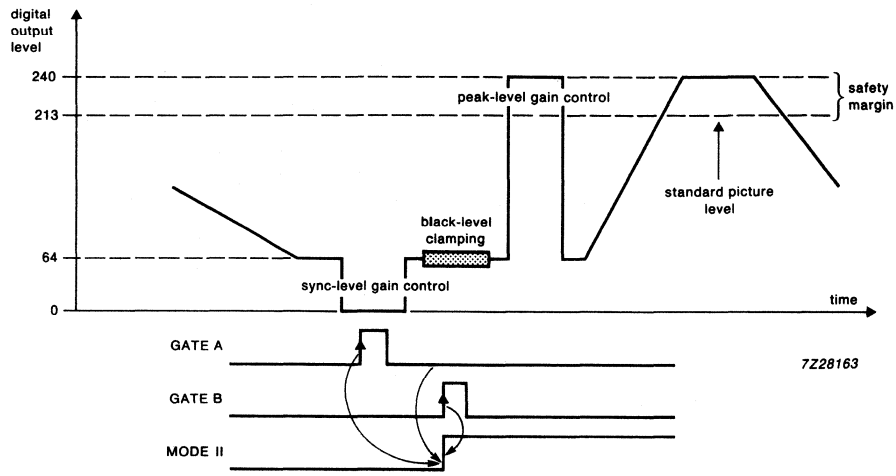


Fig.5 Control mode 2.

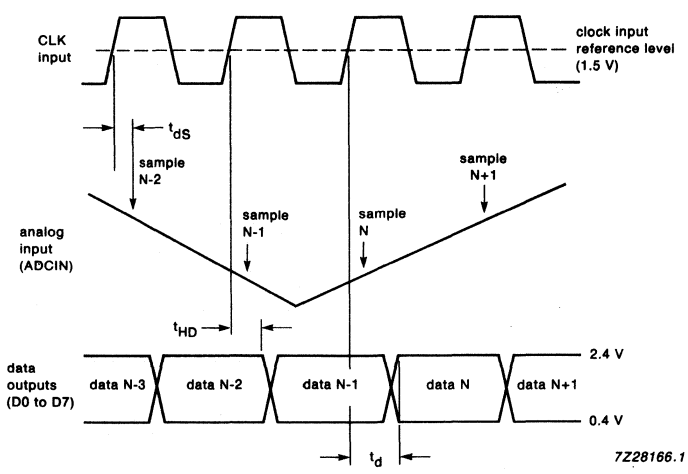


Fig.6 Timing diagram.

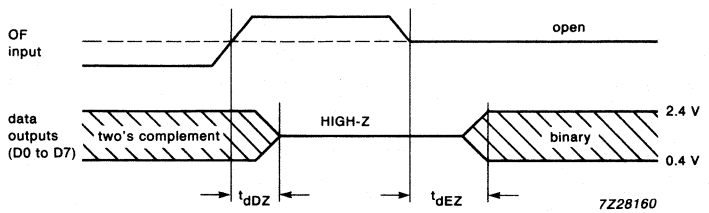


Fig.7 Output format timing diagram.

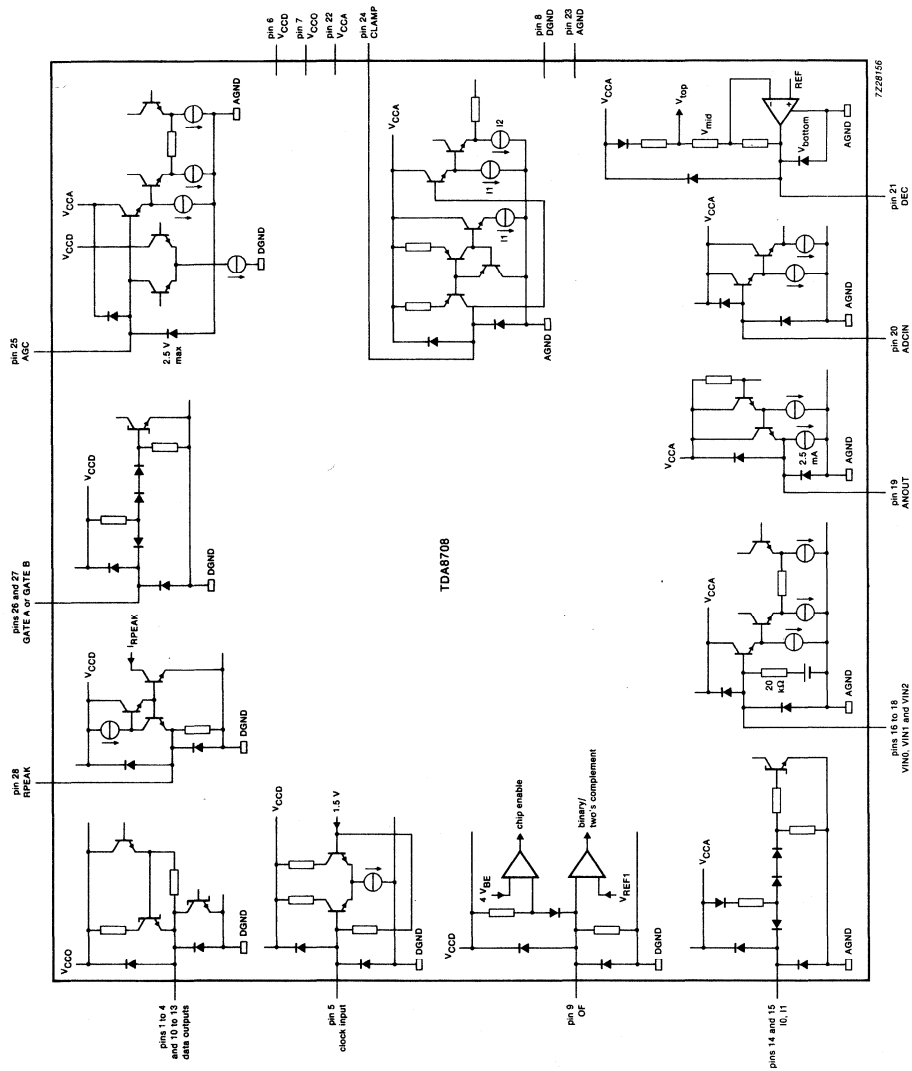
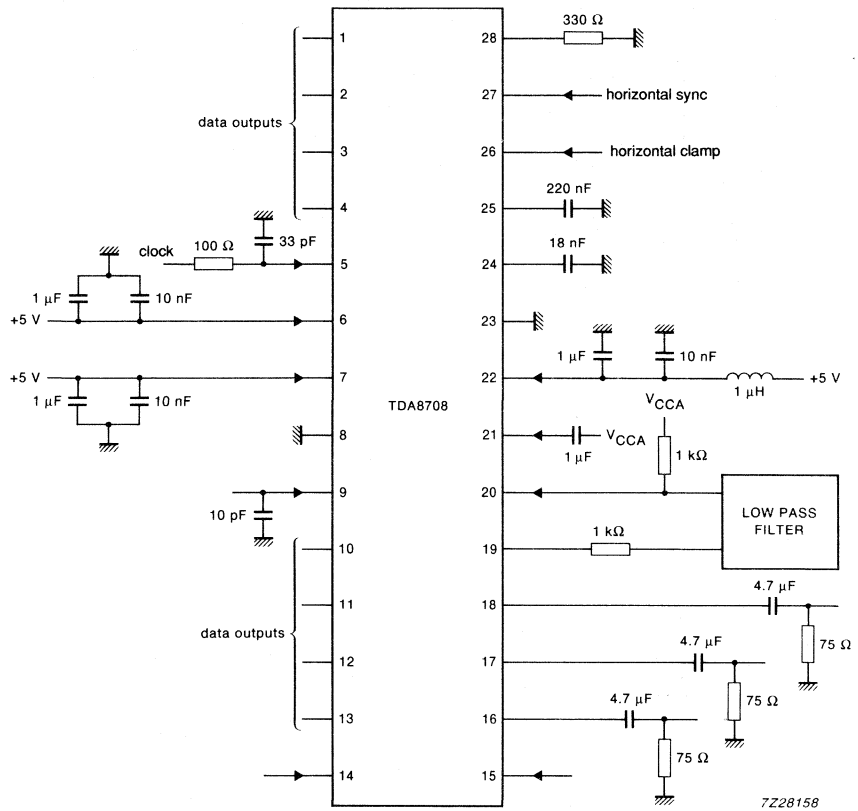


Fig.8 Internal pin configuration.

APPLICATION INFORMATION



Additional information can be found in the laboratory report FTV/8902.

Fig.9 Application diagram.

Video analog input interface TDA8709

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- Y, R, G, B signals
- Chrominance signal (C)

DESCRIPTION

The TDA8709 is a bipolar analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.5	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709	28	DIL	plastic	SOT117
TDA8709	28	SO28	plastic	SOT136A

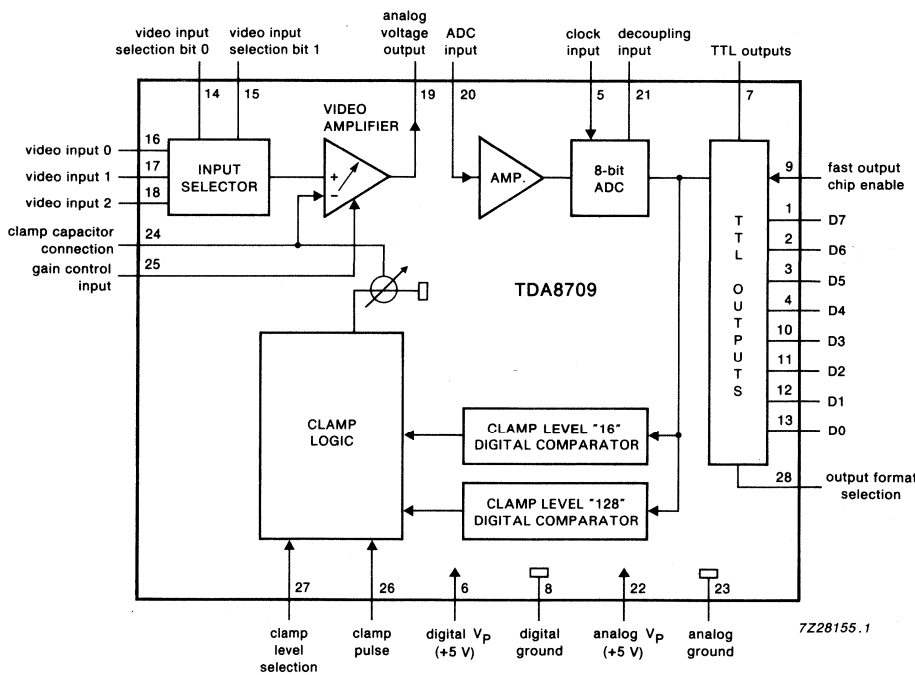


Fig.1 Block diagram.

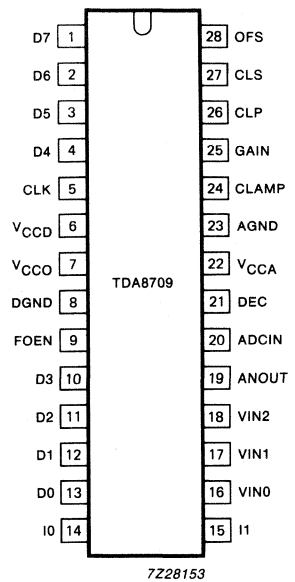


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

FUNCTIONAL DESCRIPTION

The TDA8709 is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for luminance or R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chose value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	125	−	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55	-	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136)	70	-	K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.5$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current		–	12	16	mA
Preamplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.3	1	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
CLS, OFS, CLP, TTL INPUTS (SEE FIG 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
GAIN INPUT (PIN 25)						
V_{25}	voltage for minimum gain	(see Fig.3)	–	1.5	–	V
V_{25}	voltage for maximum gain	(see Fig.3)	–	4.2	–	V
I_I	input current		–	1.0	–	µA
	stability gain/temperature		–	6	–	%
CLAMP INPUT (PIN 24)						
I_{24}	CLAMP output current	see Table 2	–	–	–	
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
I_{19}	internal current source		2.0	2.5	–	mA
V_{19}	output DC voltage for black level	CLS = logic 1	–	$V_{CCA}-2.65$	–	V
V_{19}	output DC voltage for black level	CLS = logic 0	–	$V_{CCA}-3.1$	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1 V(p-p); V_{25} = 3 V	–	1.0	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
	crosstalk between VIN inputs	note 1	–	–60	–55	dB
G_d	differential gain		–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 2	60	–	–	dB
SVRR	supply voltage ripple rejection	note 3	–	45	–	dB
ΔG	gain range		–4.5	–	10	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	input current HIGH	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
FOEN TTL input (see Table 3)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	input current HIGH	V_9 = 2.7 V	–	–	+20	μA
ADCIN INPUT (PIN 20) (SEE TABLE 4)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_{OL}	output voltage LOW	I_O = 2 mA	0	–	0.6	V
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz)						
B	–3 dB bandwidth	note 4	–	12	–	MHz
G_d	differential gain	note 5; see Fig.4	–	2	–	%
ϕ_d	differential phase	note 5; see Fig.4	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 5	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43MHz; note 5	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 6	–	1	5	%/V
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 7	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable	see Fig.7	–	16	25	ns
t_{dDZ}	3-state delay time - output disable	see Fig.7	–	12	25	ns

Notes to the characteristics

1. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1 $V_{(p\text{-}p)}$
2. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT}(p\text{-}p)}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

3. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for V_i = 1 V (peak-to-peak), 100 kHz gain = 1 and 1 V supply variation.

4. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
5. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
6. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

7. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $\overline{f_{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128 output > 128	–50 µA –50 µA
X	0	X	0
0	1	output < 16 16 < output	+50 µA –50 µA

Note

Where; X = don't care

Table 3 FOEN input current

FOEN	D0 TO D7
0	active
1	high impedance

Table 4 ADC output current

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

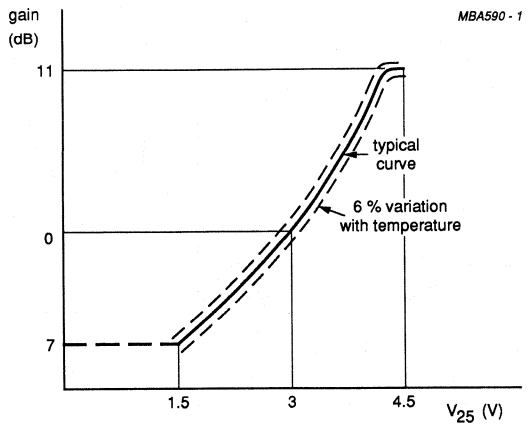


Fig.3 Typical gain control curve as a function of gain voltage.

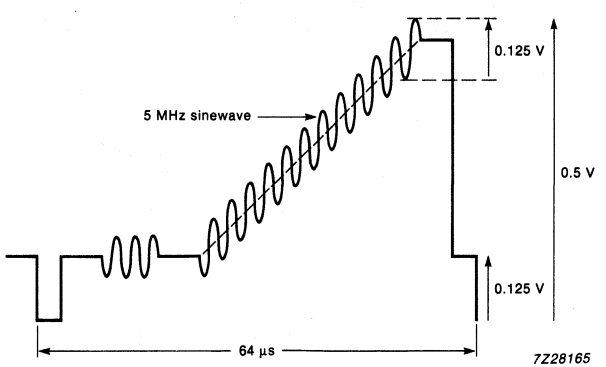


Fig.4 Test signal on the ADCIN pin for differential gain and phase measurements.

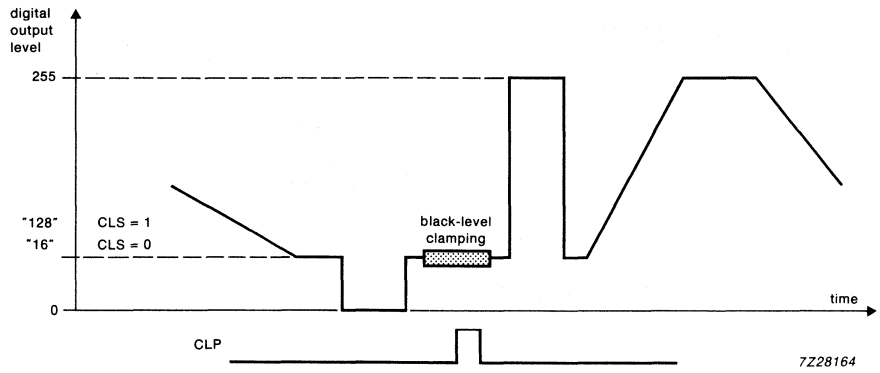


Fig.5 Control mode selection.

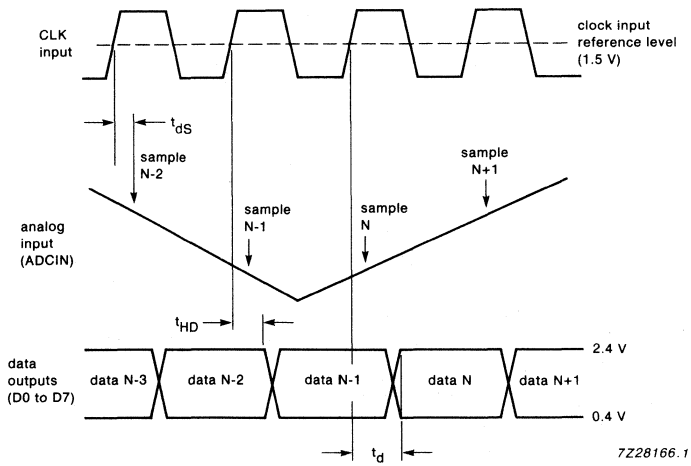


Fig.6 Timing diagram.

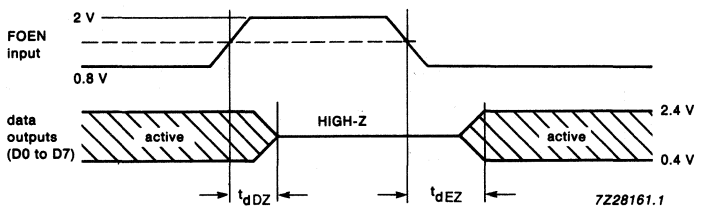


Fig.7 Output format timing diagram.

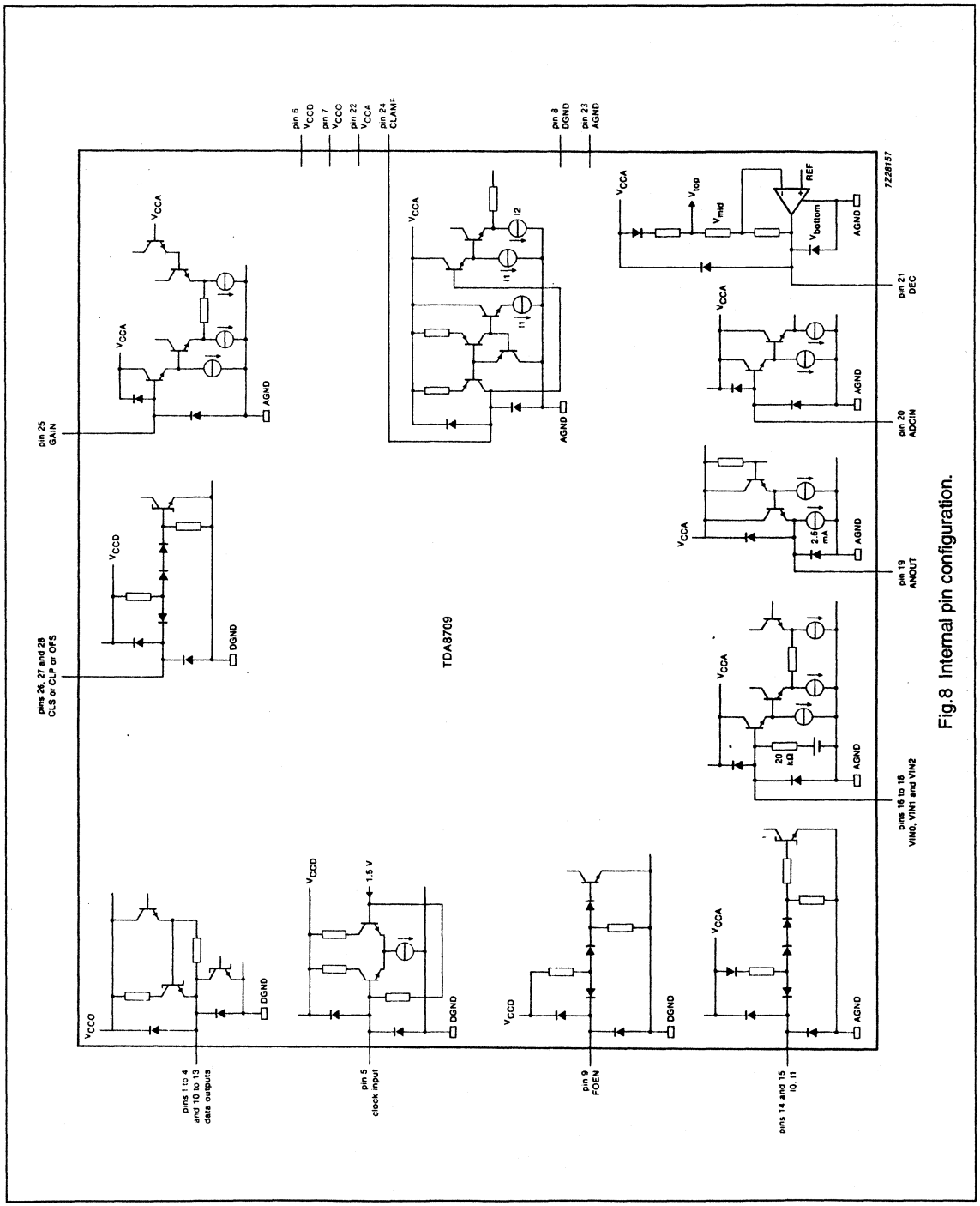
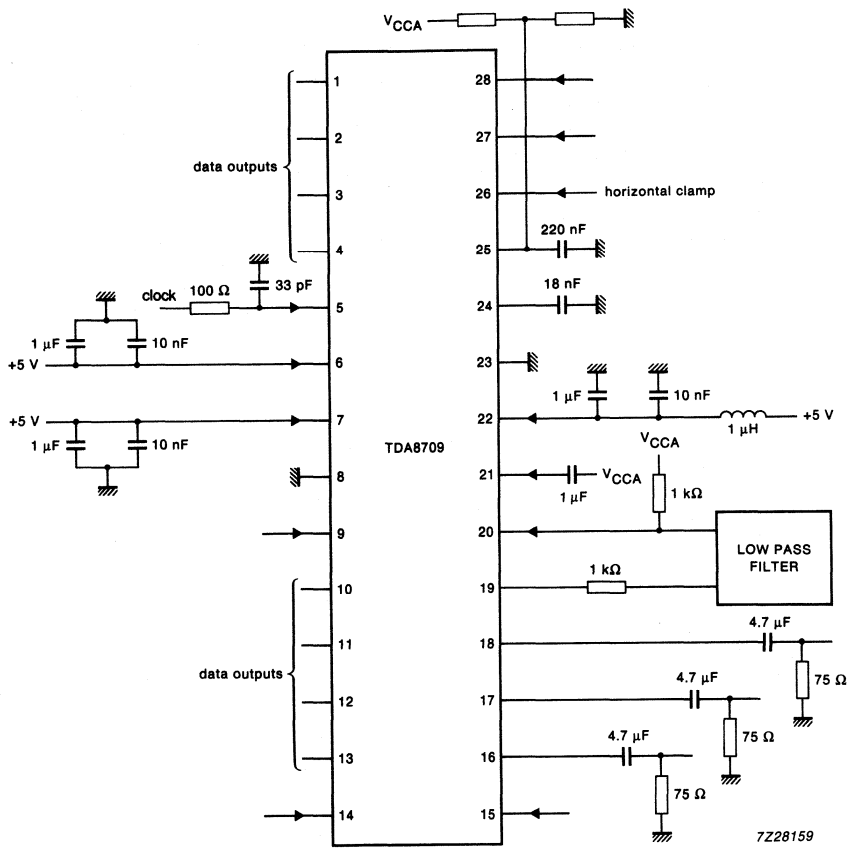


Fig.8 Internal pin configuration.

APPLICATION INFORMATION



Additional information can be found in the laboratory report FTV/9002.

Fig.9 Application diagram.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDA8713

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators
  - medical imaging

DESCRIPTION

The TDA8713 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8713	24	DIL	plastic	SOT101
TDA8713T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 1	-	-	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency	note 3	50	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).

2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).

3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak- to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

     If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

8-bit high-speed analog-to-digital converter TDA8713

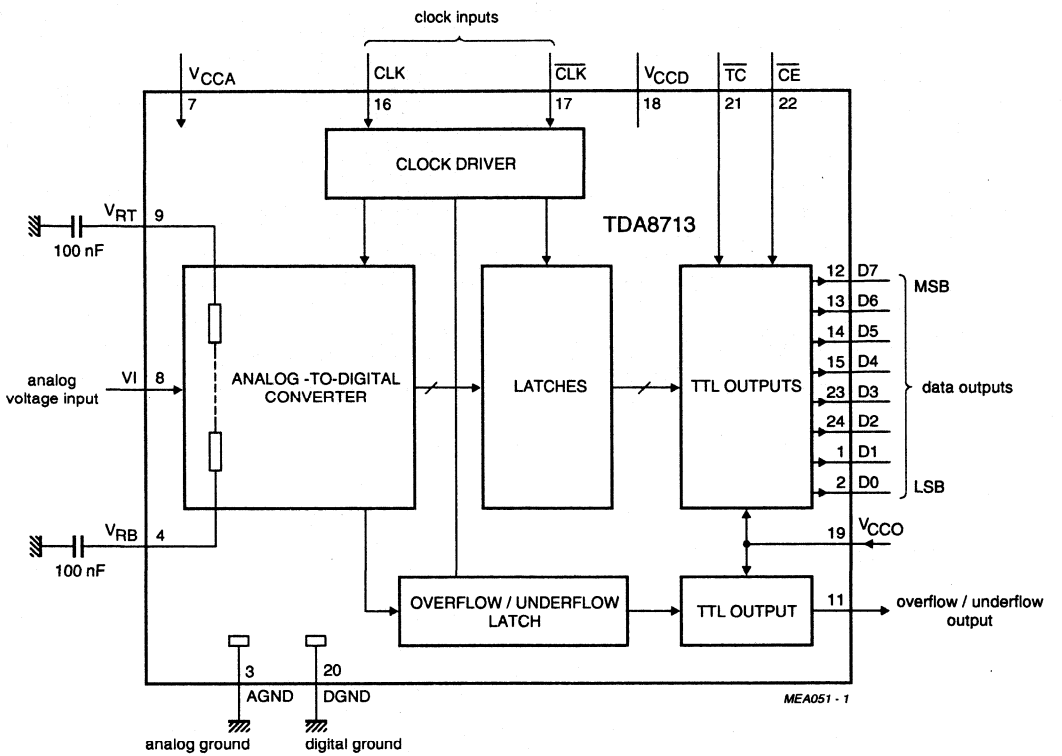


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDA8713

PIN CONFIGURATION

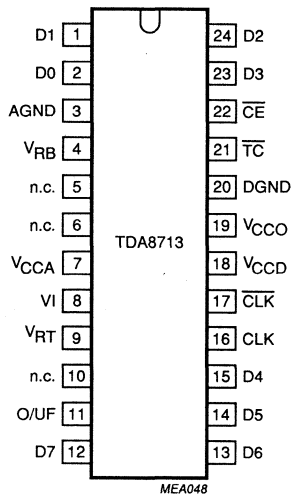


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
n.c.	5	not connected
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	see note 1	−0.3	7.0	V
V_{CCD}	digital supply voltage range	see note 1	−0.3	7.0	V
V_{CCO}	output stages supply voltage	see note 1	−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	1.2	7.0	V
$V_{\overline{CLK}}$ / V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note 2; referenced to DGND	-	2.0	V
I_O	output current		-	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		-	+125	°C

Notes to the Ratings

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 V and +7.0 V as long as the difference V_{CCA} - V_{CCD} lies between −1 V and + 1 V.

2. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

  If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT101	+ 55	K/W
$R_{th\ j\text{-}a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.75$ V to 5.25 V; $V_{CCD} = V_{18} - V_{20} = 4.75$ V to 5.25 V; $V_{CCO} = V_{19} - V_{20} = 4.75$ V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs CLOCK INPUT CLK AND $\overline{CLK}$ (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}} = 2.7$ V	-	-	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	-	-	300	µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4	-	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4.5	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
I_{IL}	input current LOW	$V_{VI} = 1.6$ V	-	0	-	µA
I_{IH}	input current HIGH	$V_{VI} = 3.8$ V	60	120	180	µA
Z_o	input impedance	$f_i = 1$ MHz	-	10	-	kΩ
C_i	input capacitance	$f_i = 1$ MHz	-	14	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		1.5	1.6	1.9	V
V_{RT}	reference voltage HIGH		3.5	3.8	3.9	V
V_{REF}	differential reference voltage V_{RT}-V_{RB}		2	2.2	-	V
I_{REF}	reference current		-	10	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 5	-	258	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 5	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 5	-	132	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 5	-	–0.3	-	mV/°C
Outputs DIGITAL OUTPUTS (D7 - D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	-	20	µA
Switching characteristics (note 1,2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	–3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.3	2.0	%
ϕ_d	differential phase	note 4	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	–65	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	–55	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 6	-	-	±2	LSB
EB	effective bits f_i = 1 MHz	f_{CLK} = 20MHZ	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 40MHZ	-	7.5	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHZ	-	7.2	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 50 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Analog input voltages producing code 00 up to and including FF
   - V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
   - V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
   - V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
   - V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.
6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.6 V, V_{RT} = 3.8 V)

			BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.858	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.858	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.668	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.668	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care.

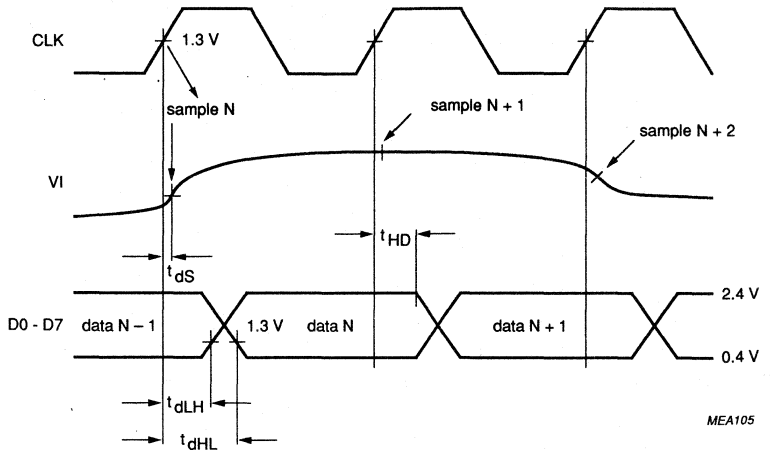


Fig.3 Timing diagram.

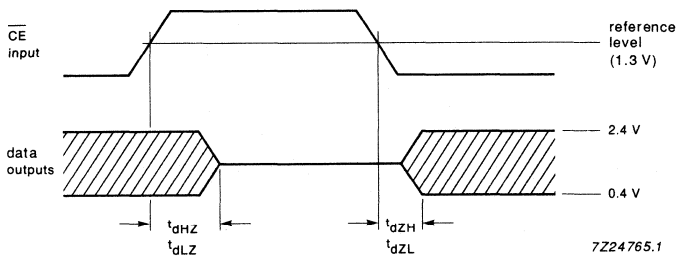


Fig.4 3-state delay timing diagram.

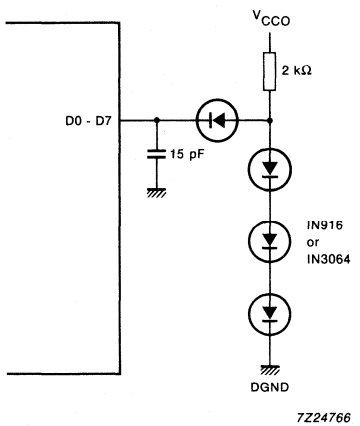


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

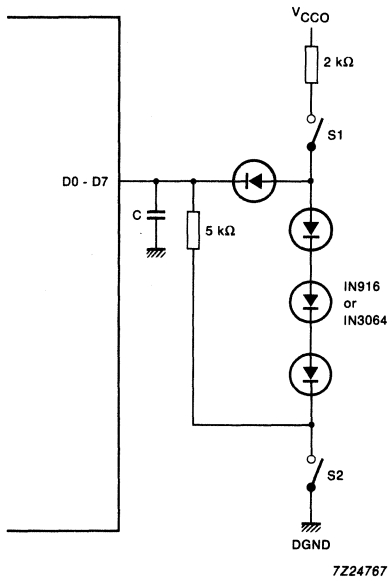


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V).

Note to Fig.6

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

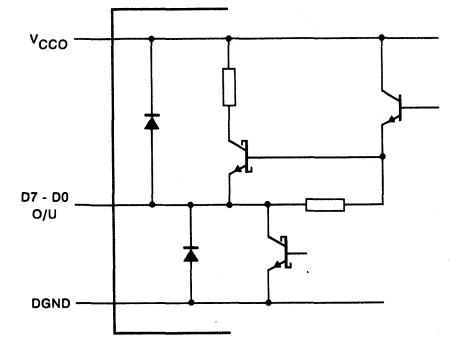


Fig.7 TTL data and overflow/underflow outputs.

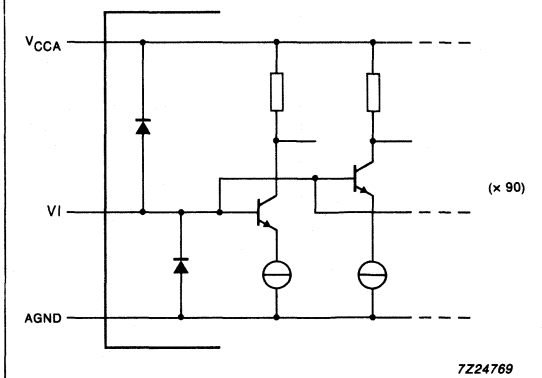


Fig.8 Analog inputs.

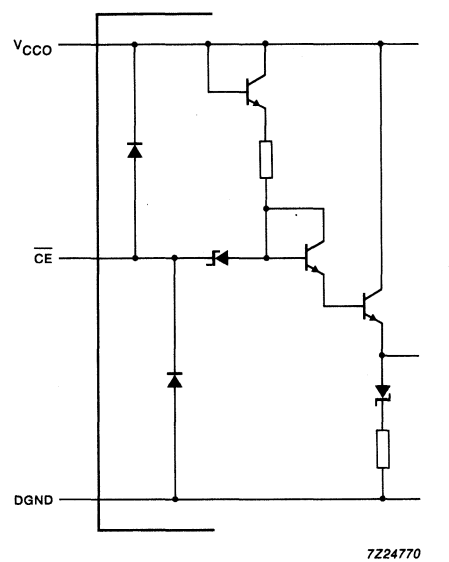


Fig.9 $\overline{CE}$ (3-state) input.

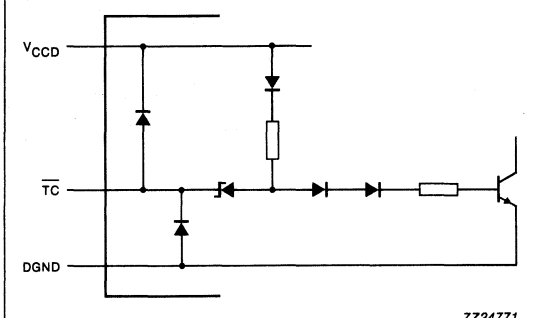


Fig.10 $\overline{TC}$ (two's complement) input.

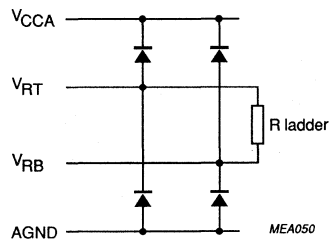


Fig.11 V_{RB}, V_{RT}.

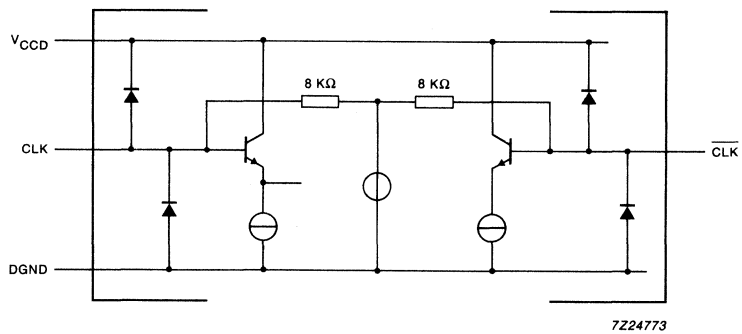


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/9001).

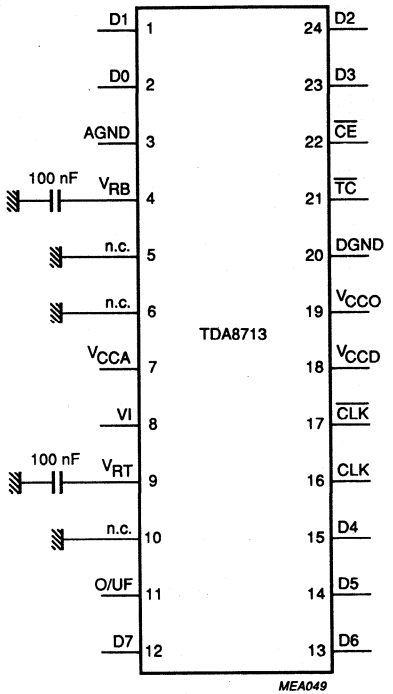


Fig.13 Application diagram.

Notes to Fig.13

1. $\overline{CLK}$ should be decoupled to the DGND with a 100 nF capacitor, if pin CLK is used (see 'Notes to the characteristics', note 1).

2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).

3. V_{RB} and V_{RT} are decoupled to AGND.

4. Analog and digital supplies should be separated and decoupled.

5. Pins 5,6 and 10 should be connected to AGND in order to prevent noise influence.

6. The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDA8715

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging

DESCRIPTION

The TDA8715 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for profesional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8715	18	DIL	plastic	SOT102
TDA8715T	20	SO20	plastic	SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	±0.4	±0.75	LSB
DLE	DC differential linearity error		-	±0.25	±0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		0	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

8-bit high-speed analog-to-digital converter TDA8715

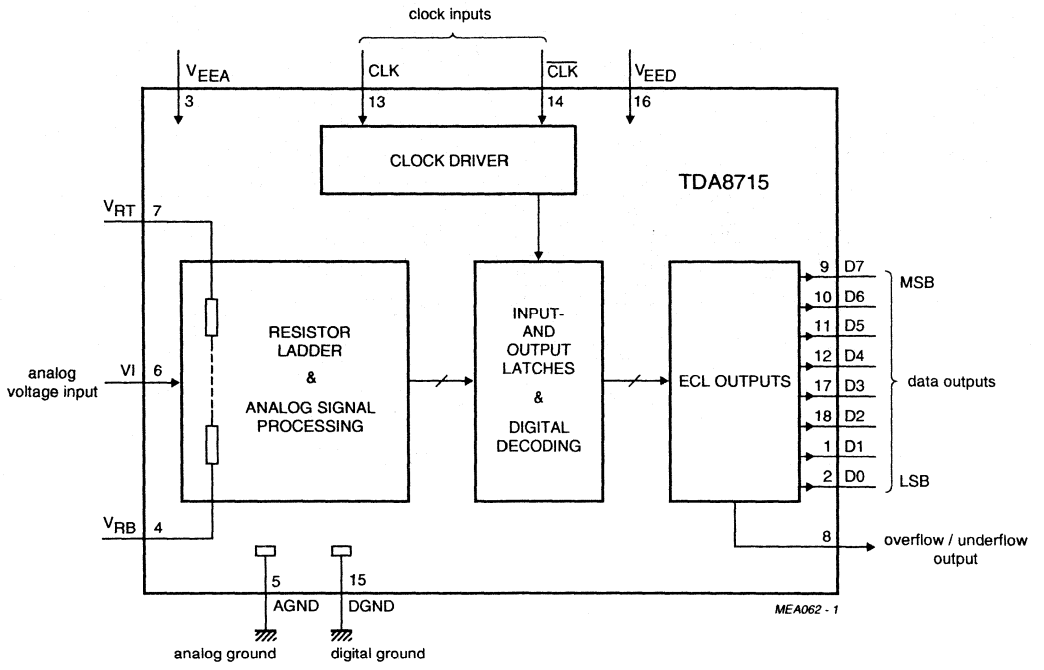


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDA8715

PIN CONFIGURATION

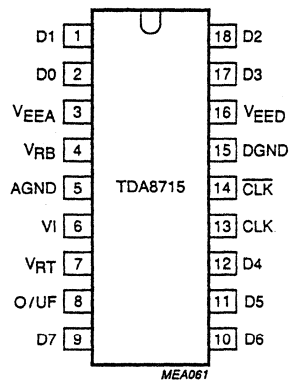


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (–5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (–5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	70	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT102	+65	K/W
$R_{th\ j\text{-}a}$	SOT163A	0	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{EEA} = V_3 - V_5 = -4.7$ V to -5.7 V; $V_{EED} = V_{16} - V_{15} = -4.7$ V to -5.7 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference V_{EEA} - V_{EED}		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		−3.2	−3.0	−2.7	V
V_{RT}	reference voltage HIGH		−0.9	−0.6	−0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.3	2.4	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	−0.3	-	mV/°C
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{CLK} = -1.77$ V	-	−240	-	µA
I_{IH}	input current HIGH	$V_{CLK} = -0.88$ V	-	−14	-	µA
R_i	input resistance	$f_{CLK} = 10$ MHz	-	7.0	-	kΩ
		$f_{CLK} = 50$ MHz	-	3.5	-	kΩ
C_i	input capacitance	$f_{CLK} = 10$ MHz	-	1.8	-	pF
		$f_{CLK} = 50$ MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}} = -1.77$ V	-	−140	-	µA
I_{IH}	input current HIGH	$V_{\overline{CLK}} = -0.88$ V	-	75	-	µA
R_i	input resistance	$f_{\overline{CLK}} = 10$ MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}} = 50$ MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}} = 10$ MHz	-	2.6	-	pF
		$f_{\overline{CLK}} = 50$ MHz	-	2.4	-	pF
$V_{\overline{CLK}(p\text{-}p)}$ − $V_{CLK(p\text{-}p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VI (analog input with V_{RB} = –3.1 V and V_{RT} = –0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	μA
I_{IH}	input current HIGH	data output FF	-	120	-	μA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	–1.95	–1.77	–1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	–0.96	–0.88	–0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	–3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	–60	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	–50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±0.5	LSB
AILE	AC integral linearity error	note 4	-	±0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.0 V; V_{RT} = -0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

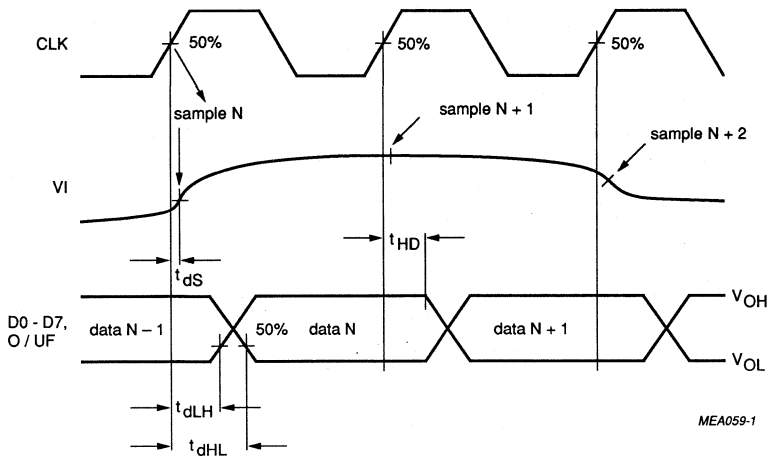


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

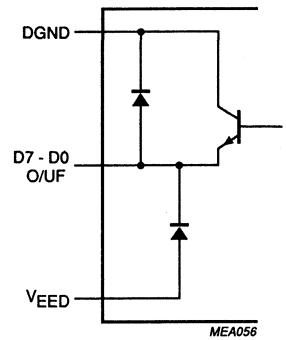


Fig.4 ECL data outputs

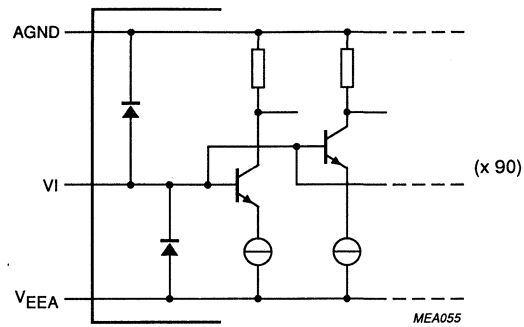


Fig.5 Analog input

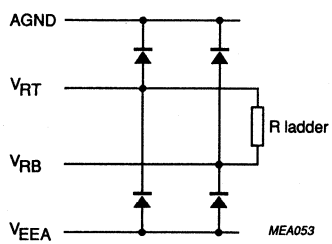


Fig.6 V_{RT} and V_{RB} inputs

APPLICATION INFORMATION

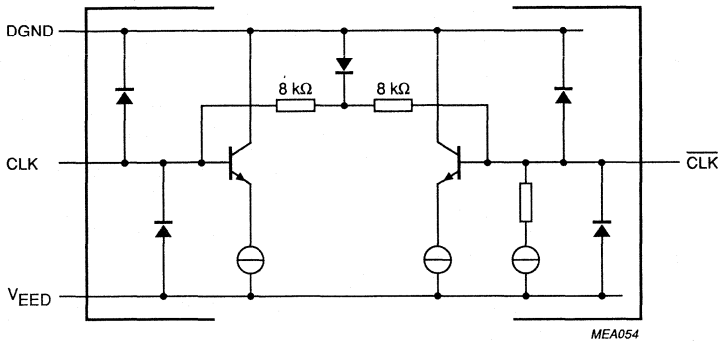


Fig.7 CLK and $\overline{CLK}$ input

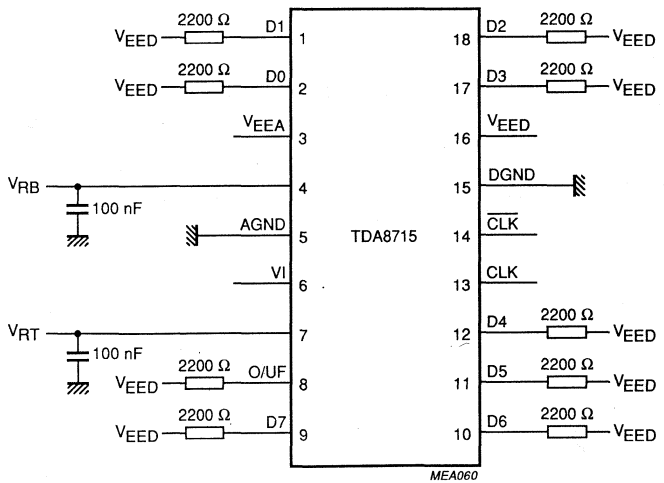


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.0$ V; $V_{RT} = -0.6$ V.

VIDEO PROCESSOR AND INPUT SELECTOR

GENERAL DESCRIPTION

The TDA9045 is a monolithic integrated circuit for video signal processing and input selection.

FEATURES

- Selection stage for three different inputs
- 4 dB amplifier
- Constant output signal amplifier controlled by synchronizing level and peak white level
- Clamping stage for a constant black level
- Circuit for stopping clamping pulses during the sync pulses
- Emitter follower output stage

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	–	12	–	V
Supply current		I_P	–	60	–	mA
Pre-amplifier						
Composite colour video input signals (peak-to-peak value)		$V_{2,3,4-11(p-p)}$	–	–	2	V
AGC amplifier						
Composite video signal (peak-to-peak value)	±6 dB	$V_{12-11(p-p)}$	–	0,4	–	V
Sync level detector						
Threshold voltage for sync level control		V_{9-11}	–	1,8	–	V
Selection						
active input pin 2		V_{1-11}	–	5	–	V
		V_{15-11}	–	5	–	V
active input pin 3		V_{1-11}	0	–	–	V
		V_{15-11}	–	5	–	V
active input pin 4		V_{1-11}	0	–	–	V
		V_{15-11}	0	–	–	V
Not allowed condition		V_{1-11}	–	5	–	V
		V_{15-11}	–	0	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

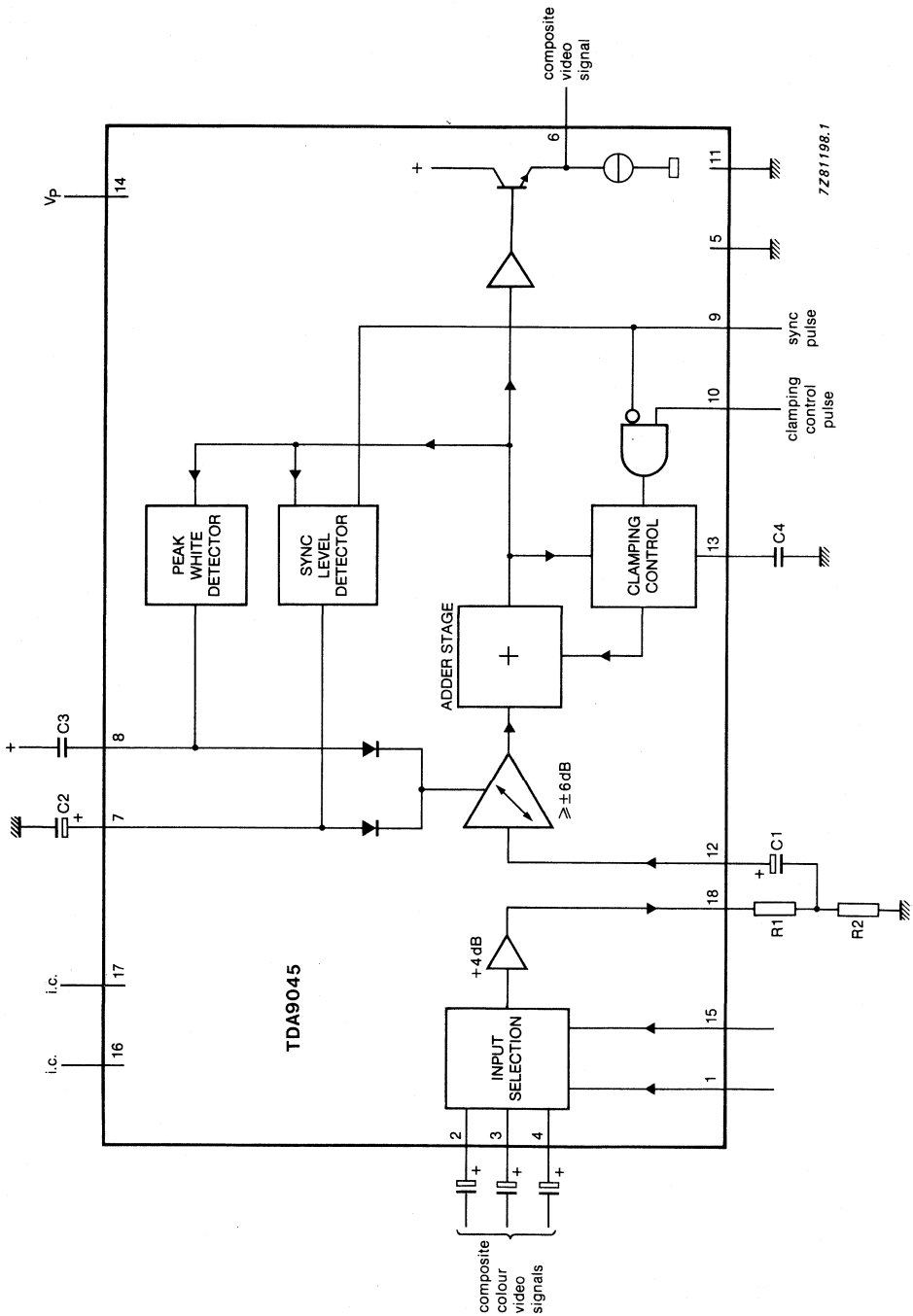


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	0	13,2	V
Voltage on pins 9, 10, 12 to pin 11 (GND)		$V_{n\text{-}11}$	0	V_P	V
Voltage readings		$V_{2, 3, 4\text{-}11}$	0	0,8 V_P	V
		$V_{7, 8\text{-}11}$	0,7 V_P	V_P	V
		$V_{13\text{-}11}$	0,25 V_P	V_P	V
		$V_{1, 15\text{-}11}$	0	5,5	V
Current readings		I_6	–	10	mA
		I_{18}	–	20	mA
Total power dissipation		P_{tot}	–	1	W
Storage temperature range		T_{stg}	–25	+150	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{14\text{-}11} = 12$ V; trigger pulse width pin 10 = 4 μs; $T_{amb} = 25$ °C; measured in test circuit Fig. 2 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	9,6	–	13,2	V
Supply current		I_P	–	60	–	mA
Input channel selector						
Input resistance		$R_{1\text{-}11}$	–	7,5	–	kΩ
Selector switching voltage						
select input pin 4		$V_{1\text{-}11}$	0	–	1	V
		$V_{15\text{-}11}$	0	–	1	V
select input pin 3		$V_{1\text{-}11}$	0	–	1	V
		$V_{15\text{-}11}$	2,5	5	5,5	V
select input pin 2		$V_{1\text{-}11}$	2,5	5	5,5	V
		$V_{15\text{-}11}$	2,5	5	5,5	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Pre-amplifier						
Composite colour video input signals (peak-to-peak value)		$V_{2,3,4-11(p-p)}$	–	1	2,0	V
Input resistance		$R_{2,3,4-11}$	–	10	–	kΩ
Input capacity		$C_{2,3,4-11}$	–	10	–	pF
Amplification		$A_{18-2,3,4}$	–	4	–	dB
DC output voltage		V_{18-11}	–	5,8	6,4	V
Frequency response	0 to 7 MHz		–	–	±2	dB
Signal suppression at output	pin 18 with no input		50	–	–	dB
AGC amplifier						
Input voltage composite video signal (peak-to-peak value)	± 6 dB	$V_{2,3,4-11(p-p)}$	–	0,4	–	V
Input resistance		R_{12-11}	–	10	–	kΩ
Input capacity		C_{12-11}	–	10	–	pF
Frequency response	0 to 7 MHz		–	–	±2	dB
Peak white and sync pulse level detectors						
capacitor current charging current		$-I_8$	–	15	–	mA
discharging current		I_8	–	0,8	–	μA
charging current		$-I_7$	–	0,3	–	mA
discharging current		I_7	–	0,3	–	mA
Threshold voltage for sync level controls		V_{9-11}	1	1,8	2,4	V
Input current		$-I_{9-11}$	–	–	50	μA
Clamping control triggering and sync pulse regeneration						
Threshold voltage for clamping control ON	V_{9-11} = 0 V	V_{10-11}	1	1,8	2,4	V
Input current		$-I_{10-11}$	–	–	50	μA
Charging current		$-I_{13}$	–	0,3	–	mA
Discharging current		I_{13}	–	0,3	–	mA
Black level voltage		V_{6-11}	5,2	5,6	6	V
Controlled output signal (peak-to-peak value)		$V_{6-11(p-p)}$	3,7	3,9	4,1	V

DEVELOPMENT DATA

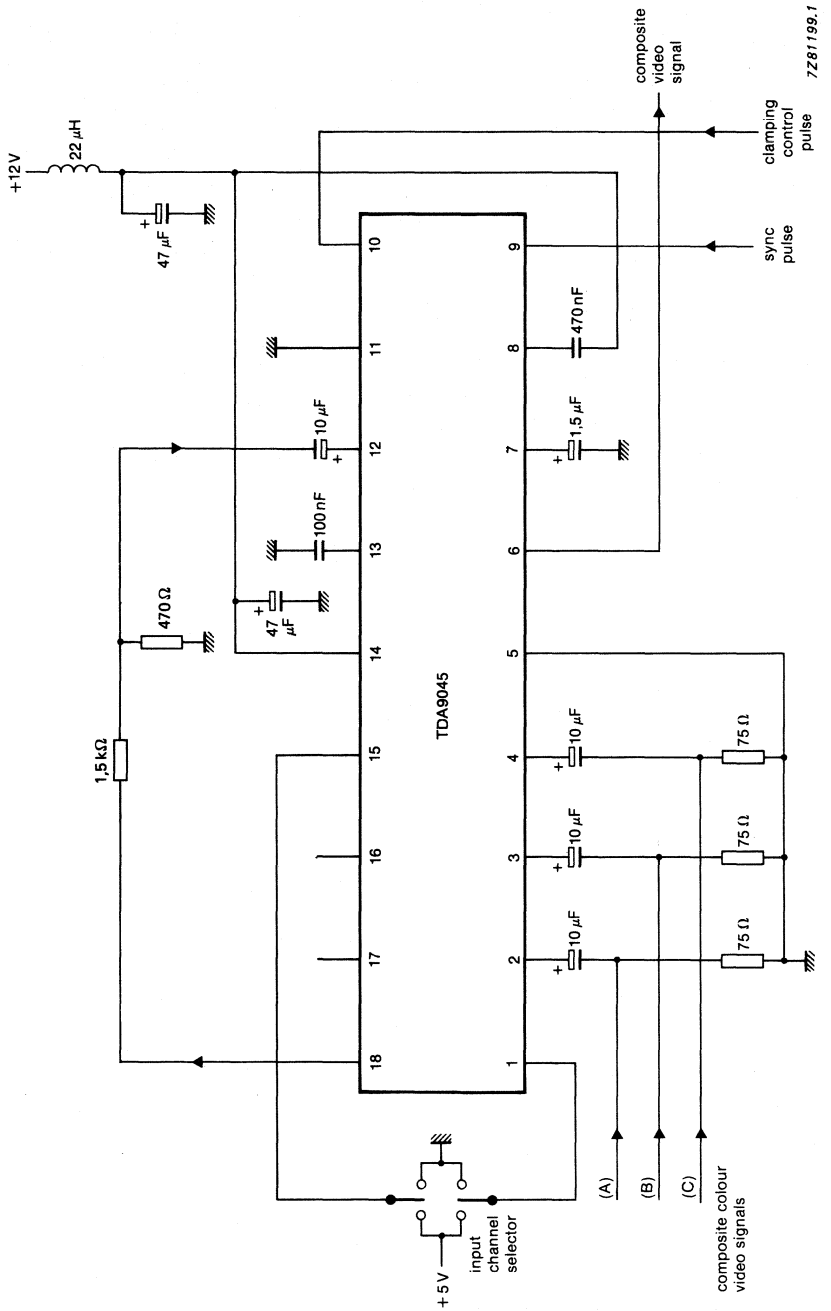


Fig. 2 Application diagram; also used as test circuit.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA9080 is an integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference −(R−Y) and −(B−Y), and a 2-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G−Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 2-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0.45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1.33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1.05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1.0	–	V
Two-level sandcastle pulse		V_{10-24}	–	2.5	–	V
			–	4.5	–	V
Control voltage ranges						
brightness		V_{20-24}	1.0	–	3.0	V
contrast		V_{19-24}	2.0	–	4.3	V
saturation		V_{16-24}	2.0	–	4.3	V

DEVELOPMENT DATA

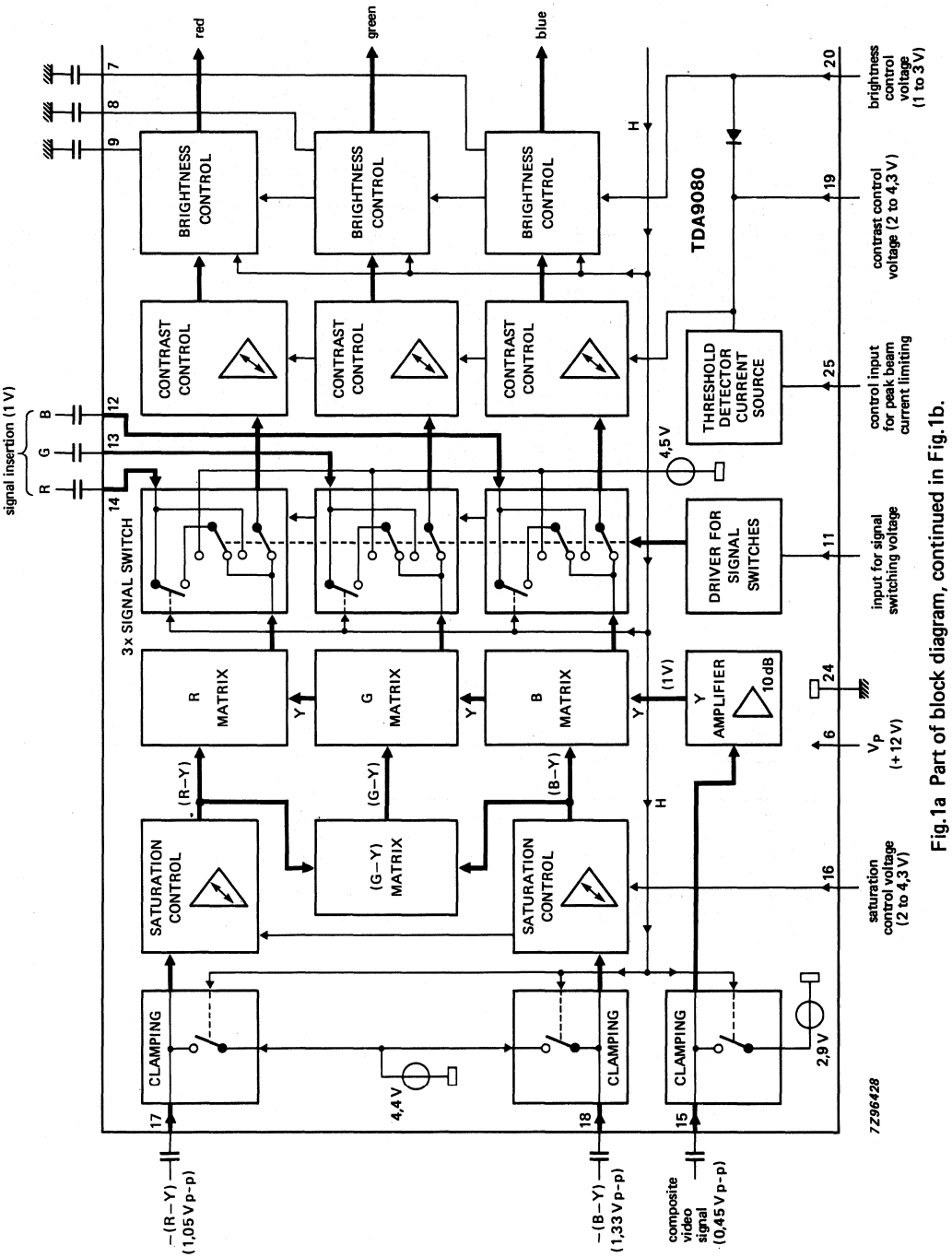


Fig.1a Part of block diagram, continued in Fig.1b.

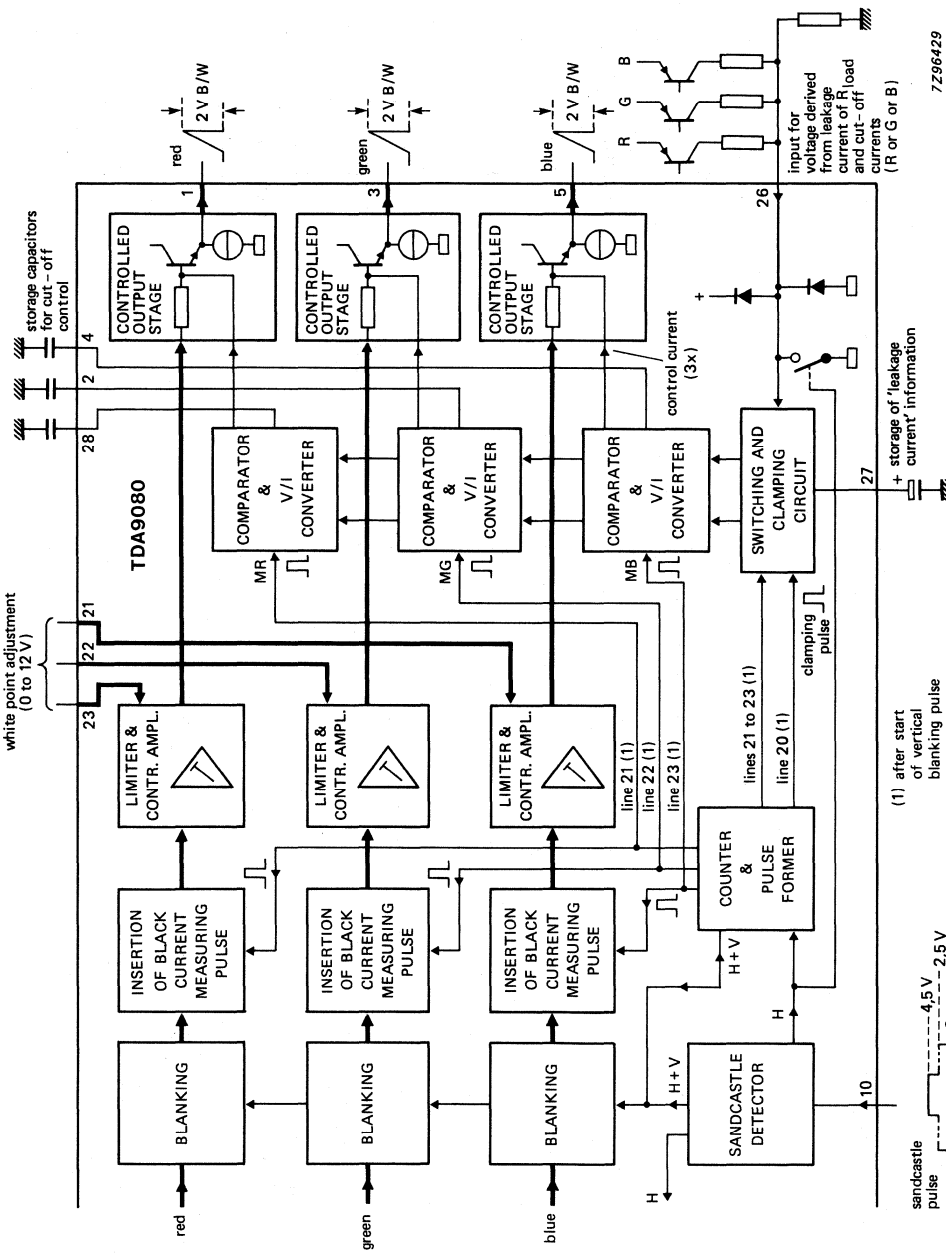


Fig.1b Part of block diagram, continued from Fig.1a.

DEVELOPMENT DATA

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13.2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0.5	3.0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	$0.5V_P$	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1.7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12.0$ V; $V_{12,13,14(p-p)} = 1.0$ V; $V_{15-24(p-p)} = 0.45$ V; $V_{17-24(p-p)} = 1.05$ V; $V_{18-24(p-p)} = 1.33$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10.8	12.0	13.2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1.05	1.48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1.33	1.88	V
Input current during scanning		$I_{17,18}$	–	–	1.0	μA
Input resistance		$R_{17,18-24}$	1.0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3.8	4.4	4.8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4.0	4.2	4.4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2.9	3.1	3.3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1.9	2.1	2.3	V
Minimum saturation	$V_{16} = 1.8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* $<$ 115 mA after warm-up

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0.85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2.5	2.9	3.3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0.4	V
Level for insertion-on		V_{11}	0.9	–	3.0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1.0	1.4	V
Input current during scanning		$I_{12,13,14}$	–	–	1.0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4.0	4.5	5.0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4.0	4.2	4.4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3.4	3.6	3.8	V
Control voltage for −10 dB below max.		V_{19}	2.6	2.8	3.0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0.6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5.3	5.5	5.7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4.5 V	I_{19}	10	20	34	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5.5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1.5	2.0	2.5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6.1	6.9	7.7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4.0	4.6	–	V
Internal current source		$I_{1,3,5}$	2.0	3.0	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6.5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0.5	0.64	0.72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 10 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 4 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1.0	1.5	2.0	V
required pulses (H + V)		V_{10}	2.1	2.5	2.9	V
horizontal pulses		V_{10}	3.0	3.5	4.0	V
required pulses (H)		V_{10}	4.1	–	5.0	V
no keying		V_{10}	–	–	1.0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0.4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

   When $V_{11\text{-}24} > 0.9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5.5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:

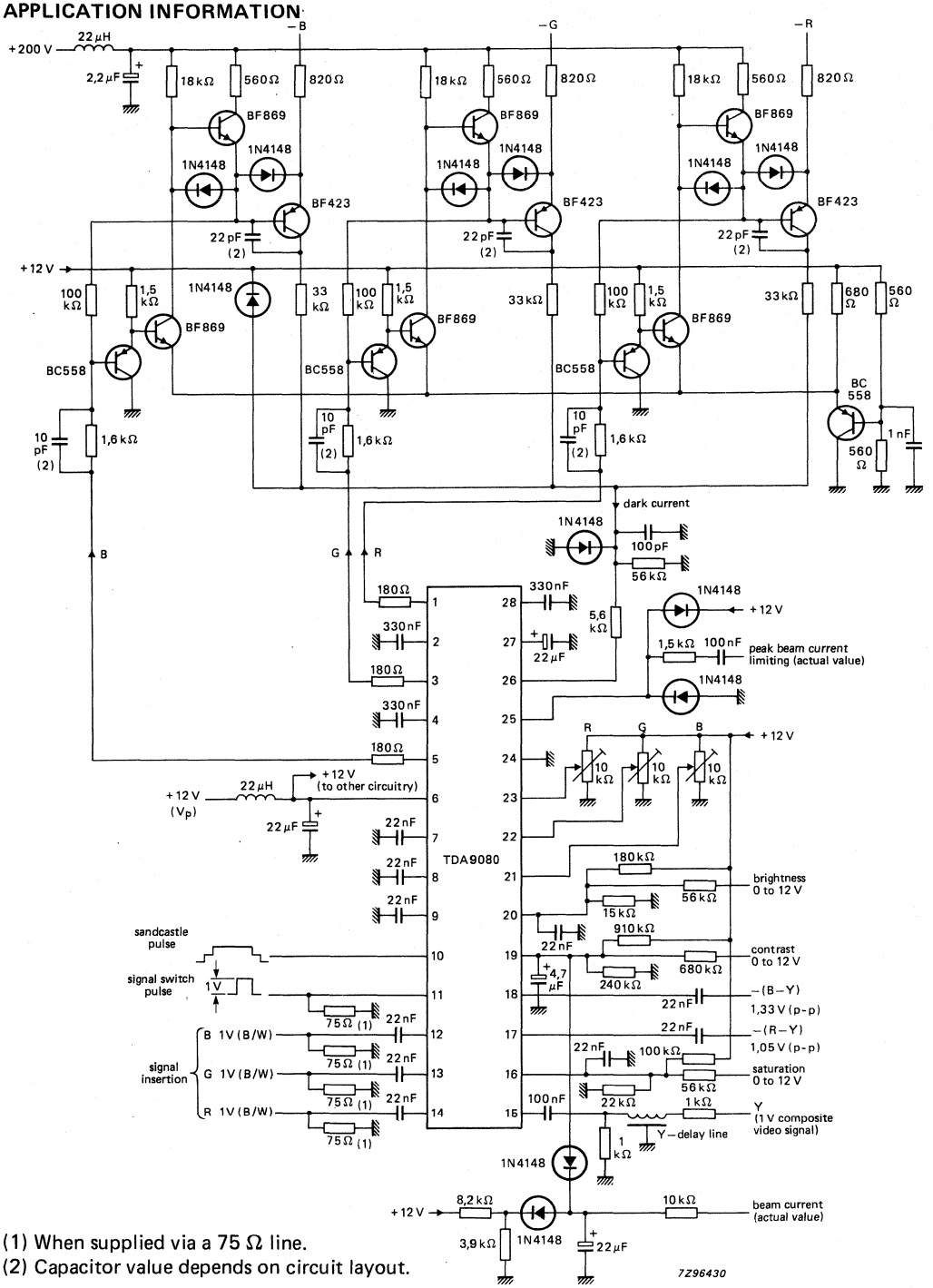
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.

   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.

   The internal blanking continues until the end of the last measured line.

   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with two internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (–25%).

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig.2 Typical application circuit diagram using the TDA9080.

DEVELOPMENT DATA

Philips Components

Data sheet	
status	Preliminary specification
date of issue	March 91
Replaces the issue of September 1990.	

TDA9820

Multistandard / dual channel TV FM intercarrier sound demodulator

FEATURES

- Multistandard application for sound standards M, B/G, I, D/K
- Two alignment-free PLL FM demodulators
- Four-input source selector for one of the two FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9820 is a monolithic, integrated, multistandard TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

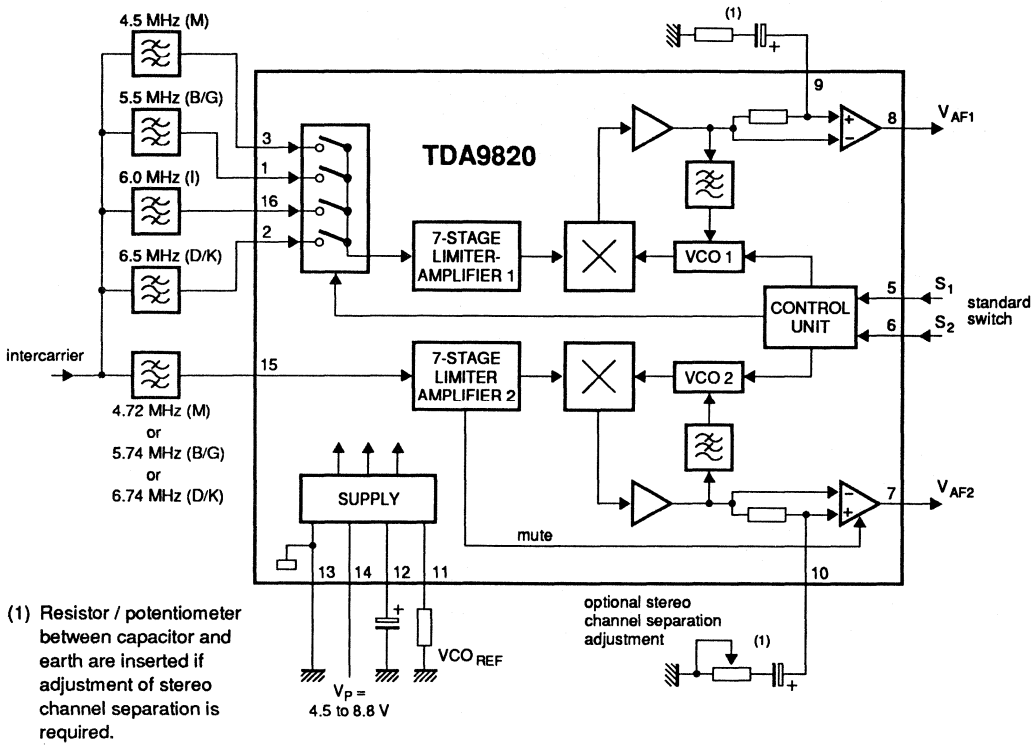
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9820	16	DIL	plastic	SOT38
TDA9820T	16	DIL	plastic	SOT162A

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820



(1) Resistor / potentiometer between capacitor and earth are inserted if adjustment of stereo channel separation is required.

Fig.1 Block diagram.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
$IN_{1(D/K)}$	2	first intercarrier input at 6.5 MHz
$IN_{1(M)}$	3	first intercarrier input at 4.5 MHz
n.c.	4	not connected
S_1	5	standard switch bit 1
S_2	6	standard switch bit 2
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
IN_2	15	second intercarrier input
$IN_{1(I)}$	16	first intercarrier input at 6.0 MHz

PIN CONFIGURATION

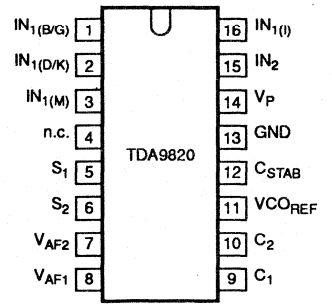


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

Source selector

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.
One of the four filtered sound carriers from pins 1, 2, 3 or 16 is fed to limiter-amplifier 1 via the appropriate electronic switch in the source selector. The electronic switch of the sound carrier is selected by the control unit (see Logic Table).
The second sound carrier of the intercarrier signal is directly fed from pin 15 to limiter-amplifier 2.

FM demodulators

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensures that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. High amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as followes:
a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9
b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

Control unit

The control unit selects the required sound standard according to the voltages on pin 5 and pin 6. The control unit performs the following:
(a) selects the free-running frequencies of VCO1 and VCO2
(b) switches the source selector (the four possible combinations are shown in Table 1).

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

Table 1 Logic Table

STANDARD	S1 (pin 5)	S2 (pin 6)	FREQUENCY VCO1	FREQUENCY VCO2	SOURCE SELECTOR CONNECTION
B/G	1	1	5.5 MHz	5.74 MHz	pin 1
M	1	0	4.5 MHz	4.72 MHz	pin 3
I	0	1	6.0 MHz	OFF	pin 16
D/K	0	0	6.5 MHz	6.74 MHz	pin 2

Note to Table 1

In columns S1 and S2:
0 = LOW
1 = HIGH.

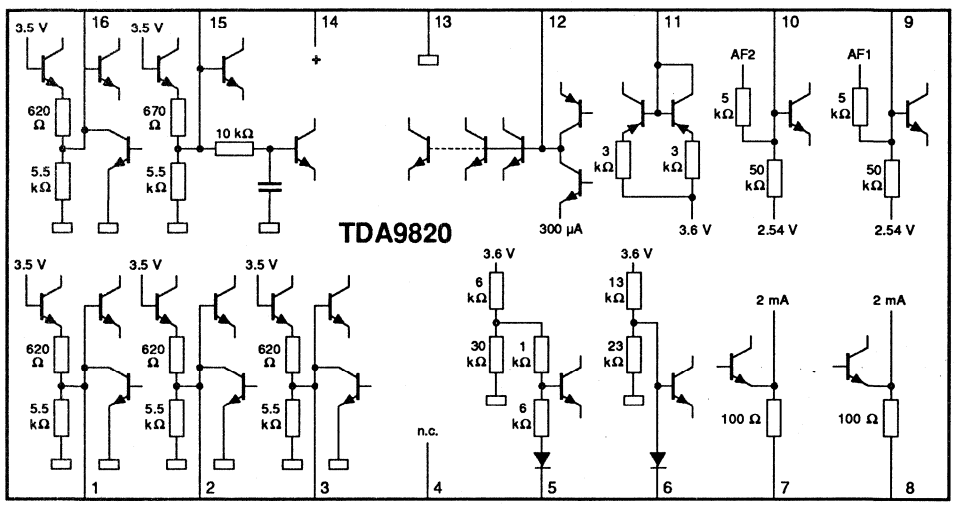


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	–0.5	9.0	V
V_i	input signal (pins 1, 2, 3, 15 and 16)	–0.5	5.0	V
V_{adj}	adjustment voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1,2,3,16/15(rms)}$ = 10 mV; T_{amb} = 25 °C; measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Source selector and limiter-amplifier 1 (pins 1, 2, 3 and 16)						
V_I	DC input voltage	input activated	–	2.55	–	V
		input not activated	–	–	0.1	V
R_I	input resistance	input activated	480	600	720	Ω
		input not activated	–	–	100	Ω
$V_{i(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB	–	100	250	μV
	allowed input signal (RMS value)		200	–	–	mV
α_i	crosstalk attenuation	not activated input to activated input	–	50	–	dB
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	μV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
R_{15}	input resistance		480	600	720	Ω
δ	hysteresis of level detector		–	12	–	dB
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – – –	4.5 5.5 6.0 6.5	– – – –	MHz MHz MHz MHz
f_{VCO2}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – –	4.72 5.74 6.74	– – –	MHz MHz MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	resistance at pin 11	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output amplifiers AF1 (pin 8) and AF2 (pin 7)						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
$\Delta V_o/\Delta V_o$	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 µs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment (pin 9 and pin 10)	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
THD	distortion (pin 8 and pin7)	with 50 µs de-emphasis	–	0.1	0.3	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 µs de-emphasis; m = 0.3; Δfi = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 µs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
Control unit (see Table 1)						
$V_{5,6}$	voltage for 'low'		0	–	0.8	V
$I_{5,6}$	input current	$0 < V_{5,6} < 0.8$	–	–180	–250	µA
$R_{5,6}$	allowed resistance to ground	$0 < V_{5,6} < 0.8$ ('low')	–	–	3.0	kΩ
V_5	voltage for HIGH (note 2)		2.2	–	V_P	V
V_6	voltage for HIGH (note 2)		1.8	–	V_P	V
$I_{5,6}$	input current	$V_{5,6} = V_P$	–	–	10	µA

Notes to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.
2. An open pin (n.c.) is interpreted as HIGH.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

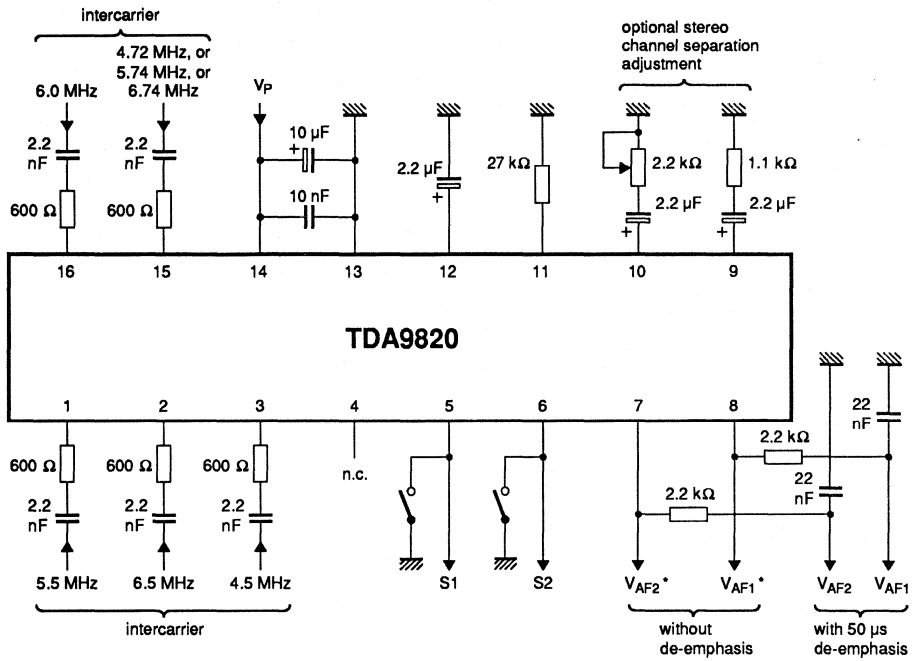


Fig.4 Test circuit.

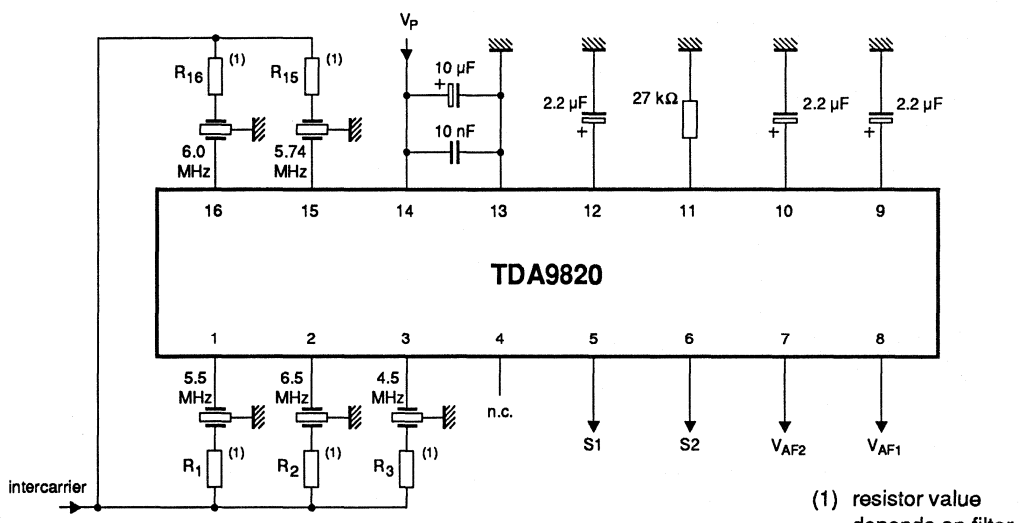


Fig.5 Application circuit.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA9821

Dual channel TV FM intercarrier sound demodulator

FEATURES

- Two alignment-free PLL FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9821 is a monolithic, integrated, TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9821	16	DIL	plastic	SOT38

Dual channel TV FM intercarrier sound demodulator

TDA9821

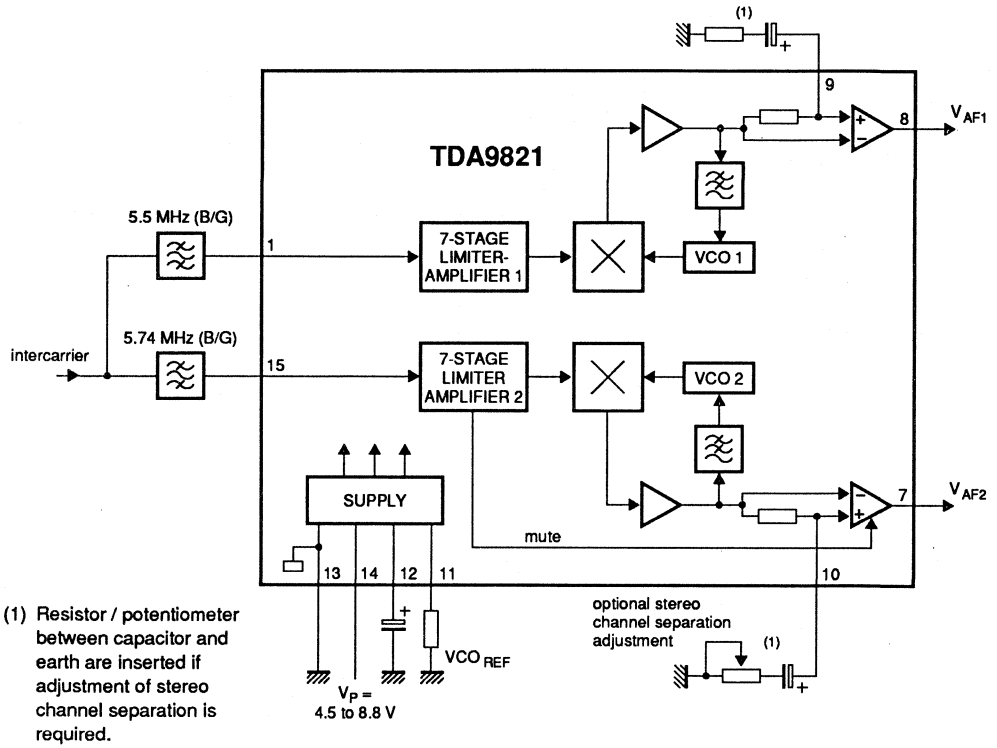


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

FM demodulators

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensure that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. The high amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as follows:

a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9

b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Normally stereo channel separation is adjusted in the stereo decoder for the B/G standard.

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

Dual channel TV FM intercarrier sound demodulator

TDA9821

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
n.c.	2	not connected
n.c.	3	
n.c.	4	
n.c.	5	
n.c.	6	
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
$IN_{2(B/G)}$	15	second intercarrier input
n.c.	16	not connected

PIN CONFIGURATION

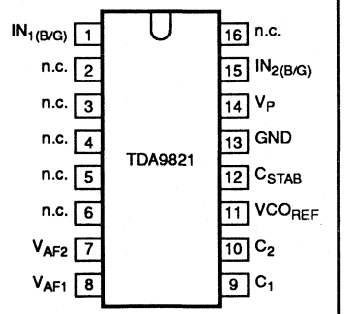


Fig.2 Pin configuration.

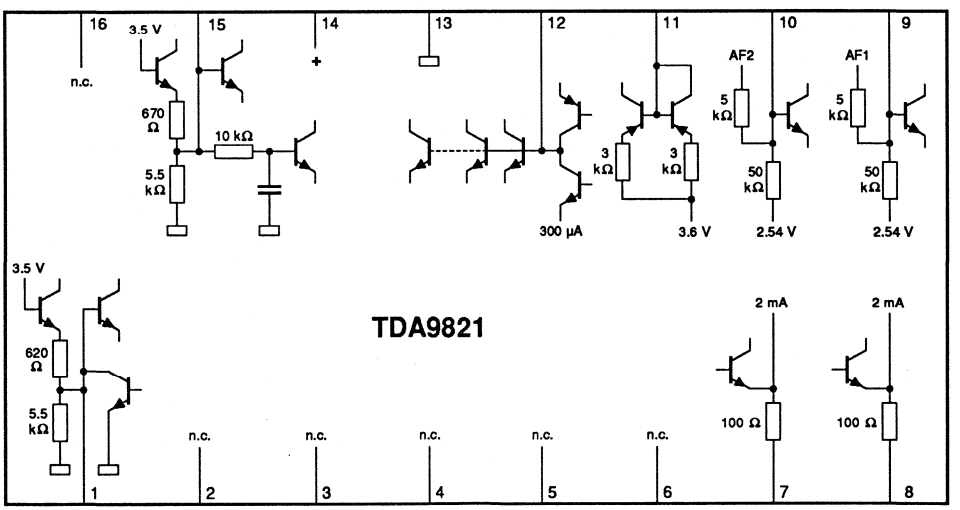


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	–0.5	9.0	V
V_i	input signal (pin 1 and pin 15)	–0.5	5.0	V
V_{adj}	adjusting voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1/15(rms)}$ = 10 mV; T_{amb} = 25 °C;measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Limiter-amplifier 1						
V_1	DC input voltage		–	2.55	–	V
R_1	input resistance		480	600	720	Ω
$V_{1(rms)}$	input signal(RMS value)	(S+N)/N = 40 dB	–	100	250	µV
	allowed input signal (RMS value)		200	–	–	mV
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	µV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
ΔV_{15}	mute hysteresis		–	12	–	dB
R_{15}	input resistance		480	600	720	Ω
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequency	R_{11} = 27 kΩ	–	5.5	–	MHz
f_{VCO2}	free-running frequency	R_{11} = 27 kΩ	–	5.74	–	MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulators VCO1 and VCO2 (continued)						
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	R_{11} = 27 kΩ	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz
Output amplifiers AF1 (pin 8) and AF2 (pin 7) and overall performance						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 μs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment at pin 9	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
	at pin 10		–	1.1	2.2	kΩ
THD	total harmonic distortion at pin 8	with 50 μs de-emphasis	–	0.1	0.3	%
	at pin 7		–	0.25	0.5	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 μs de-emphasis; m = 0.3; Δf_i = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 μs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB

Note to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.

Dual channel TV FM intercarrier sound demodulator

TDA9821

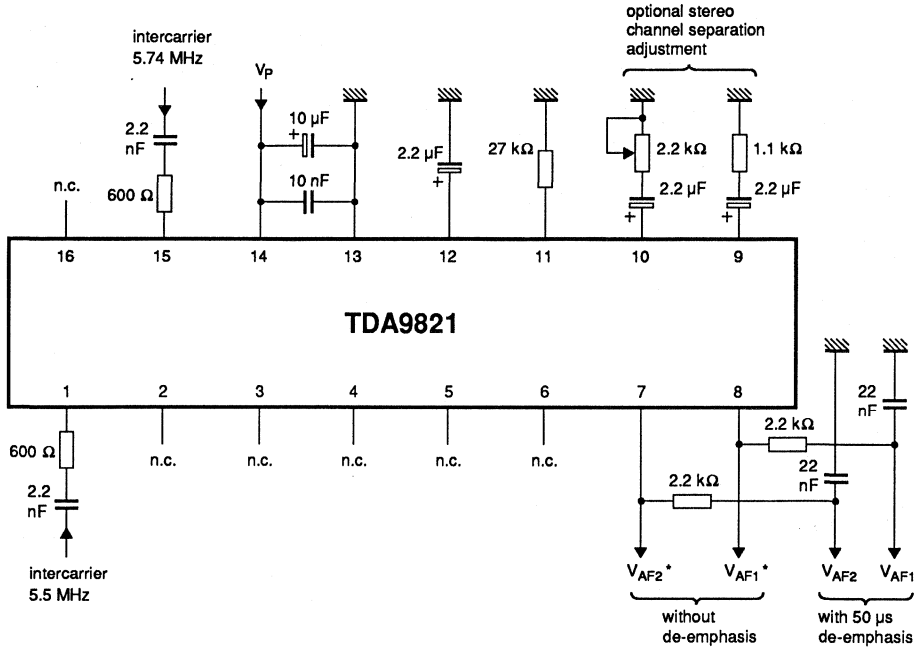


Fig.4 Test circuit.

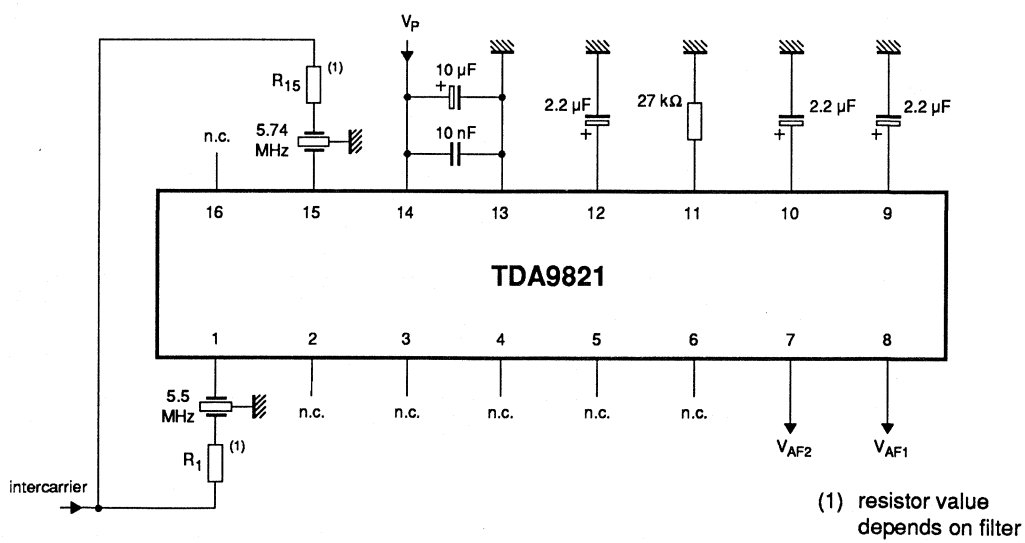


Fig.5 Application circuit.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDE8712D

8-bit video digital-to-analog converter

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation (250 mW typical)
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Test and measurement
- Telecommunications
- Radar/sonar
- Image processing

DESCRIPTION

The TDE8712D is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for professional video and other applications. The operating temperature range is -55 °C to +125 °C. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8712D	16	CERDIP	ceramic	SOT74

8-bit video digital-to-analog converter TDE8712D

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
V_{OUT} – $\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		50	-	-	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

8-bit video digital-to-analog converter TDE8712D

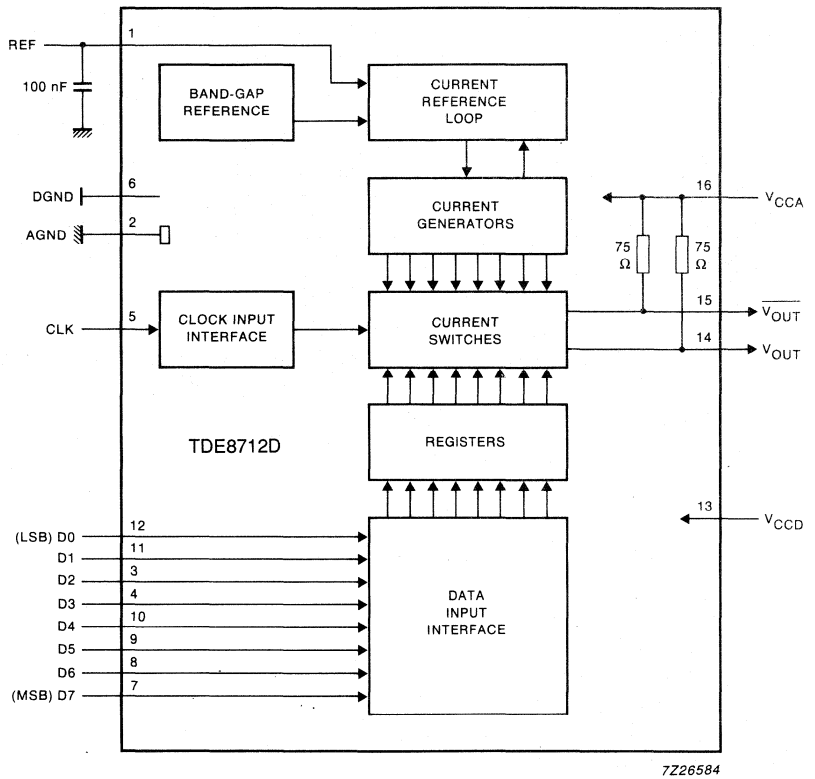


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDE8712D

PIN CONFIGURATION

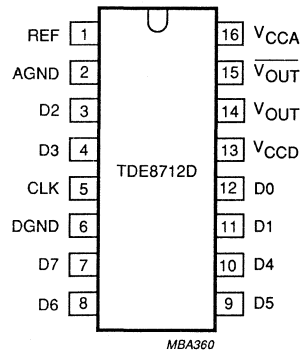


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	−0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+ 0.5	V
AGND − DGND	ground voltage differential	−0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{OUT}	total output current range (pin 14)	−5	+ 26	mA
$\overline{I_{OUT}}$	total output current range (pin 15)	−5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−55	+125	°C
T_j	junction temperature	-	+175	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT74	112	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.75$ V to 5.25 V; $V_{CCD} = V_{13} - V_6 = 4.75$ V to 5.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = -55$ °C to +125 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	0.1	V
Inputs DIGITAL INPUTS (D7 - D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		50	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak- to-peak value)	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
		$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω
Transfer function ($f_{CLK} = 50$ MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (fCLK = 50 MHz; notes 4 and 5; see Figs 3,4 and 5)						
$t_{SU;DAT}$	data set-up time		–0.3	-	-	ns
$t_{HD;DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; $f_{CLK} = 50$ MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).

5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\ DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.

6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

DAC OUTPUT VOLTAGES					
CODE	BINARY INPUT DATA (D7 - D0)	Z_L = 10 kΩ	Z_L = 75 Ω		
		$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)
0	000 000 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	. . . . .	.	.	.	.
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	. . . . .	.	.	.	.
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

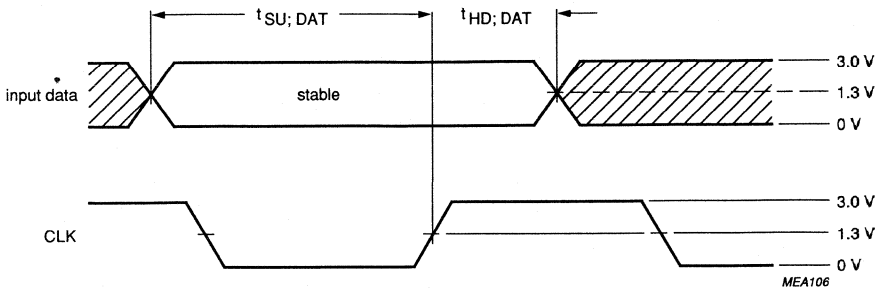


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

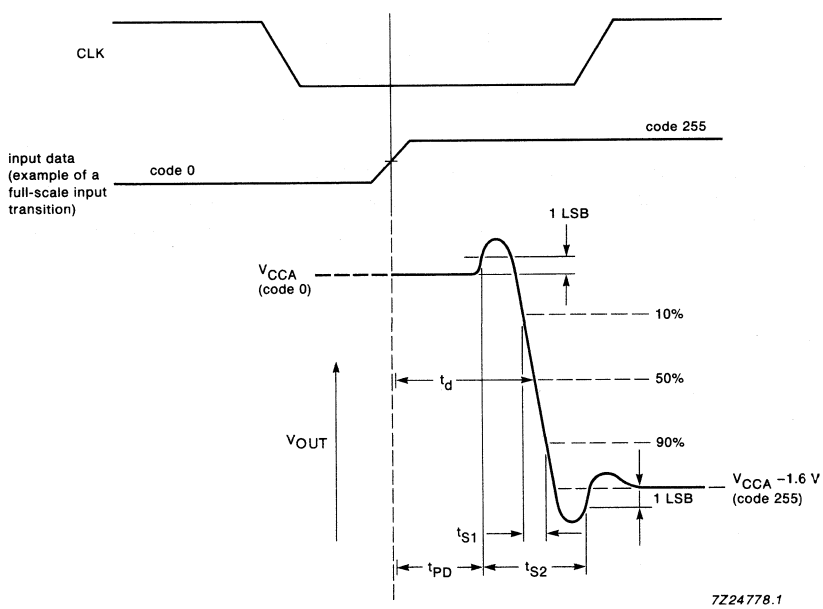


Fig.4 Switching characteristics.

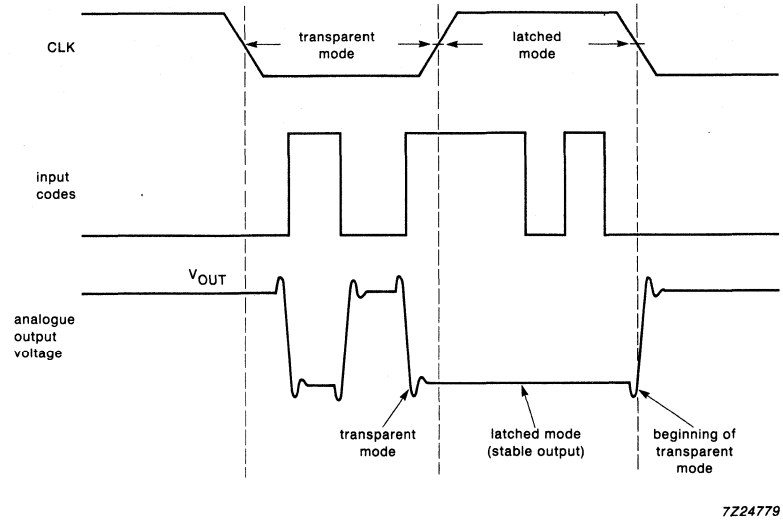


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

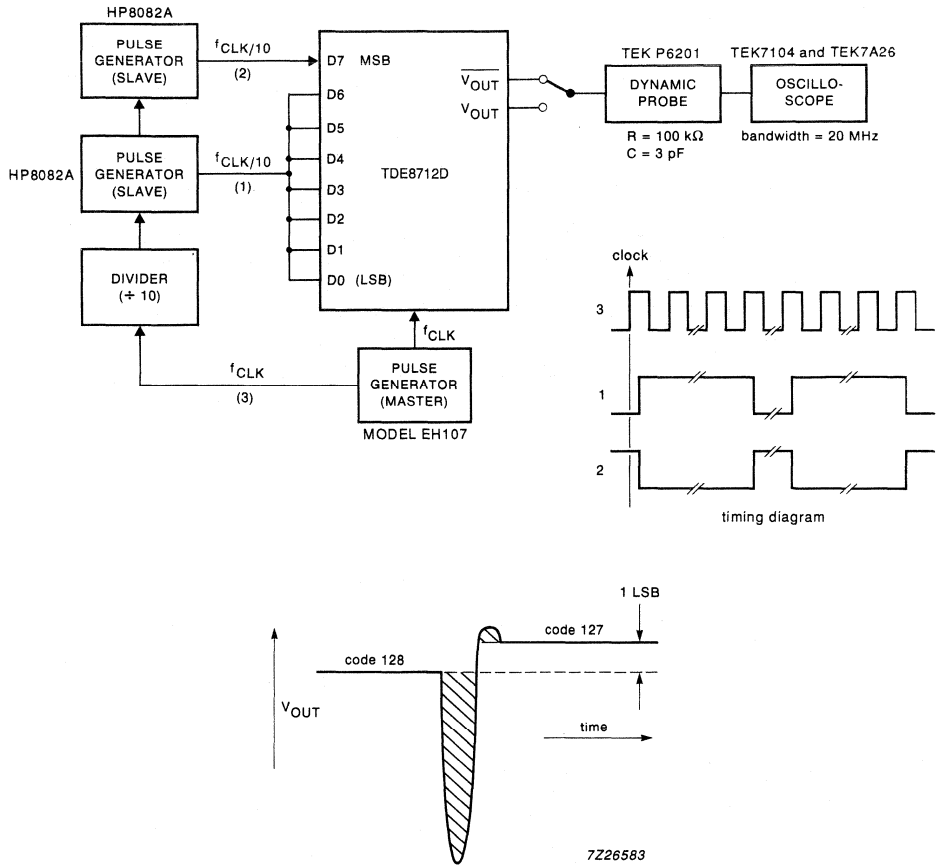


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

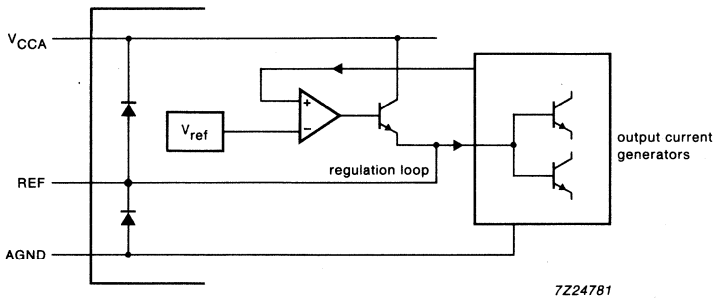


Fig.7 Reference voltage generator decoupling.

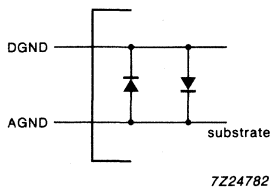


Fig.8 AGND and DGND.

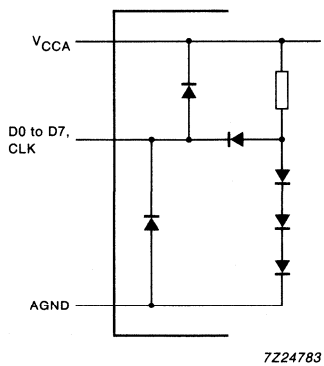


Fig.9 D7 to D0 and CLK.

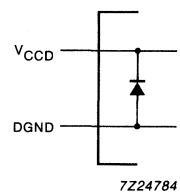


Fig.10 Digital supply.

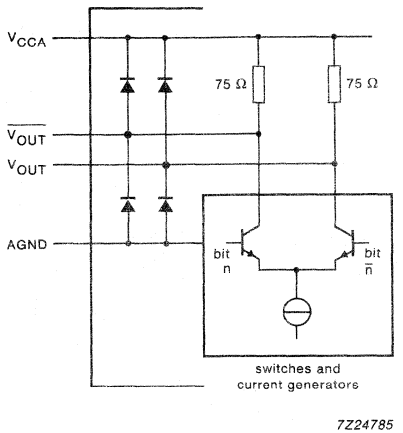


Fig.11 Analog outputs.

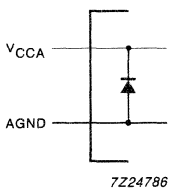


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

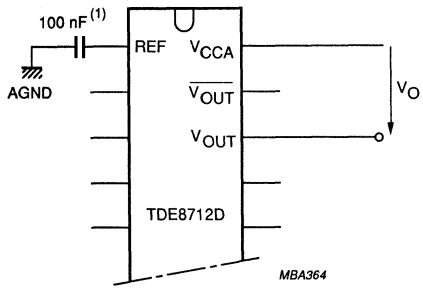


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

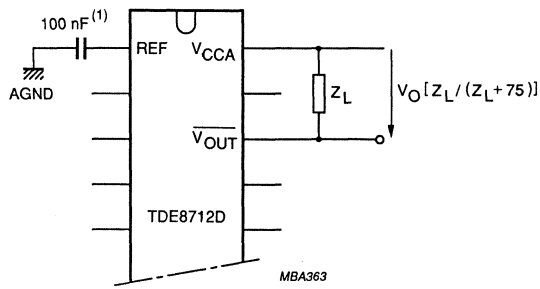


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

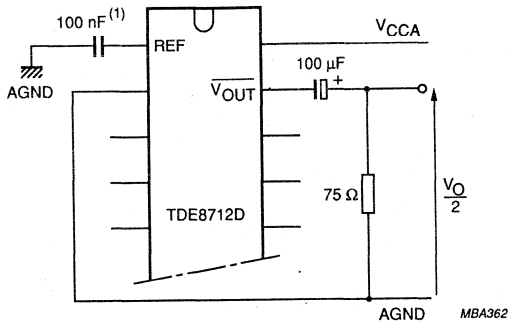


Fig.15 Analog output with AGND as reference.

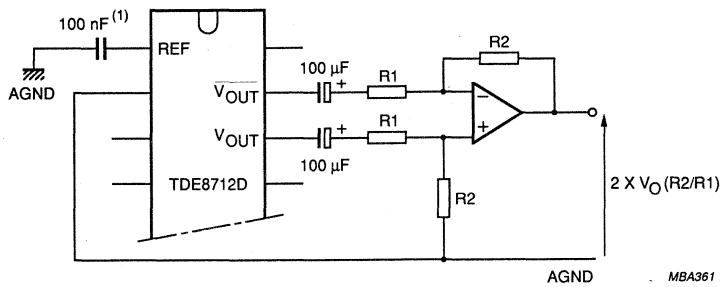


Fig.16 Differential mode (improved supply voltage ripple rejection).

Notes to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDE8715D

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 50 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging

DESCRIPTION

The TDE8715D is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. The operating temperature range is 55 °C up to 125 °C It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10 KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8715D	18	DIL	ceramic (cerdip)	SOT 133BH3

8-bit high-speed analog-to-digital converter TDE8715D

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.95	–5.2	–5.45	V
V_{EED}	digital supply voltage		–4.95	–5.2	–5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	± 0.4	± 0.75	LSB
DLE	DC differential linearity error		-	± 0.25	± 0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		–55	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

8-bit high-speed analog-to-digital converter TDE8715D

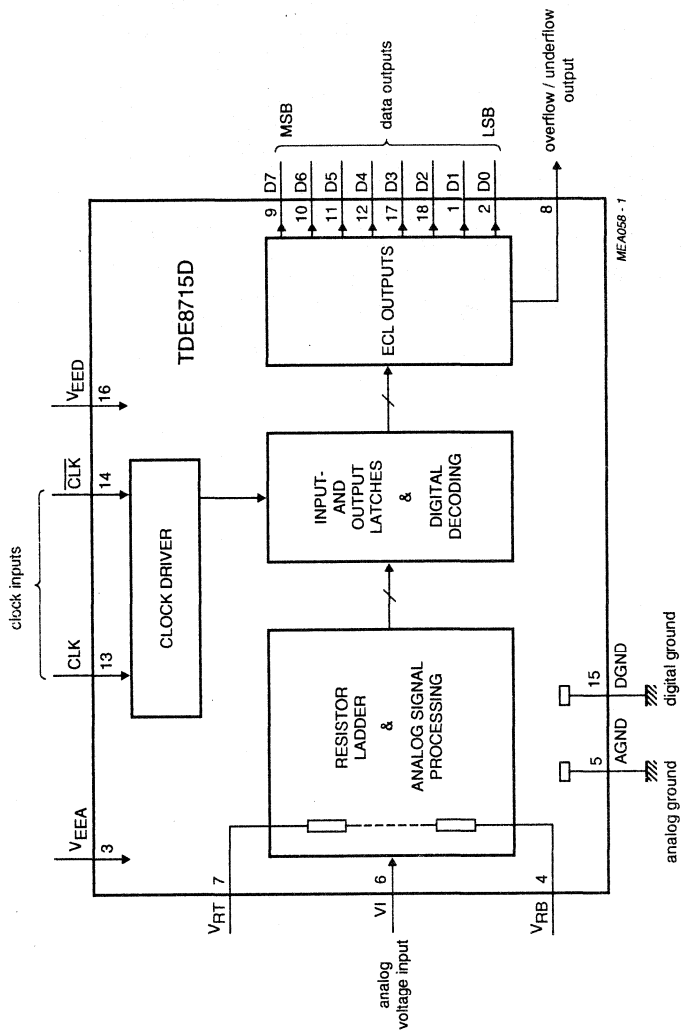


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDE8715D

PIN CONFIGURATION

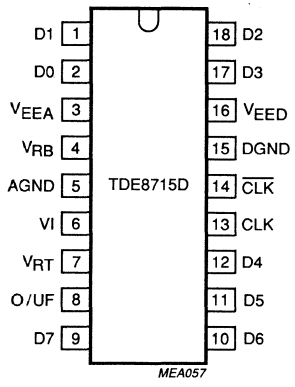


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (−5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (−5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		-55	+125	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT133BH3	+75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.95$ V to -5.45 V; $V_{EED} = V_{16} - V_{15} = -4.95$ V to -5.45 V; AGND and DGND shorted together; $T_{amb} = -55$ °C to $+125$ °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		−4.95	−5.2	−5.45	V
V_{EED}	digital supply voltage		−4.95	−5.2	−5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference V_{EEA} - V_{EED}		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		−3.4	−3.1	−2.8	V
V_{RT}	reference voltage HIGH		−1.0	−0.6	−0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.4	2.5	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	−0.3	-	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	V_{CLK} = −1.77 V	-	−240	-	μA
I_{IH}	input current HIGH	V_{CLK} = −0.88 V	-	−14	-	μA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}}$ = −1.77 V	-	−140	-	μA
I_{IH}	input current HIGH	$V_{\overline{CLK}}$ = −0.88 V	-	75	-	μA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
VI (analog input with V_{RB} = −3.1 V and V_{RT} = −0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	μA
I_{IH}	input current HIGH	data output FF	-	120	-	μA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	−1.9	−1.77	−1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−60	-	dB
F_{odd}	odd harmonics (full-scale)	f_i = 4.43 MHz	-	−50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±0.5	LSB
AILE	AC integral linearity error	note 4	-	±0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20 MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50 MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50 MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.1 V; V_{RT} = –0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

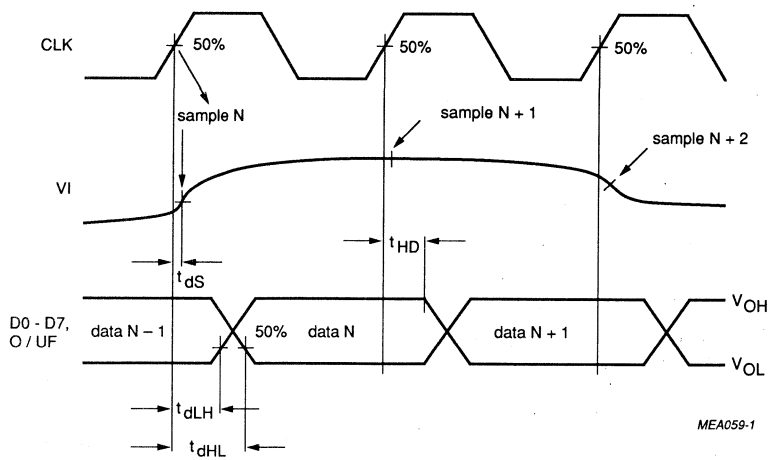


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

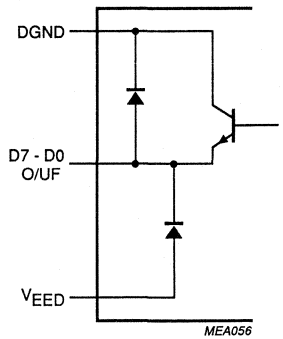


Fig.4 ECL data outputs

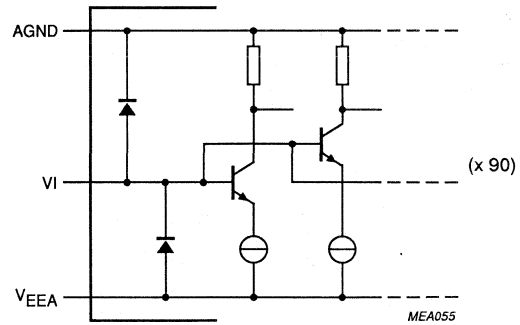


Fig.5 Analog input

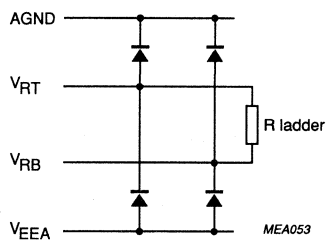


Fig.6 V_{RT} and V_{RB} inputs

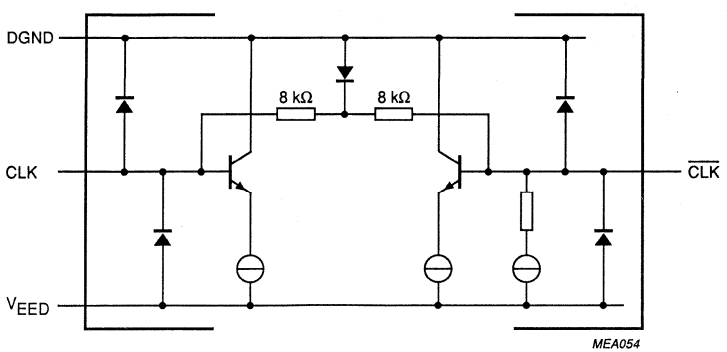


Fig.7 CLK and $\overline{CLK}$ input

8-bit high-speed analog-to-digital converter TDE8715D

APPLICATION INFORMATION

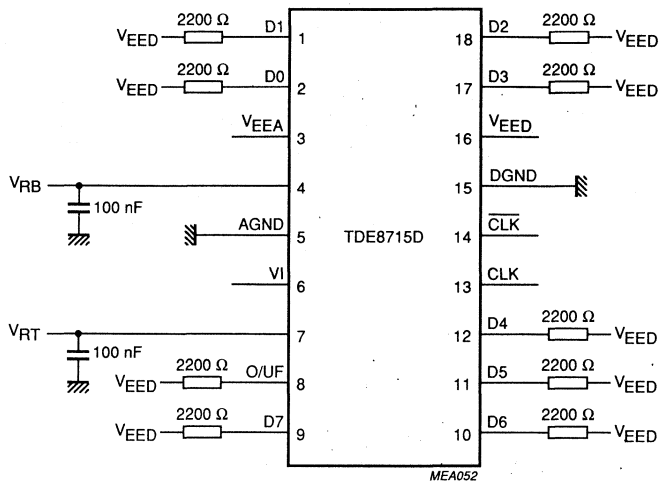


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom. 14	V
Supply current	I_{CC}	max. 13	mA
Output pulse repetition frequency range	f_o	1 Hz to 100	kHz
Output current LOW	I_{OL}	max. 1	A
Operating ambient temperature range	T_{amb}	−25 to +125	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

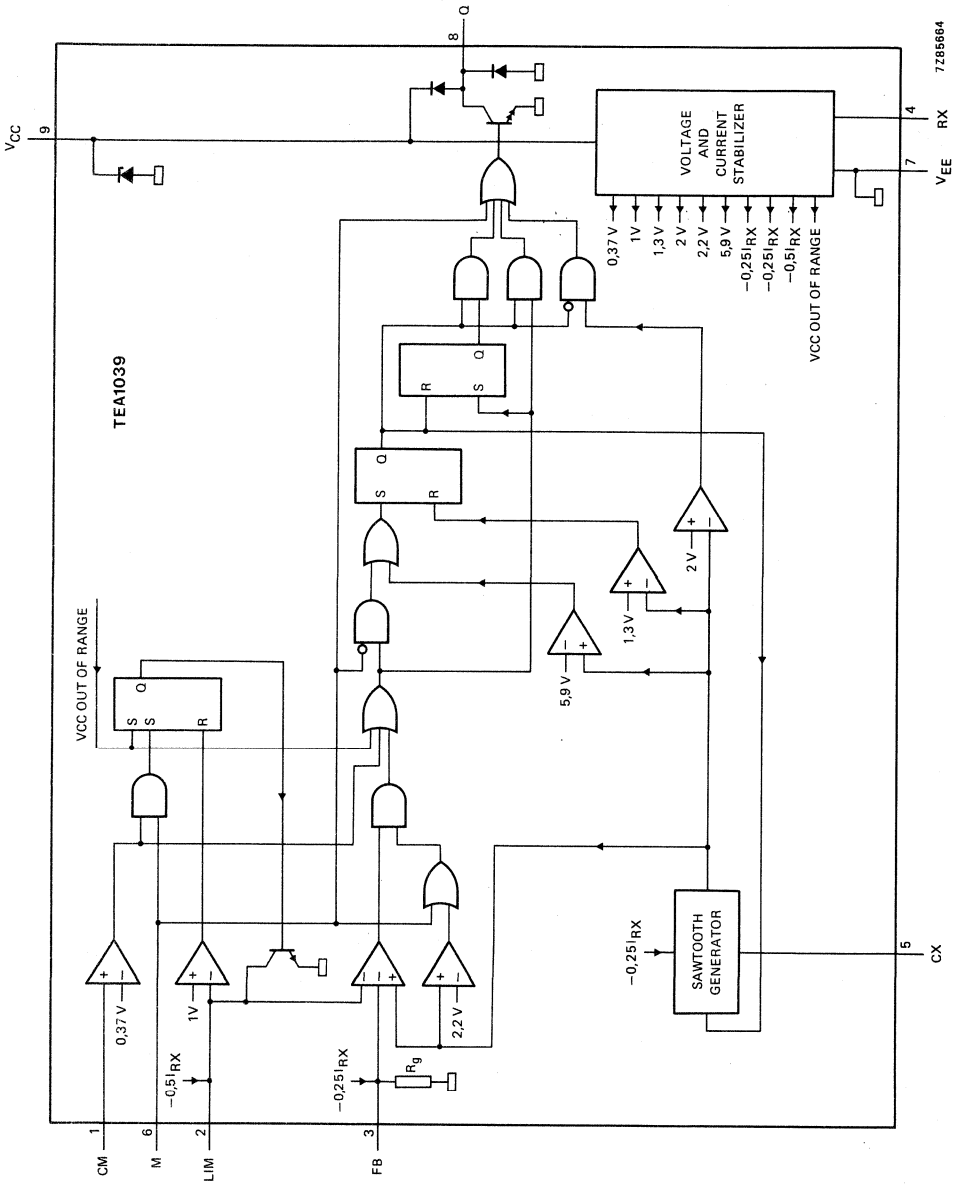


Fig. 1 Block diagram.

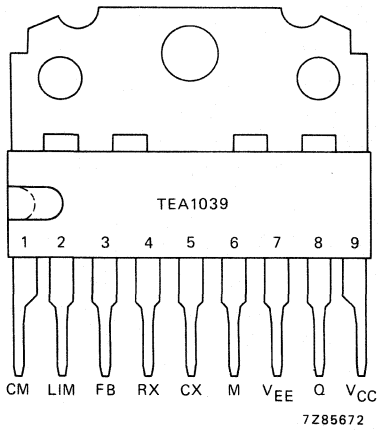


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	V_{8-7}	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

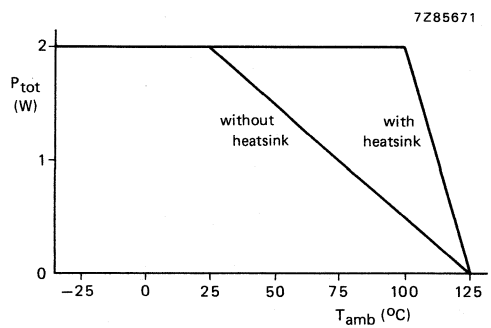


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

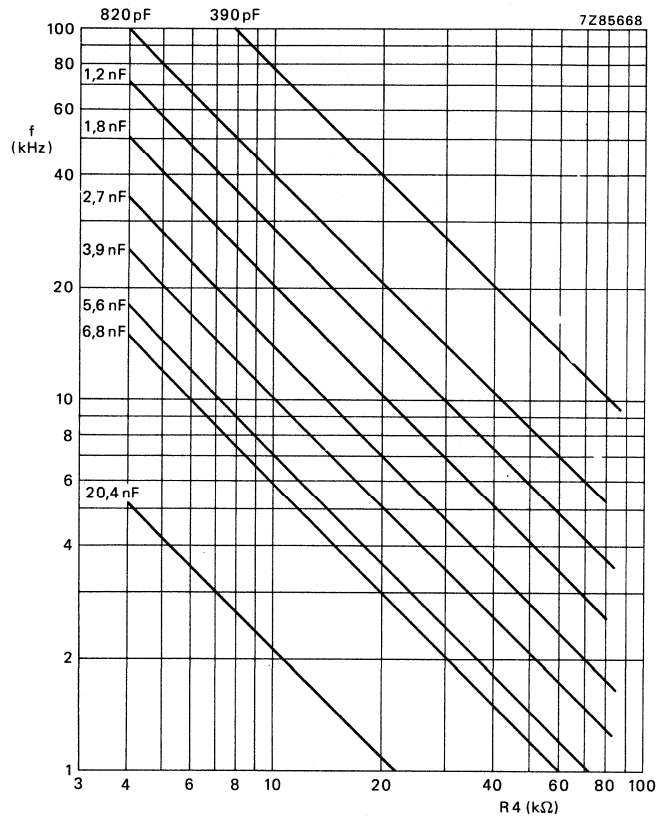


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

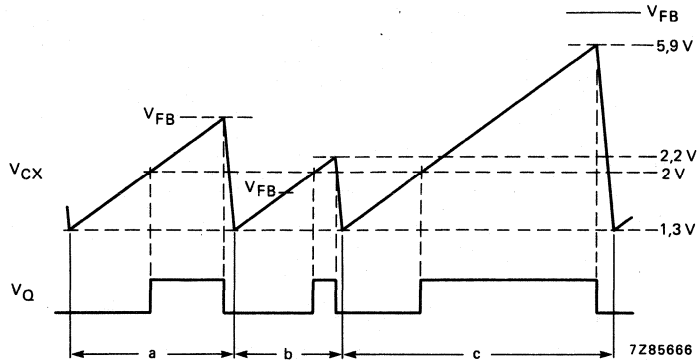


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

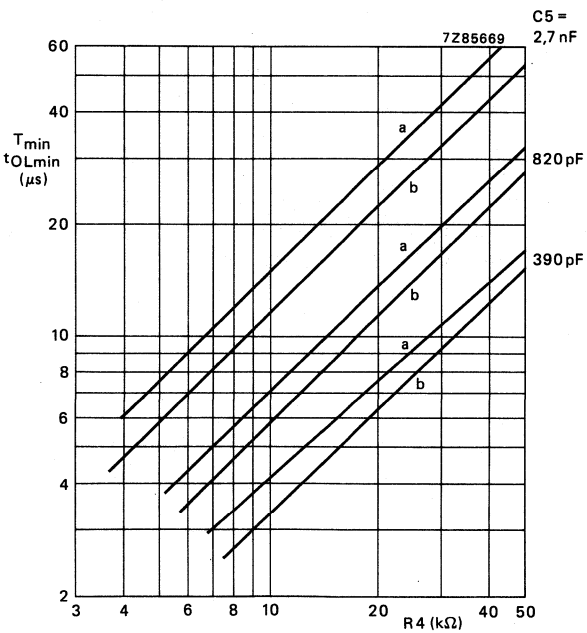


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

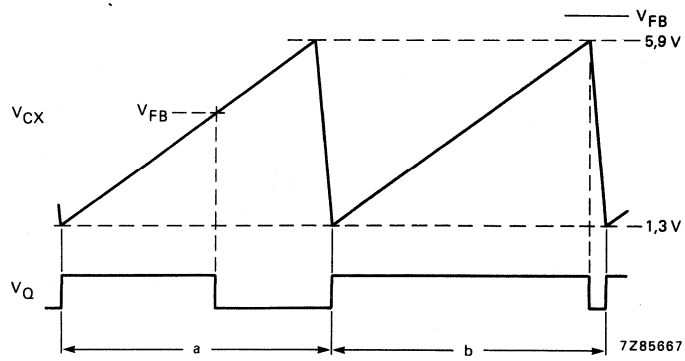


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

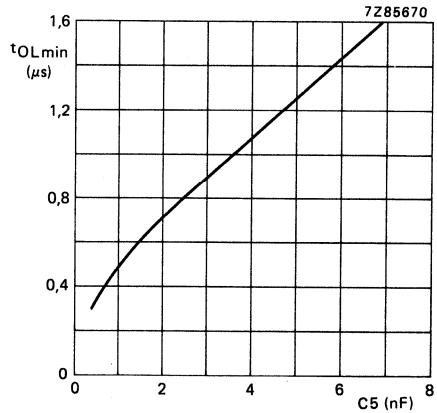


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

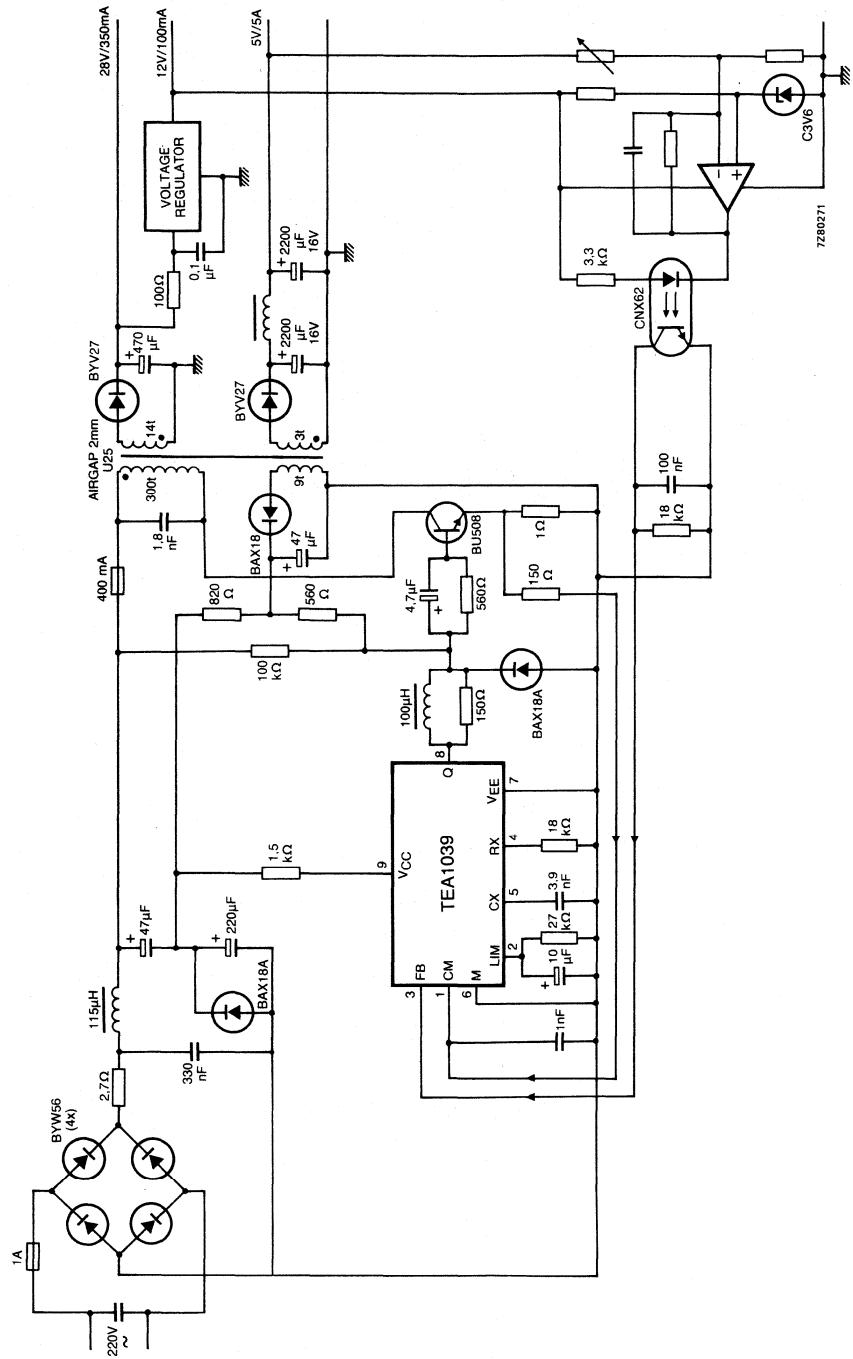


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

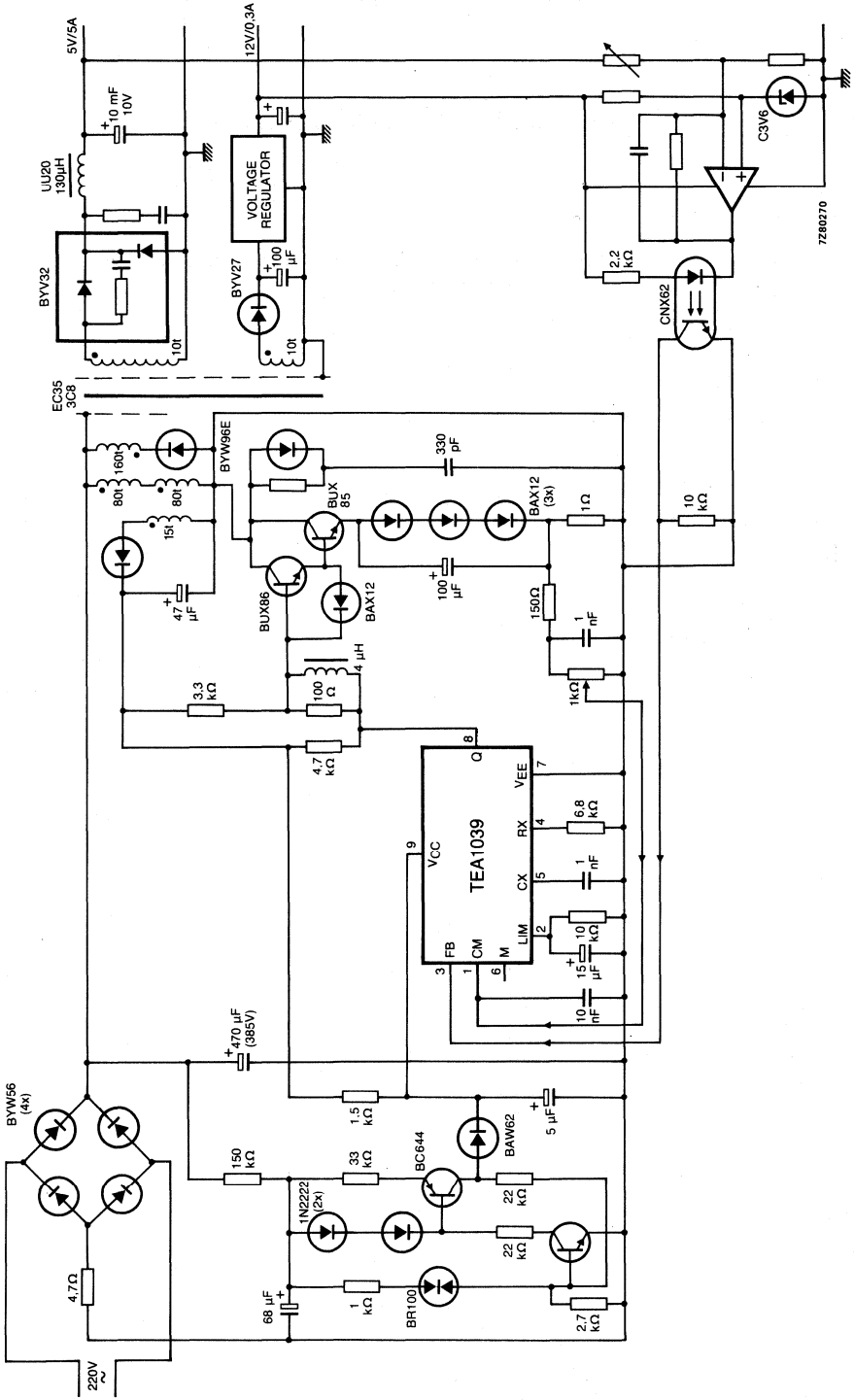


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

PAL/NTSC COLOUR ENCODER

GENERAL DESCRIPTION

The TEA2000 is a monolithic integrated circuit, which encodes colour information and provides composite video output for driving a VHF or UHF modulator.

Features

- European PAL and American NTSC/M standard selectable
- Internal generation of burst timing and PAL-switch-function
- 6 bit binary TTL compatible input provides 64 different colours
- TTL compatible colour blanking input
- TTL compatible sync input

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}9}$	typ.	12 V
Supply current at $V_{11\text{-}9}$ = 12 V	I_{11}	typ.	55 mA
Input voltage pins 1,2,3,4,5,14,16,17,18	V_{IL}	max.	0,8 V
	V_{IH}	min.	2,0 V
Composite video output (sync tip to white)	$V_{6\text{-}9(p\text{-}p)}$	typ.	2,0 V
Operating temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic with internal heat spreader (SOT102).

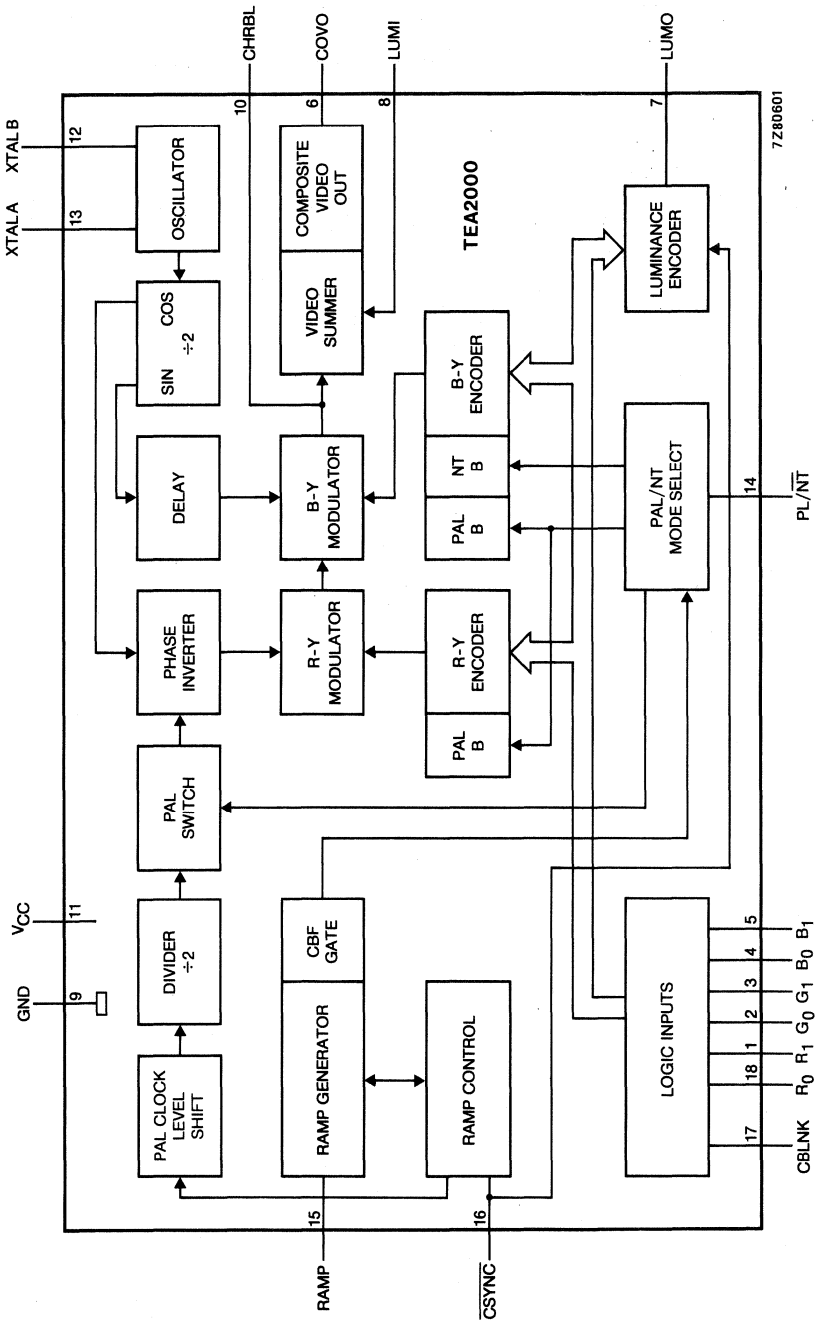


Fig. 1 Block diagram.

PINNING

1. Red 1 binary input
2. Green 0 binary input
3. Green 1 binary input
4. Blue 0 binary input
5. Blue 1 binary input
6. Composite video output
7. Luminance output to delay line
8. Luminance input from delay line
9. Ground 0 volt
10. Chrominance band limiting
11. Supply voltage
12. } Oscillator inputs { 7,16 MHz crystal for NTSC
13. } { 8,86 MHz crystal for PAL
14. PAL/NTSC switch
15. Ramp
16. Composite sync input ($\overline{\text{CSYNC}}$)
17. Composite blanking input (CBLNK)
18. Red 0 binary input

FUNCTIONAL DESCRIPTION

The TEA2000 PAL/NTSC colour encoder and video summer integrated circuit has an internal oscillator from which the (R-Y) and (B-Y) waveforms are generated. The TEA2000 accepts timing signals (composite sync, composite blanking) and a 6 bit binary coded input giving colour information. The inputs are organized as 2 bits per primary colour and gamma correction is applied to the resultant luminance and chrominance levels. Each of the equally spaced intensity levels (for each primary colour) is combined with those of the other primary colours. This produces 64 output colours comprising a wide range of saturated and desaturated colours, black, white and two levels of grey. The resultant output is a composite video signal compatible with the PAL and NTSC/M standards.

PIN DESCRIPTION

R0, R1, G0, G1, B0, B1, pins 18, 1,2,3,4 and 5.
These are the red, green and blue logic inputs. 2 bits per primary colour. These inputs are TTL compatible.

$\overline{\text{CSYNC}}$, pin 16.

Composite sync input requiring a negative logic signal, TTL compatible. For PAL operation the field sync must include line sync information.

XTALA, XTALB, pins 12 and 13.

Oscillator inputs. A crystal in series with a trimmer capacitor is connected between pins 12 and 13. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder. The crystal frequencies are:

PAL mode 8,867238 MHz
NTSC mode 7,15909 MHz

LUMO, LUMI, pins 7 and 8.

Luminance output and input. The combined luminance and sync signal appearing at pin 7 must be d.c. coupled to pin 8 via an appropriate luminance delay line or resistor network. Resistors must have a tolerence of ± 5%, or better, as they affect the d.c. level at COVO, pin 6.

CHRBL, pin 10.

Chrominance filtering can be accomplished by connecting a chrominance frequency tuned filter (4,43 MHz or 3,57 MHZ), via a blocking capacitor to pin 10. This point is the chrominance summing junction and has a nominal internal impedance of 1,5 kΩ. If a filter is used at this point then the delay caused to the chrominance signal should be compensated by an appropriate luminance delay line.

COVO, pin 6.

Composite video output is internally buffered giving a nominal output voltage swing of 2 V sync-white and a nominal sync 5 V level.

PL/$\overline{\text{NT}}$, pin 14.

PAL/NTSC, select input selects PAL mode when HIGH and NTSC mode when LOW. This input is TTL compatable. An internal pull-up resistor selects PAL if the pin is not connected.

RAMP, pin 15.

Ramp timing component connection. A capacitor and resistor connected to pin 15 provide timing information for the colour burst and for PAL phase switching. Alternative components may be used to optimise for NTSC operation.

V_{CC}, pin 11.

12 volt supply.

GND, pin 9.

Ground connection, zero volts.

CBLNK, pin 17.

Blanking input when high, switches off colour inputs. CBLNK must be high during sync and colour burst unless colour inputs are all low at this time. This input is TTL compatible.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage V_{11-9}	max.	13,2	V
Voltages, pin 1,2,3,4,5,14,16,17,18	max.	V_{11-9}	V
Storage temperature		−20 to +125	°C
Operating ambient temperature		0 to + 70	°C

CHARACTERISTICS

V_{11-9} = 12 V; T_{amb} = 25 °C; measured in Fig. 3 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{11-9}	10,8	12	13,2	V
Supply current V_{11-9} = 12 V	I_{11}	–	55	–	mA
Oscillator stability, pins 12 and 13					
Crystal type 4322 143 04051					
V_P = 10,8 to 12 V		–	+50	–	Hz
V_P = 12 to 13,2 V		–	–50	–	Hz
Digital inputs					
$\overline{CSYNC}$, CBLNK, PL/$\overline{NT}$ pins 16,17,14 R0,R1,G0,G1,B0,B1 pins 18,1,2,3,4,5					
V_{IN} (LOW)	V_{IL}	–0,5	–	0,8	V
V_{IN} (HIGH)	V_{IH}	2	–	V_{11-9}	V
Input capacitance	C_i	–	–	10	pF
Input rise and fall times	t_r,t_f	–	–	200	ns
$\overline{CSYNC}$, CBLNK, R0,R1,G0,G1,B0,B1 pins 16,17,18,1,2,3,4,5					
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–100	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	20	μA
PL/$\overline{NT}$, pin 14					
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–500	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	–200	μA
Composite video output, pin 6					
Output amplitude (sync tip-white)	$V_{6-9\ (p-p)}$	–	2	–	V
Sync tip level	V_{6-9}	–	5	–	V
Output load resistor	R_{6-9}	0,47	1	–	kΩ
Variation of output amplitude T_{amb} = 0 to +70 °C	$V_{(p-p)}$	–	–	tbf	%
Over supply range V_{11-9} = 10,8 to 13,2 V	ΔV	–	–	tbf	%
Output impedance (with 1 kΩ load)	R_L	–	15	–	Ω
Residual chrominance on white	ΔV_{rms}	–	30	–	mV
Tolerance on luminance amplitude	ΔV	–	10	–	%
Tolerance on chrominance amplitude	ΔV	–	10	–	%
Tolerance on chrominance phase	ΔΩ	–	tbf	–	%
Chrominance band limiting, pin 10					
Internal resistance	R_{10-11}	–	1,5	–	kΩ
Luminance delay, pins 7 and 8					
Nominal series resistor (±5%)	R_S	–	1,2	–	kΩ
Nominal load resistor at luminance input (±5%)	R_L	–	1	–	kΩ
Ramp timing, pin 15 (see Fig. 4)					
With external RC circuit R = 36 kΩ; C = 330 pF (note 1)					
Start of burst from line sync	t_b	–	5,7	–	μs
Burst width	t_w	–	2,5	–	μs
Threshold for seperation of equalizing pulses and sync pulses	t	36	44	56	μs

Note: 1. A figure of 5 pF is assumed for external capacitance. This figure includes temperature dependence of the components.

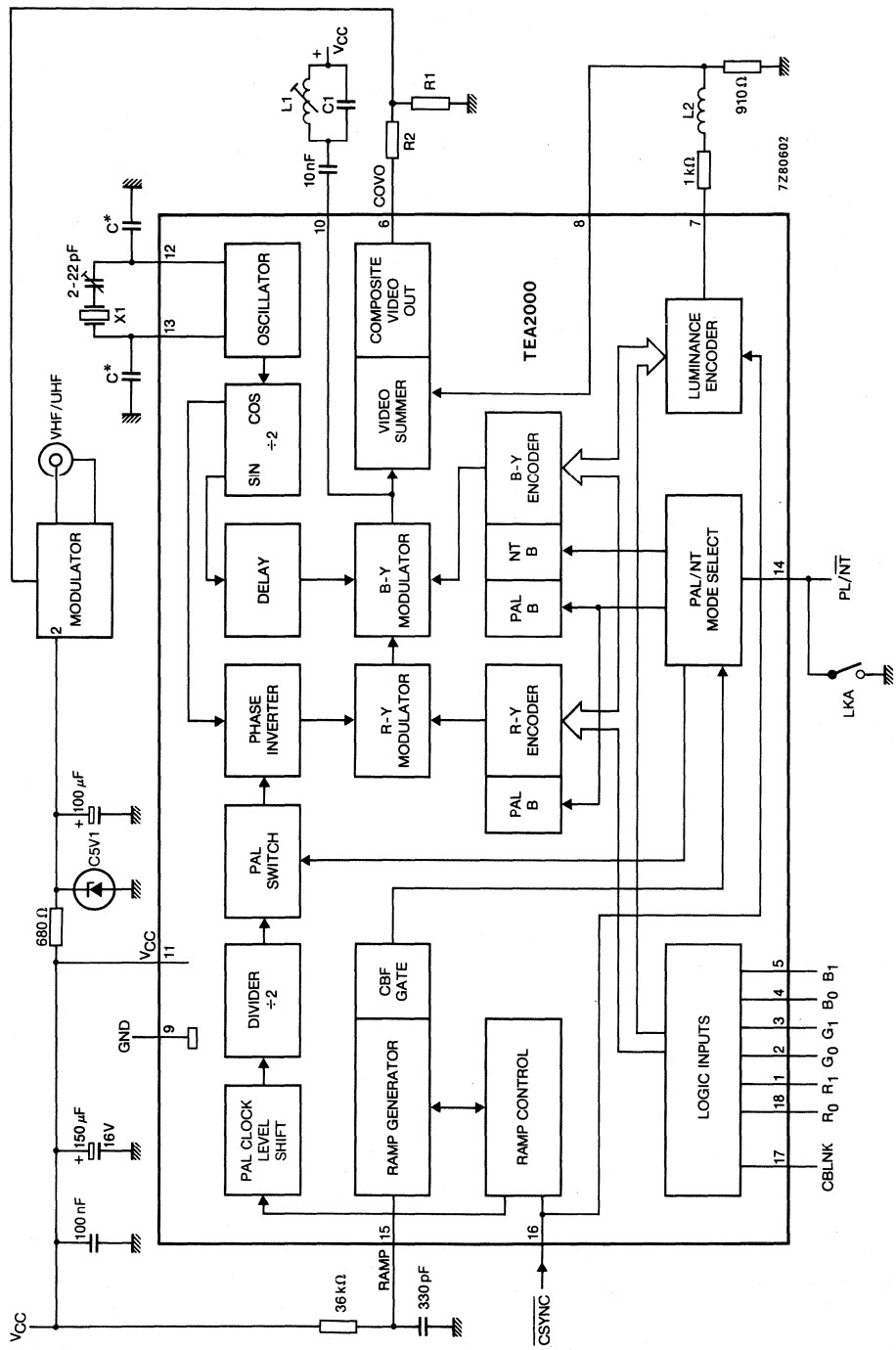


Fig. 2 Internal circuit details and typical external connections.

X1 (PAL) = 8,867238 MHz
X1 (NTSC) = 7,159100 MHz
C* = 5,6 pF only for mask version 1

COMPONENT	PAL	NTSC
L1	15 μH	18 μH
C1	82 pF	100 pF
L2	DL270	DL330
R1	430 Ω	510 Ω
R2	510 Ω	750 Ω
M1	UM1233	UM1622
LKA	o/c	made

Component list for Fig. 2.

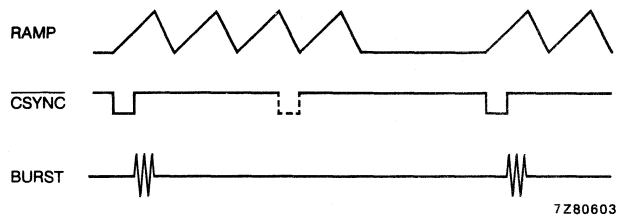


Fig. 3 Ramp timing.

PLL STEREO DECODER (BTSC SYSTEM)

GENERAL DESCRIPTION

The TEA5582, a 20-pin integrated phase-locked loop (PLL) stereo decoder, is designed primarily for low cost stereo decoding in a low- to medium-line TV. The MUX input (pin 1) is a low impedance current input, the gain of the input amplifier is therefore determined by the external resistor R1 (see Fig.5). All characteristics are measured with R1 = 47 kΩ. The de-emphasis of (L, R) and (L−R) can be chosen by means of external capacitors and resistors. The supply voltage range of the device is from 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- LED driver for stereo indicator
- Smooth mono/stereo control
- Matrix and two amplifiers for left and right output signals
- A source selector to switch between the MUX signal and an external signal
- Mute circuit for 60 dB muting of the output level
- External de-emphasis control of (L, R) and (L−R)
- 6 dB fixed attenuation of (L−R) with respect to (L+R) prior to matrix
- All pins are protected against Electrostatic Discharge (ESD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Decoder						
Overall gain	mono; R1 = 47 kΩ	$G_o(V_o/V_i)$	4	5.8	7	dB
AF output voltage (RMS value)		$V_{14} = V_{15}$	–	245	–	mV
Total harmonic distortion	V_o = 600 mV	THD	–	0.3	–	%
Output channel unbalance		$\lvert V_{14}/V_{15}\rvert$	–	0.1	–	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Source selector						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Output amplifiers						
Gain output amplifier						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	−0.5	0	+0.5	dB
AF output voltage (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

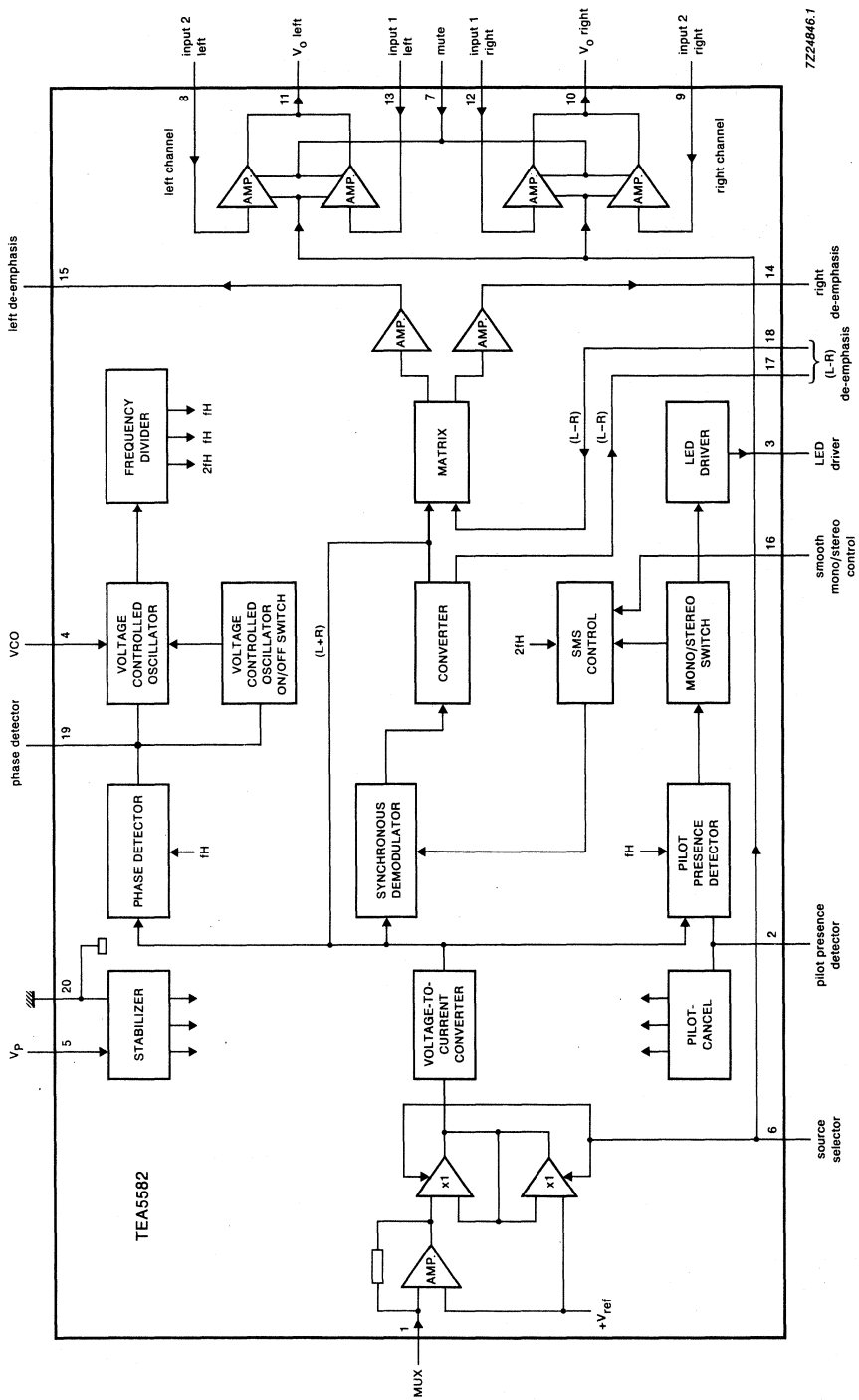


Fig.1 Block diagram.

PINNING

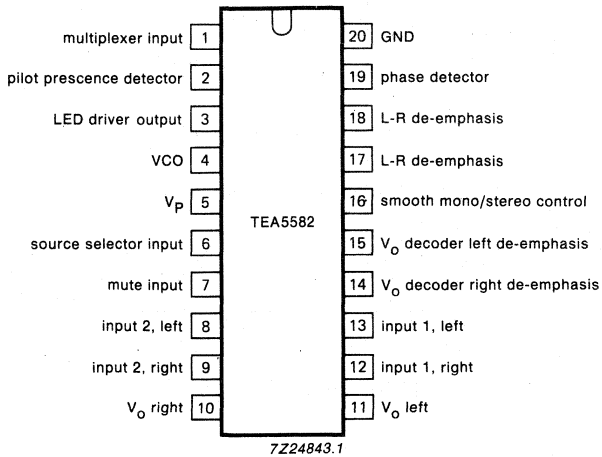


Fig.2 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 5)	V_P	–	18	V
LED-driver current (peak value)	I_3	–	75	mA
Total power dissipation	P_{tot}	see Fig.3		
Storage temperature range	T_{stg}	–65	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C
Electrostatic handling *	V_{es}	–2	+2	kV

* ESD withstand voltage is defined by MIL STD 883C (C = 100 pF; R = 1.5 kΩ).

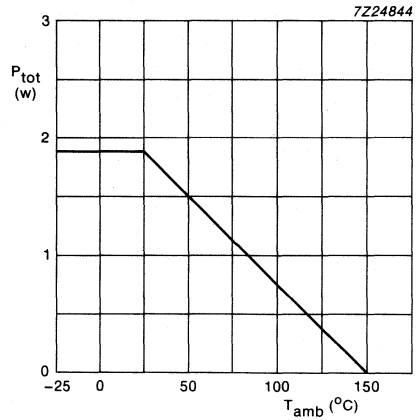


Fig.3 Power derating curve.

DC CHARACTERISTICS

All voltages are with respect to ground (pin 20); all currents are positive into the device; all parameters are measured in the test set-up (see Fig.5) at a nominal supply voltage of V_S = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Power dissipation		P_{tot}	–	160	–	mW
Voltage						
pin 1		V_1	–	2.1	–	V
pins 8, 9, 10, 11, 12 and 13		V_8-V_{13}	–	4.2	–	V
DC output current						
pins 14 and 15		$-I_{14}$, I_{15}	1.1	1.4	1.8	mA
LED-driver current						
pin 3		I_3	–	–	20	mA
Switch "VCO-OFF"						
voltage	I_{19} = 50 μA	V_{19}	–	2	–	V
Switch "VCO-OFF"						
current		I_{19}	50	–	–	μA

AC CHARACTERISTICS

Measured in the test circuit of Fig.5; V_S = 8.5 V; T_{amb} = 25 °C.
AC conditions: (1) input signal (V_i) of 815 mV p-p for L = 1, R = 1 (mono) f_m = 1 kHz (= 80% modulation). (2) MUX input signal (V_i) of 1.2 V p-p for L = 1, R = 0 and no DBX; f_m = 1 kHz (stereo) and V_{pilot} = 200 mV p-p. (3) S1 open, unless specified (without L–R filter); voltage controlled oscillator (VCO) adjusted to 188.8 kHz at V_i = 0 V; values are measured with an external IF roll-off network (–2 dB at 31.5 kHz = $2f_H$) at the input (dashed components RS and CS in Fig.5).
All the above conditions apply unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Overall performance (V_i to V_o)						
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R1 = 47 kΩ	G_o (V_o/V_i)	4	5.8	7	dB
AF output voltage (mono) (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
AF output voltage (mono) (RMS value)		$V_{15} = V_{14}$	–	245	–	mV
Total harmonic distortion	note 1	THD	–	0.3	0.5	%
Output voltage	THD = 1%	$V_{11} = V_{10}$	–	800	–	mV
Output channel unbalance		$\lvert V_{11}/V_{10} \rvert$	–	0.1	1	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Signal-to-noise ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
Pilot presence detector	note 2					
Switching to:						
stereo		V_{pilot}	–	40	60	mV
mono		V_{pilot}	15	30	–	mV
hysteresis		ΔV_{pilot}	–	2.5	–	dB
Smooth mono/stereo control (pin 16)	see Fig.4					
Channel separation (α)						
Full stereo	$V_{16} \geqslant 1.25$ V	α	24	28	–	dB
Smooth operation	V_{16} = typ. 1 V	α	–	10	–	dB
Full mono	$V_{16} \leqslant 0.75$ V	α	–	–	1	dB
Attenuation (L–R)			–	6	–	dB

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f_{pilot} = 15.734 kHz (1 fH)	αfH	32	36	–	dB
Subcarrier suppression f = 2 fH		α2fH	–	60	–	dB
VCO suppression f = 12fH		α12fH	–	75	–	dB
SAP signal suppression (Second Audio Programme) f = 5fH		α5fH	–	60	–	dB
Intermodulation suppression	note 4					
f_m = 8.367 kHz	spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 10.823 kHz	spurious signal f_s = 1 kHz	α_3	–	70	–	dB
Ripple rejection	f = 120 Hz; V_{ripple} = 100 mV; mono	RR_{120}	–	50	–	dB
VCO						
R adjust (R5)	f_{osc} = 188.808 kHz R7 = 10 kΩ 5% C6 = 820 pF 1%	R_{adj}	0	–	8	kΩ
Capture range	deviation from f_{osc} centre frequency; V_{pilot}=200 mV p-p	$\Delta f/f$	–	4.5	–	%
Temperature coefficient	uncompensated	TC	–	250 x 10^{-6}	–	K^{-1}
Output amplifiers						
Gain						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	–0.5	0	+0.5	dB
Input impedance		Z_i	–	50	–	kΩ
Output impedance		Z_o	–	10	–	Ω
External load impedance		Z_1	10	–	–	kΩ
External load capacitance		Z_1	–	–	1.5	nF
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
DC offset voltage at outputs	mute OFF-to-ON	ΔV	–	10	50	mV
	mute ON-to-OFF	ΔV	–	10	50	mV
Source selector (pin 6)						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Switching level	MUX selected					
voltage		V_{IL}	–	–	0.8	V
current	$V_I = 0.8$ V	I_{IL}	–	10	25	μA
Switching level	external selected					
voltage		V_{IH}	2	–	V_P	V
current	$V_I = V_P$	I_{IH}	–	0.1	1	μA
Muting circuit (pin 7)						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2	–	V_P	V
Input current	mute ON; $V_{IL} = 0.8$ V	$-I_{IL}$	–	10	25	μA
	mute OFF; $V_{IH} = V_P$	I_{IL}	–	0.1	1	μA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Adjustable.
3. S1 closed; reference: AF output voltage f = 1 kHz (mono).
4. Intermodulation suppression (Beat-Frequency Components (BFC)):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 8.367\text{ kHz}) - fH$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 10.823\text{ kHz}) - 2fH$$

measured with 100% modulated input signal: L = R; pilot signal = 200 mV p-p; f_m = 8.367 or 10.823 kHz.

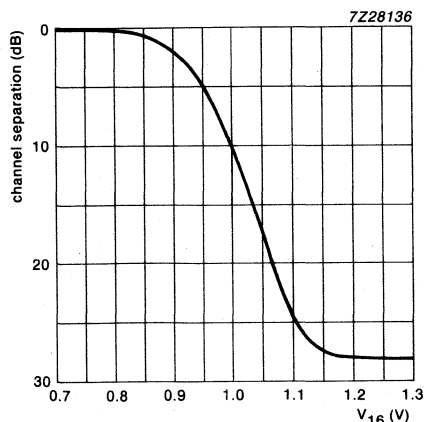


Fig.4 Smooth mono/stereo control.

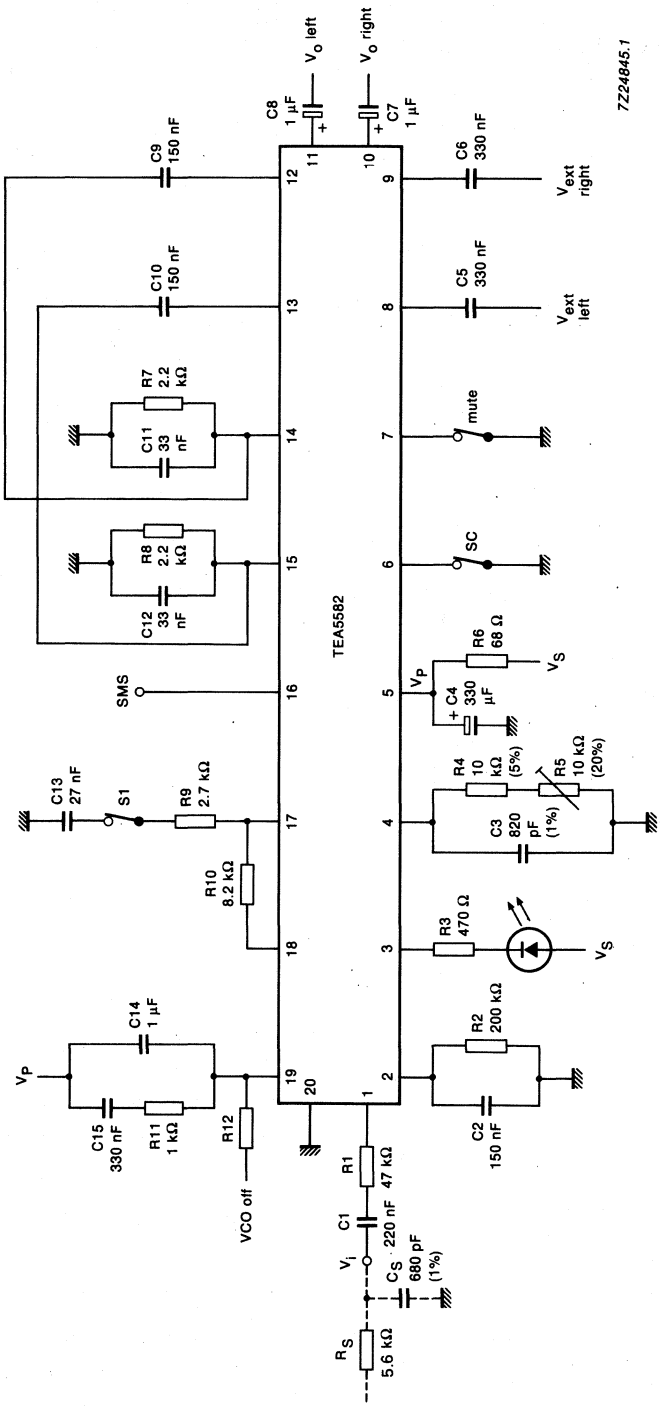


Fig.5 Test and application circuit.

μA733/733C
Differential Video Amplifier

Product Specification

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

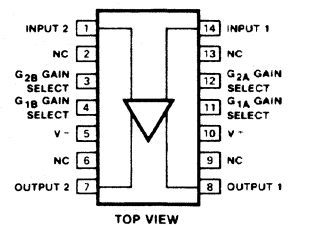
- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10, 100, and 400**
- **No frequency compensation required**
- **MIL-STD-883A, B, C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

PIN CONFIGURATION

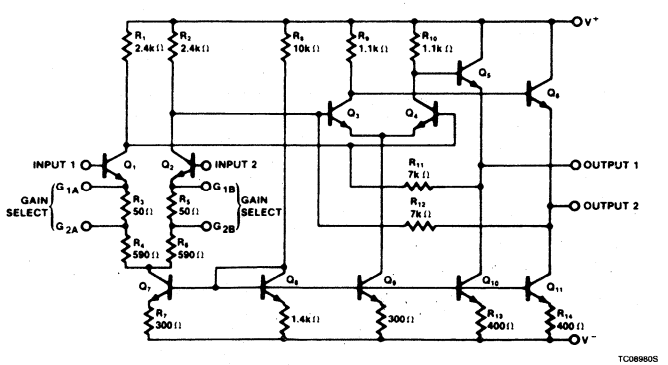
F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA733F
14-Pin Plastic DIP	−55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN
14-Pin Ceramic DIP	0 to +70°C	μA733CF

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range μA733C μA733	 0 to +70 −55 to +125	 °C °C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1] F package N package	 1190 1420	 mW mW

NOTE:
1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0, unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain Gain 1[2] Gain 2[2] Gain 3[3]	R_l = 2kΩ, V_{OUT} = 3V_{P-P}	 250 80 8	 400 100 10	 600 120 12	 300 90 9	 400 100 10	 500 110 11	 V/V V/V V/V
BW	Bandwidth Gain 1[1] Gain 2[2] Gain 3[3]			 40 90 120			 40 90 120		 MHz MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = 1V_{P-P}		 10.5 4.5 2.5	 12 		 10.5 4.5 2.5	 10 	 ns ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = 1V_{P-P}		 7.5 6.0 3.6	 10 		 7.5 6.0 3.6	 10 	 ns ns ns
R_{IN}	Input resistance Gain 1[2] Gain 2[2] Gain 3[3]		 10 	 4.0 30 250	 	 20 	 4.0 30 250	 	 kΩ kΩ kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW = 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2 Gain 2	 V_{CM} = ±1V, f ≤ 100kHz V_{CM} = ±1V, f = 5MHz	 60 	 86 60	 	 60 	 86 60	 	 dB dB
SVRR	Supply voltage rejection ratio Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB

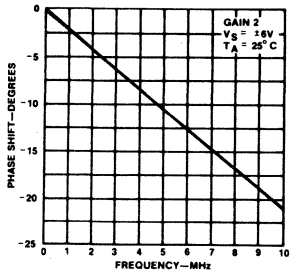
DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$		 0.6 0.35	 1.5 1.5		 0.6 0.35	 1.5 1.0	 V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**-55°C ≤ T_A ≤ 125°C**			
	Differential voltage gain Gain 1[1] Gain 2[2] Gain[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8		 600 120 12	 200 80 8		 600 120 12	 V/V V/V V/V
R_{IN}	Input resistance Gain 2[2]		 8			 8			 kΩ
I_{OS}	Input offset current				6			5	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2	$V_{CM} = \pm V$, $F \leq 100kHz$	50			50			dB
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$			 1.5 1.5			 1.5 1.2	 V V
V_{DIFF}	Output voltage swing, differential	$R_L = 2k\Omega$	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



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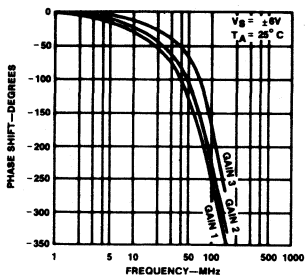
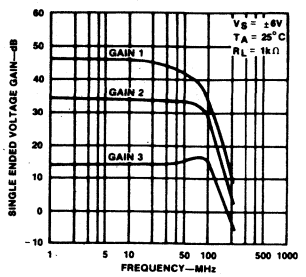
Phase Shift as a Function of Frequency



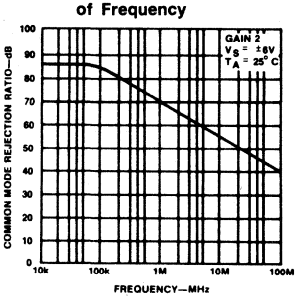
OP05630S

Voltage Gain as a Function of Frequency



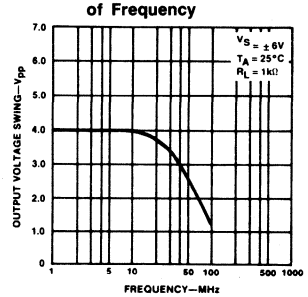
OP05640S

Common Mode Rejection Ratio as a Function of Frequency



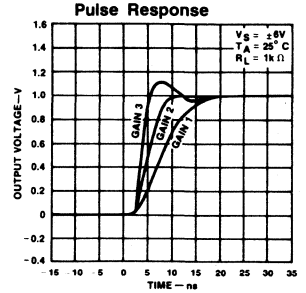
OP05650S

Output Voltage Swing as a Function of Frequency



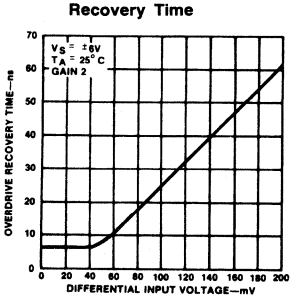
OP05660S

Pulse Response



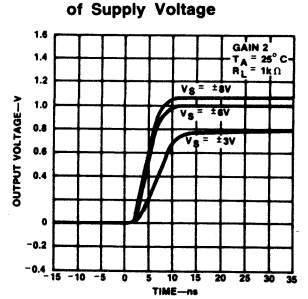
OP05670S

Differential Overdrive Recovery Time



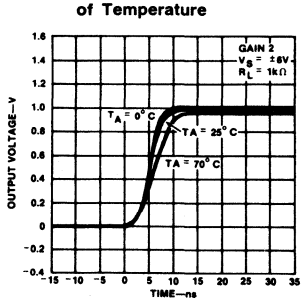
OP05680S

Pulse Response as a Function of Supply Voltage



OP05690S

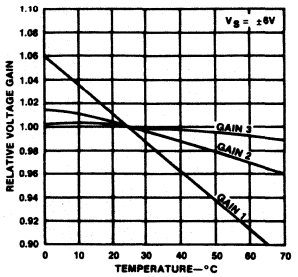
Pulse Response as a Function of Temperature



OP05700S

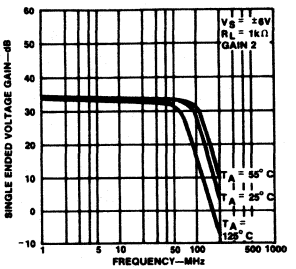
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



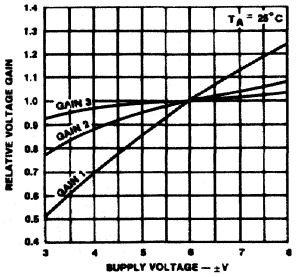
OP05710S

Gain vs Frequency as a Function of Temperature



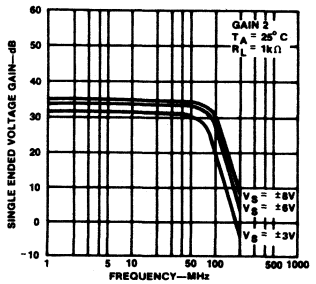
OP05720S

Voltage Gain as a Function of Supply Voltage



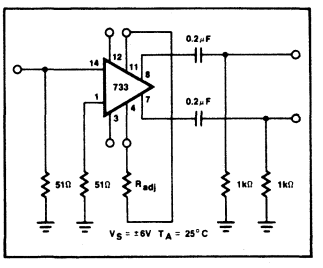
OP05730S

Gain vs Frequency as a Function of Supply Voltage



OP05740S

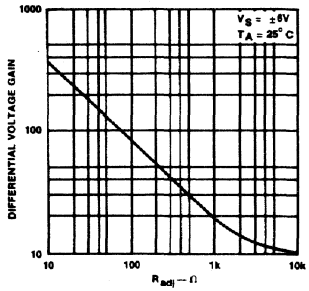
Voltage Gain Adjust Circuit



(Pin numbers apply to K Package)

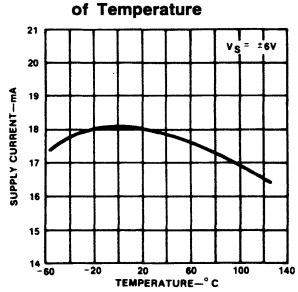
OP05750S

Voltage Gain as a Function of RADJ (Figure 3)



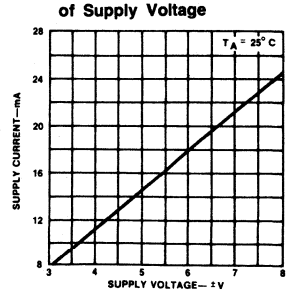
OP05760S

Supply Current as a Function of Temperature



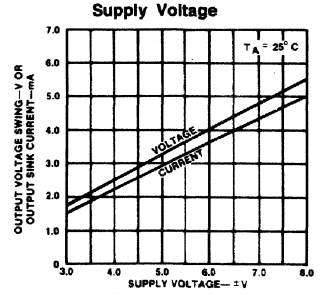
OP05770S

Supply Current as a Function of Supply Voltage



OP05780S

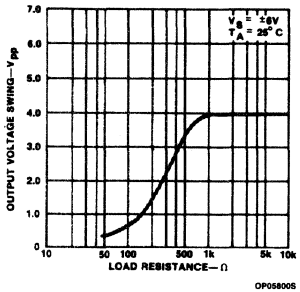
Output Voltage and Current Swing as a Function of Supply Voltage



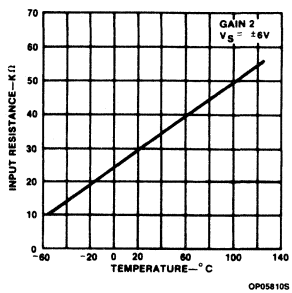
OP05790S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

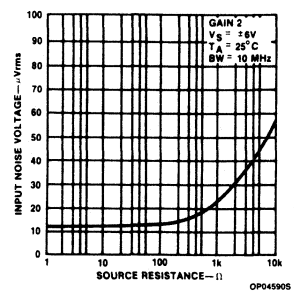
Output Voltage Swing as a Function of Load Resistance



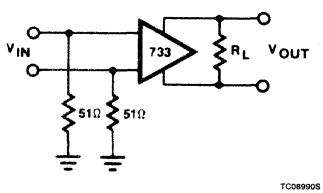
Input Resistance as a Function of Temperature

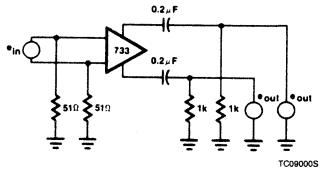


Input Noise Voltage as a Function of Source Resistance



TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



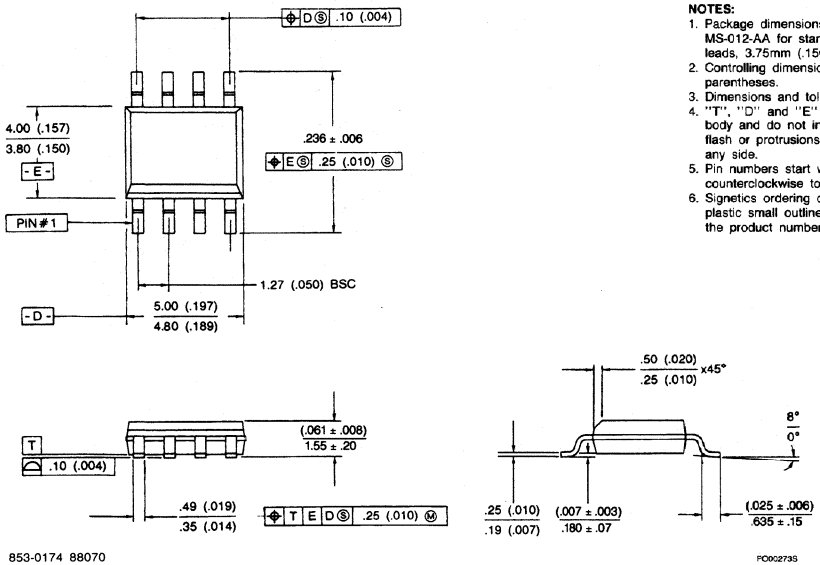


PACKAGE INFORMATION

Package outlines

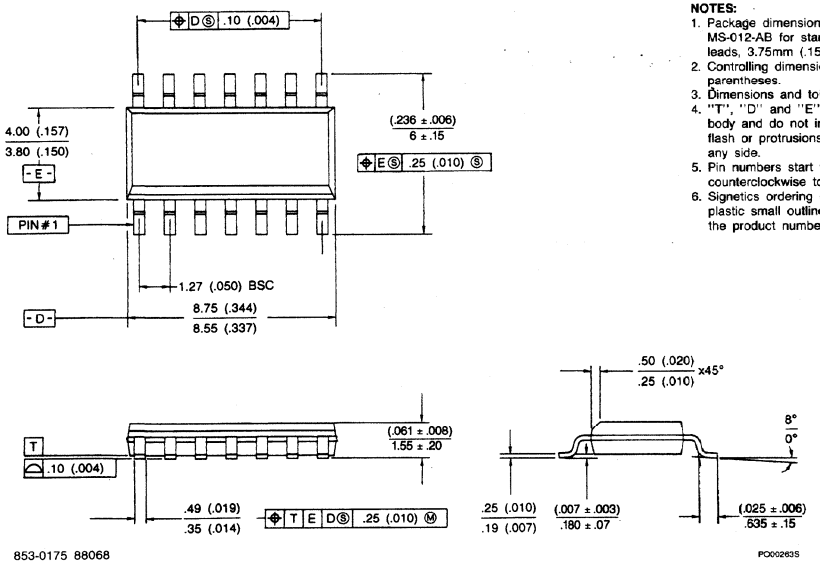
Soldering

8-PIN PLASTIC SO (D PACKAGE)



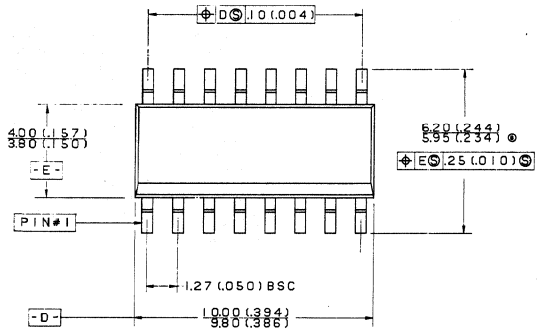
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-PIN PLASTIC SO (D PACKAGE)



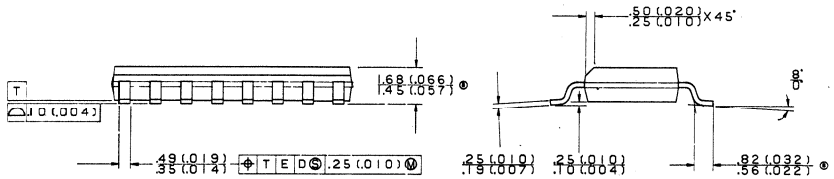
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE)



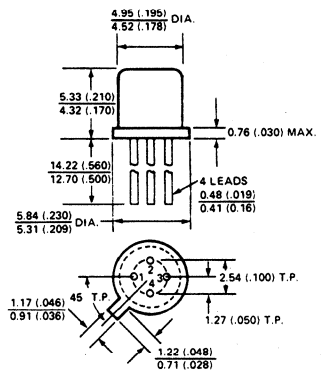
NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AC FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 16 LEADS, 3.75MM (.150") BODY WIDTH (ISSUE A, JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#16 WHEN VIEWED FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.



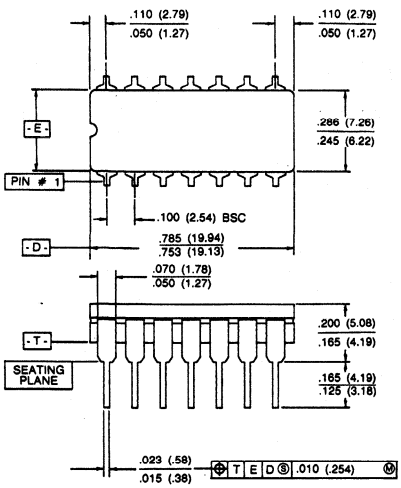
853-0005 91504

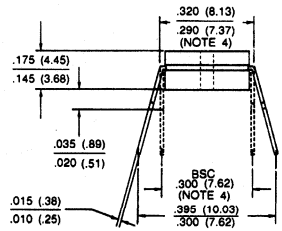
4-PIN HERMETIC TO-72 HEADER (E PACKAGE)



PO00970S

14-PIN CERDIP (F PACKAGE)



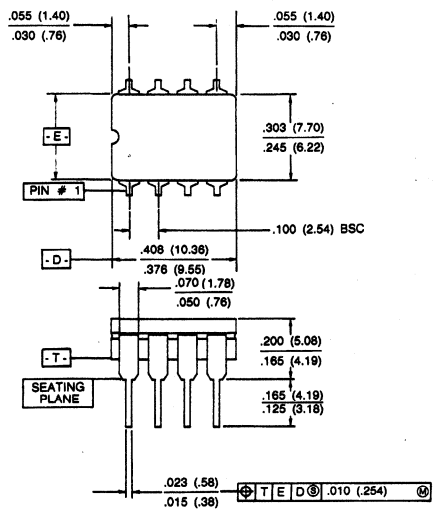


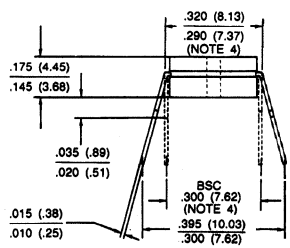
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0581 81594

PO00440S

8-PIN CERDIP (FE PACKAGE)



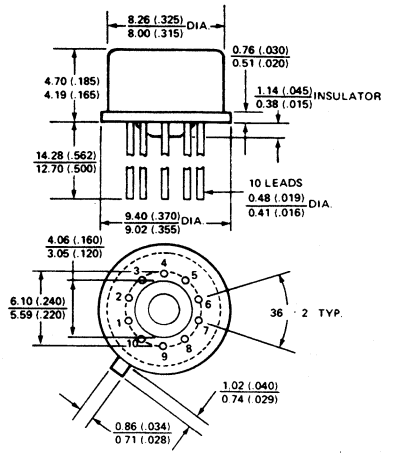


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

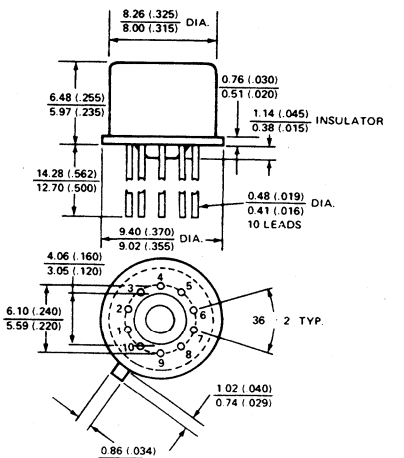
853-0580 81594

PO00480S

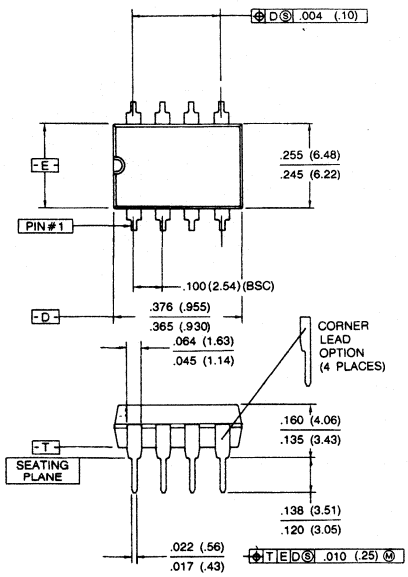
10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)

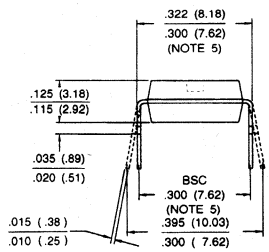


10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)



8-PIN PLASTIC PDIP (N PACKAGE)



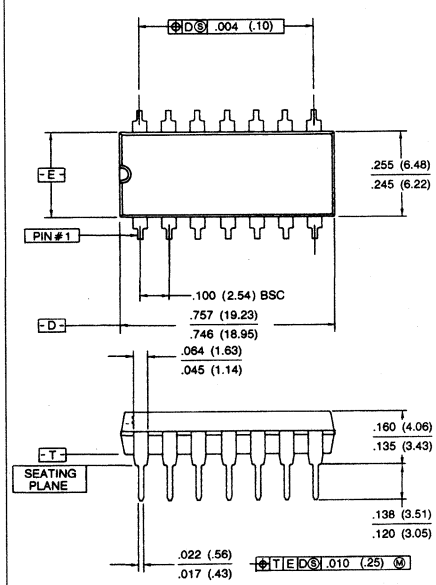


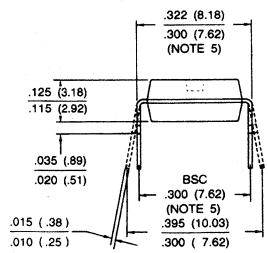
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

14-PIN PLASTIC DIP (N PACKAGE)



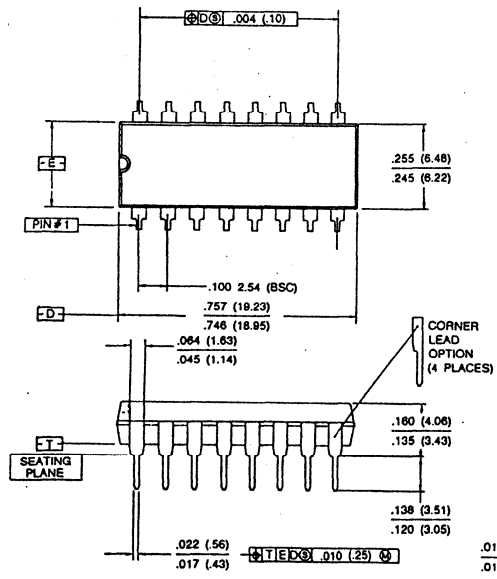


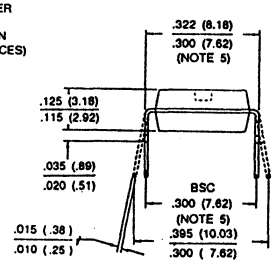
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

PO00330S

NJ1 16-PIN PLASTIC PDIP





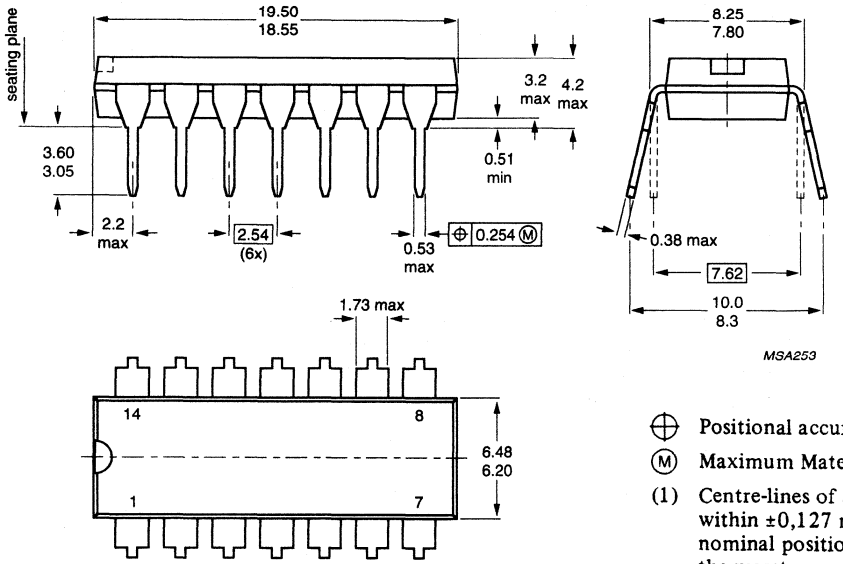
NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14: 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO002905

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



⊕ Positional accuracy.

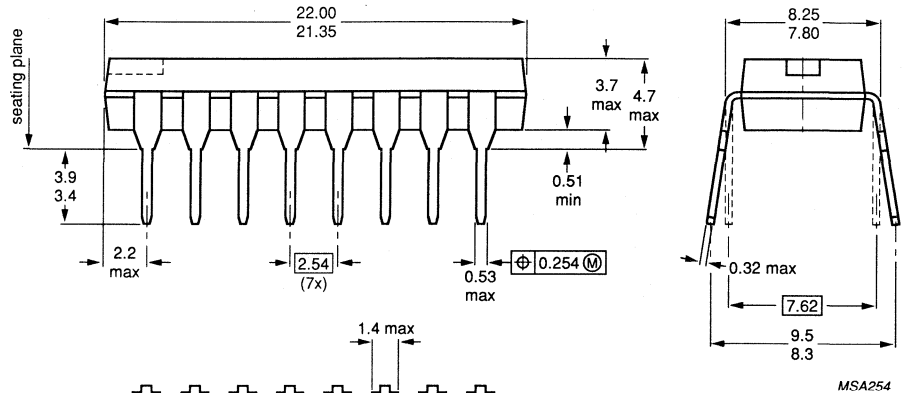
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



⊕ Positional accuracy.

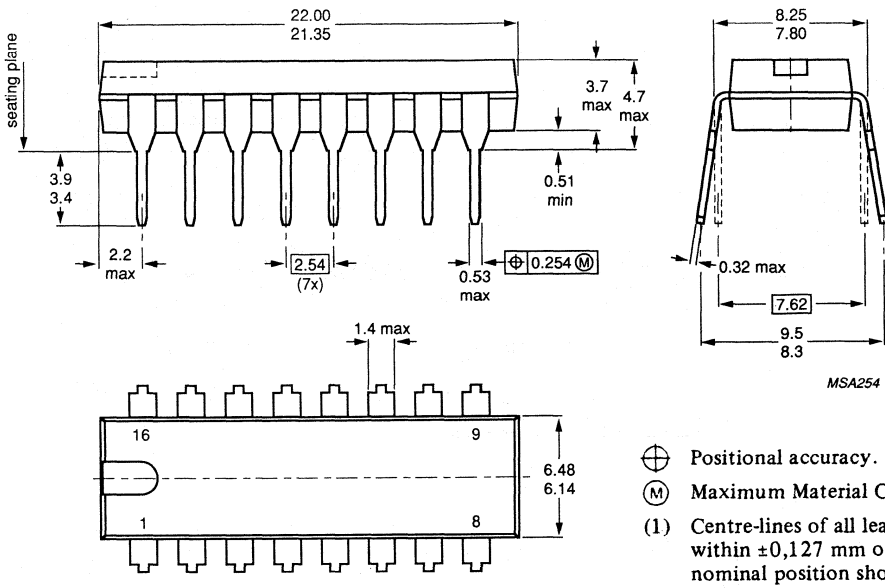
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)



⊕ Positional accuracy.

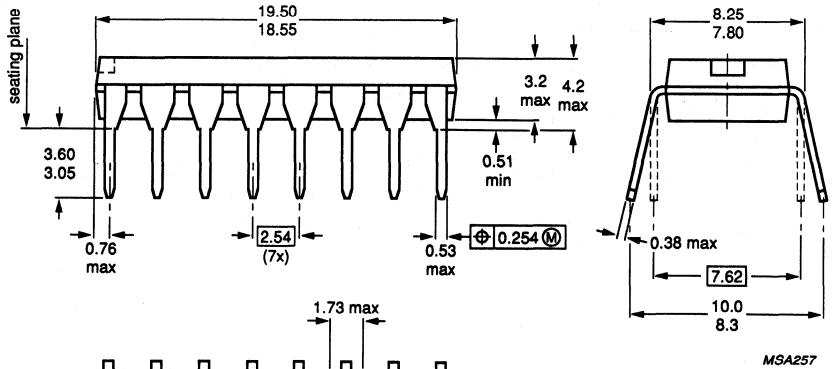
Ⓜ Maximum Material Condition.

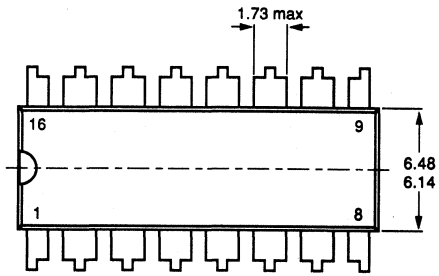
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38D)





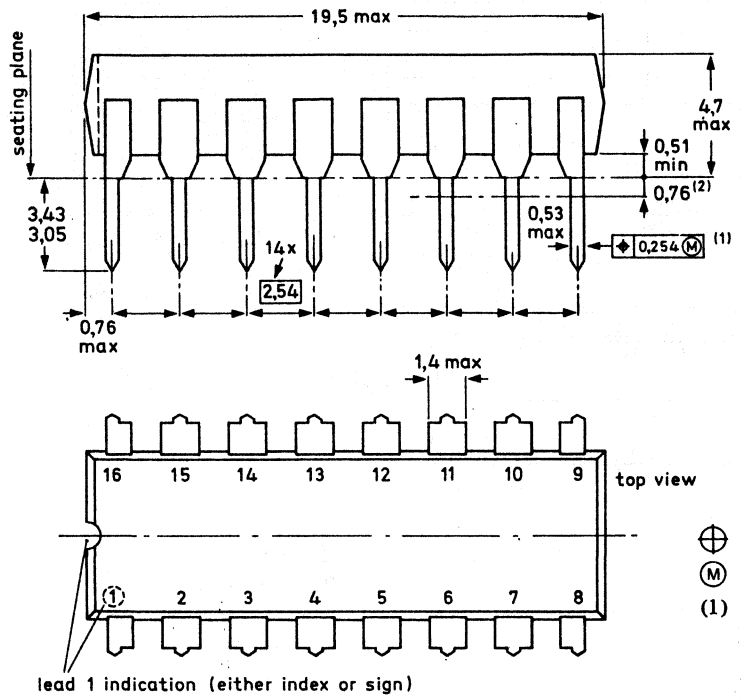
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

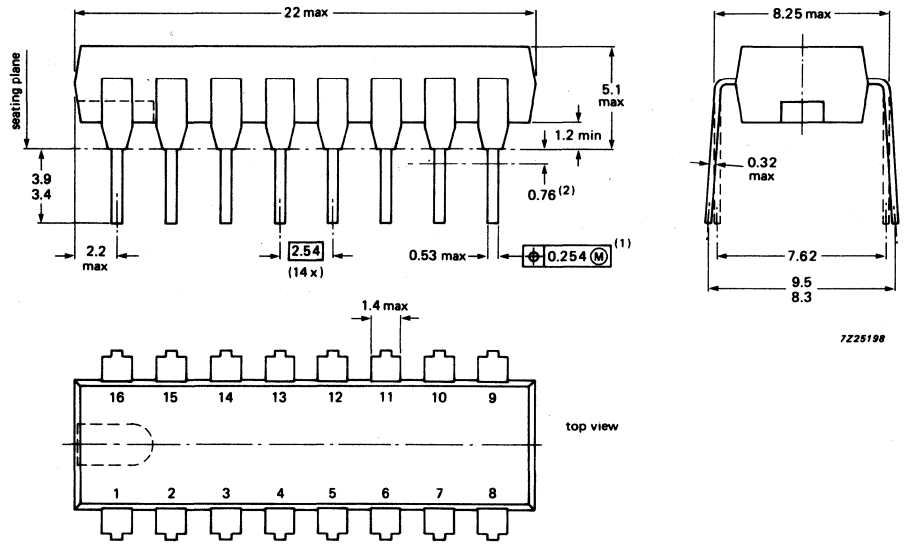
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (OPPOSITE BENT LEADS) (SOT38WBE)

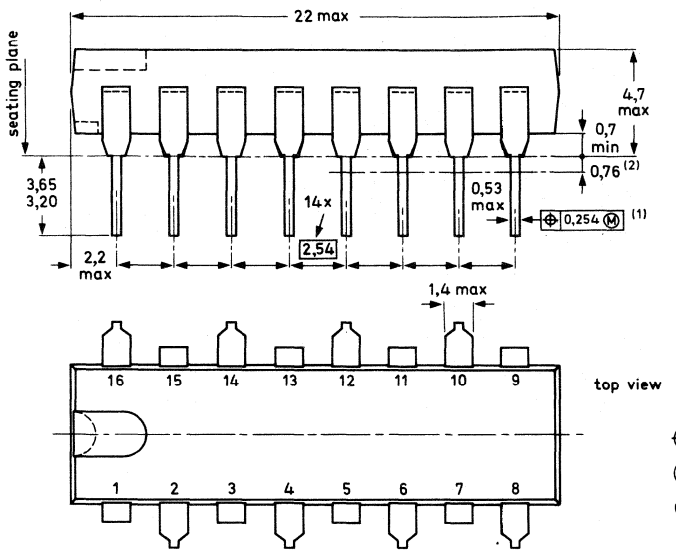


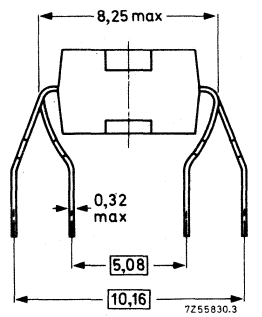
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT58)





⊕ Positional accuracy.

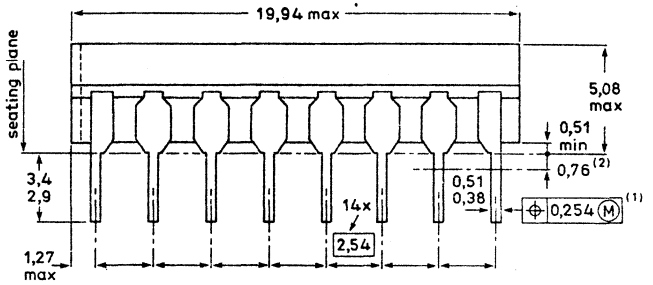
Ⓜ Maximum Material Condition.

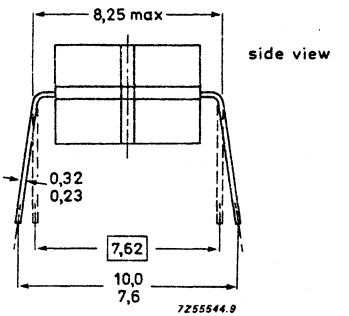
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

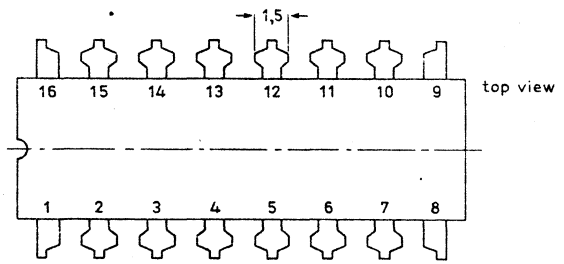
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT74)







Dimensions in mm

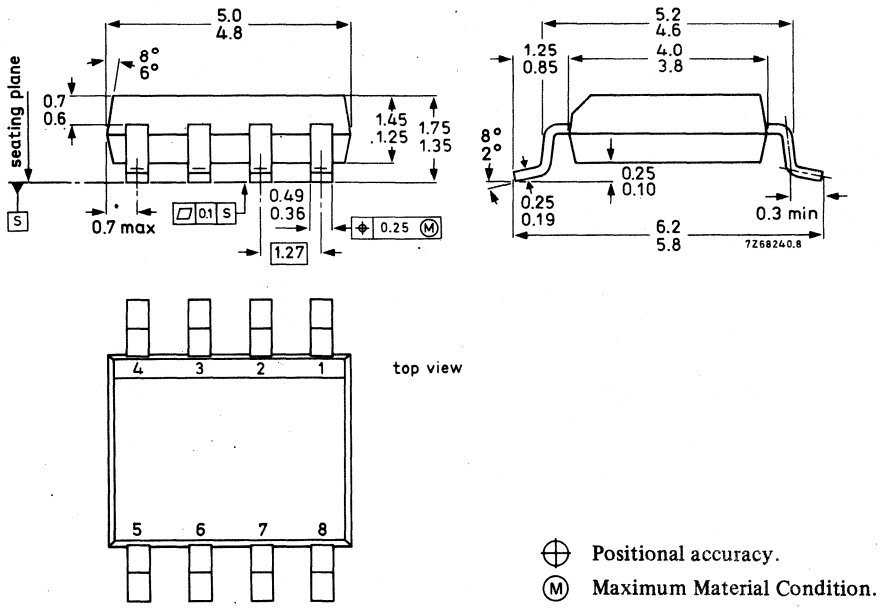
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

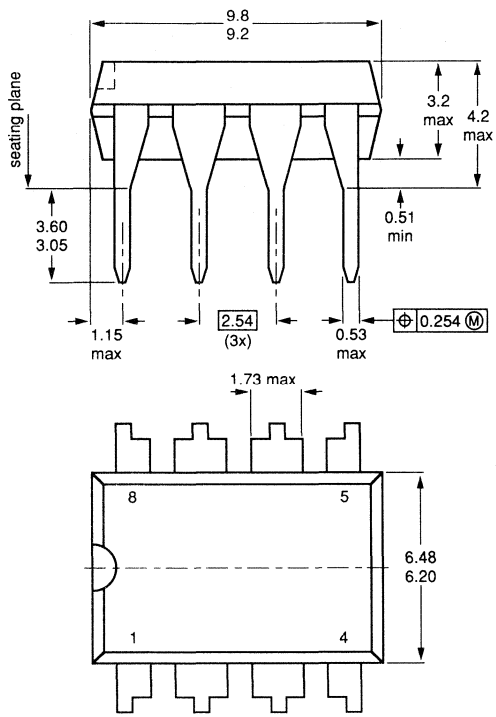


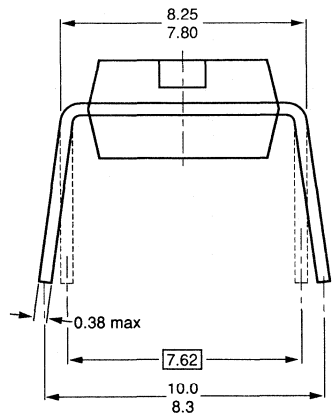
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





MSA252

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

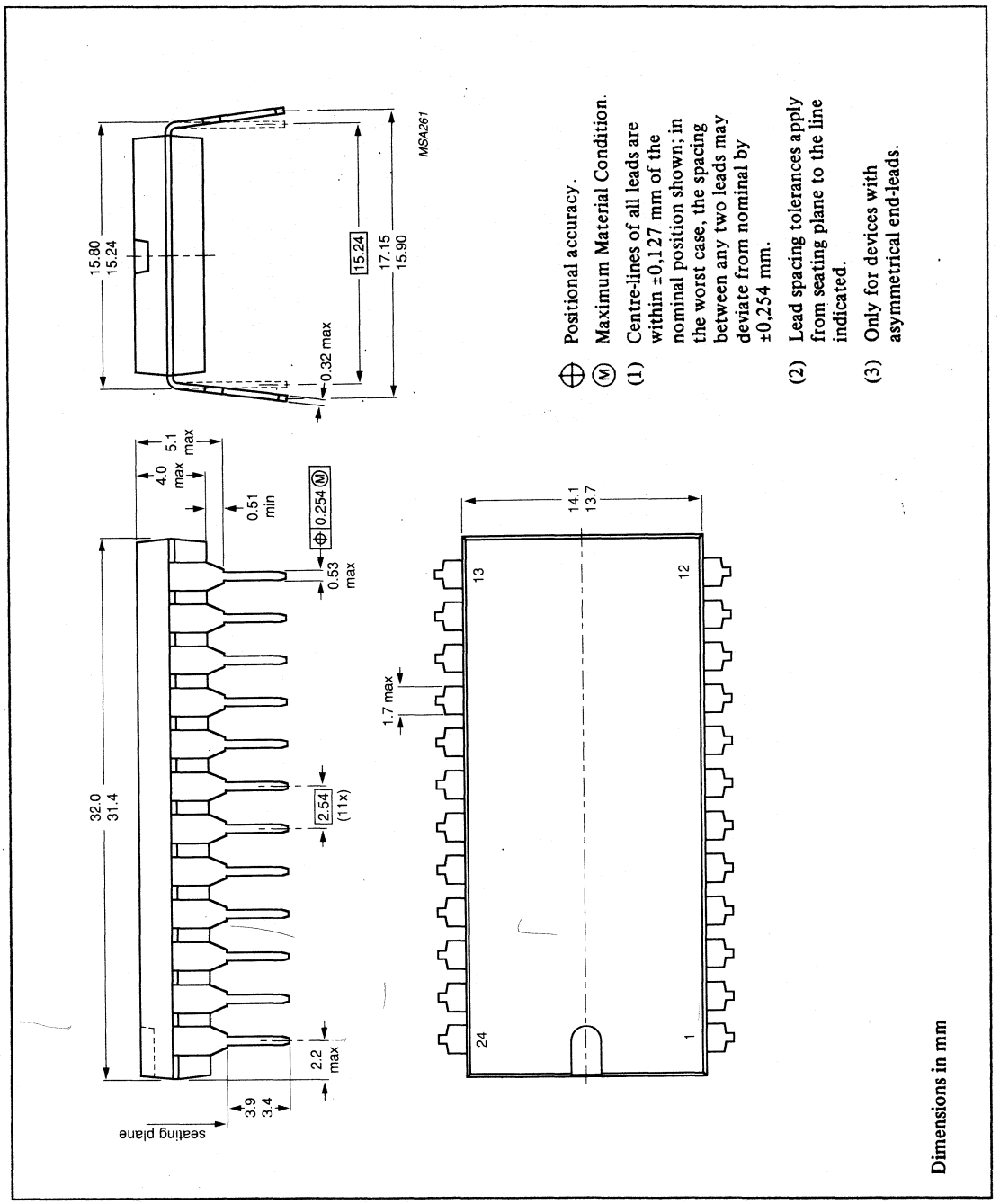
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT 101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

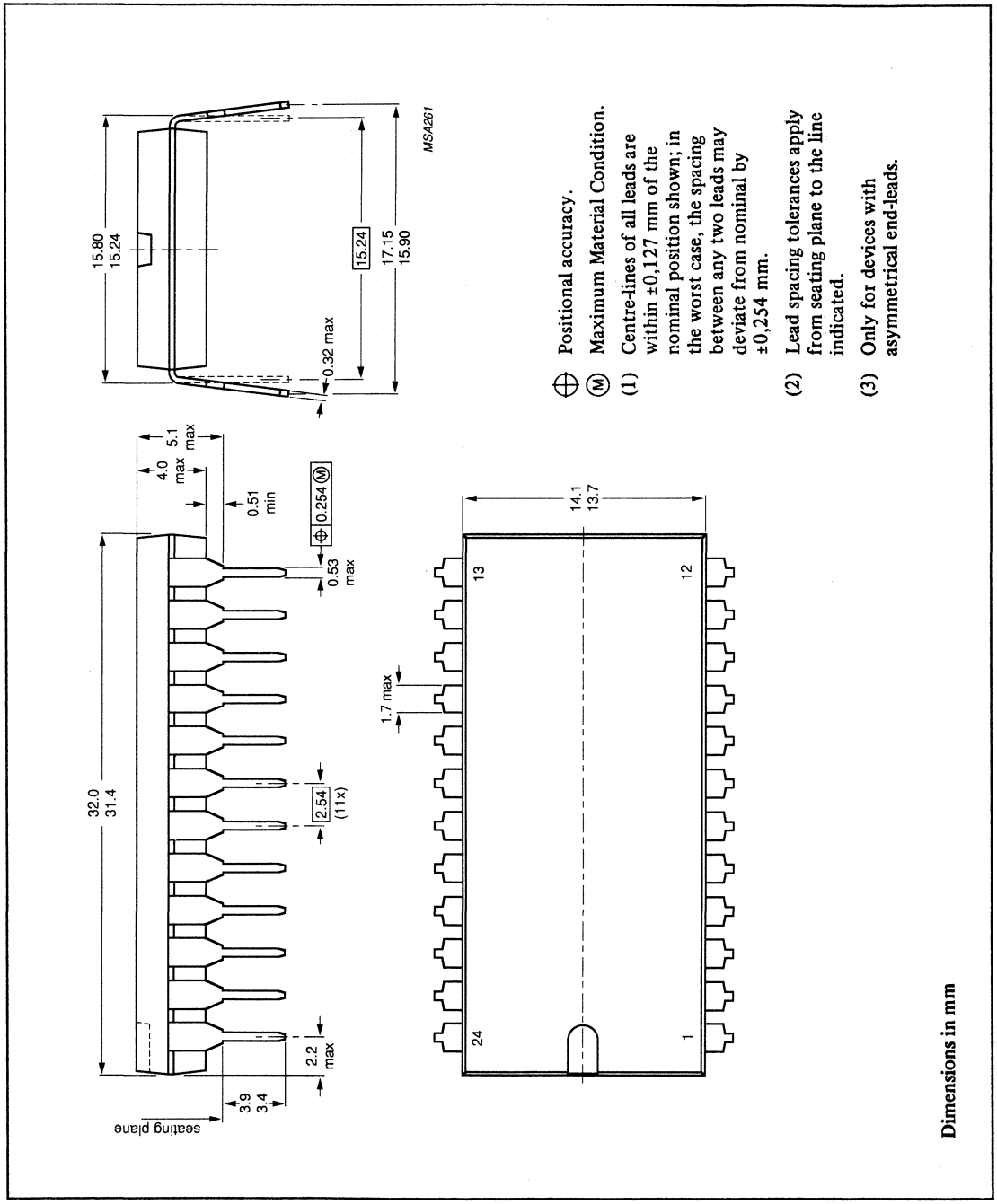
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

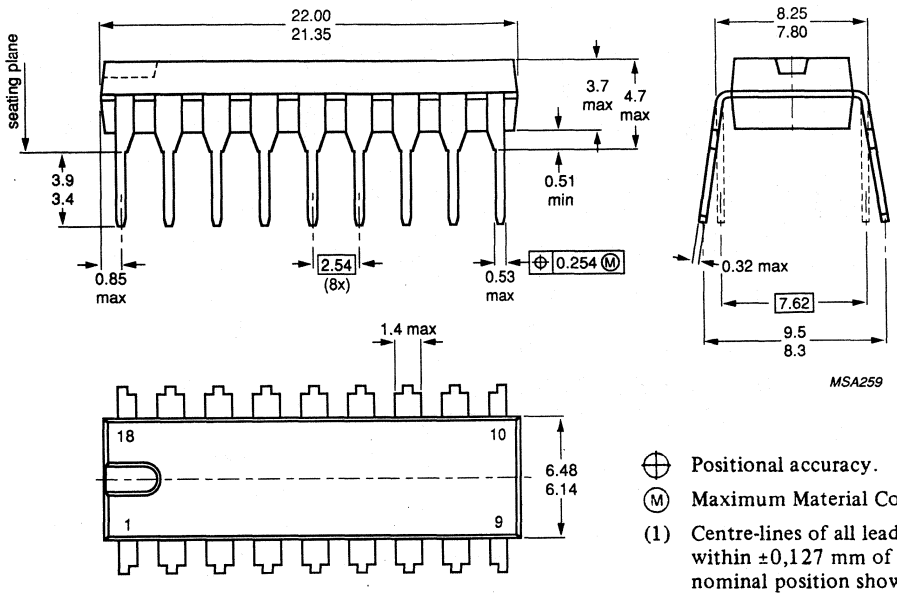
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)



⊕ Positional accuracy.

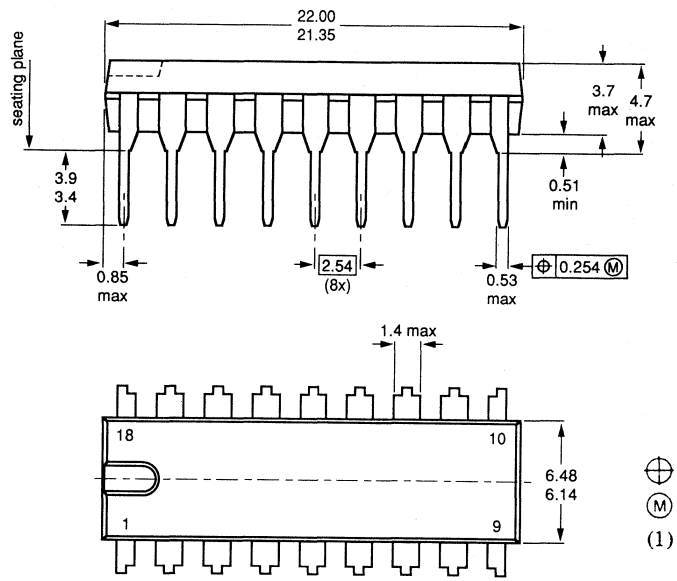
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT102)



⊕ Positional accuracy.

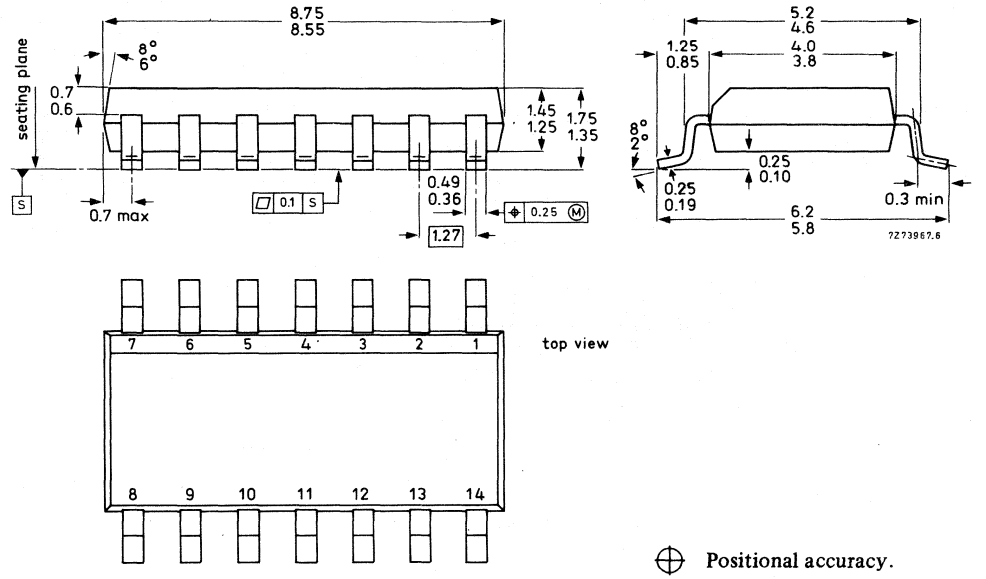
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO14; SOT108A)

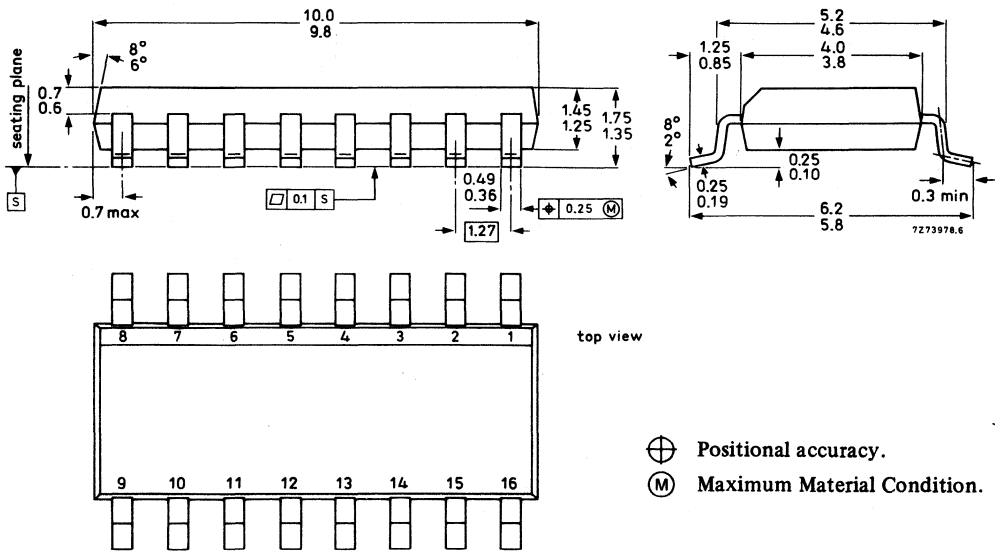


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimension in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

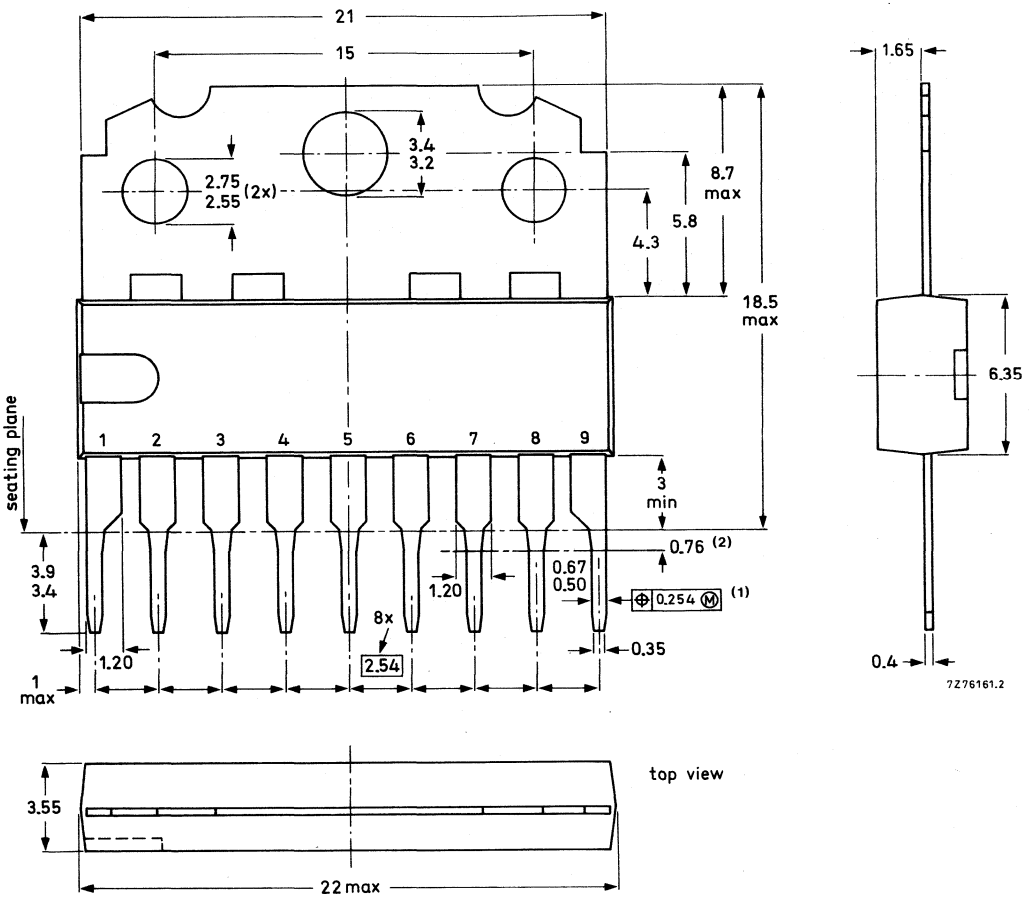


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

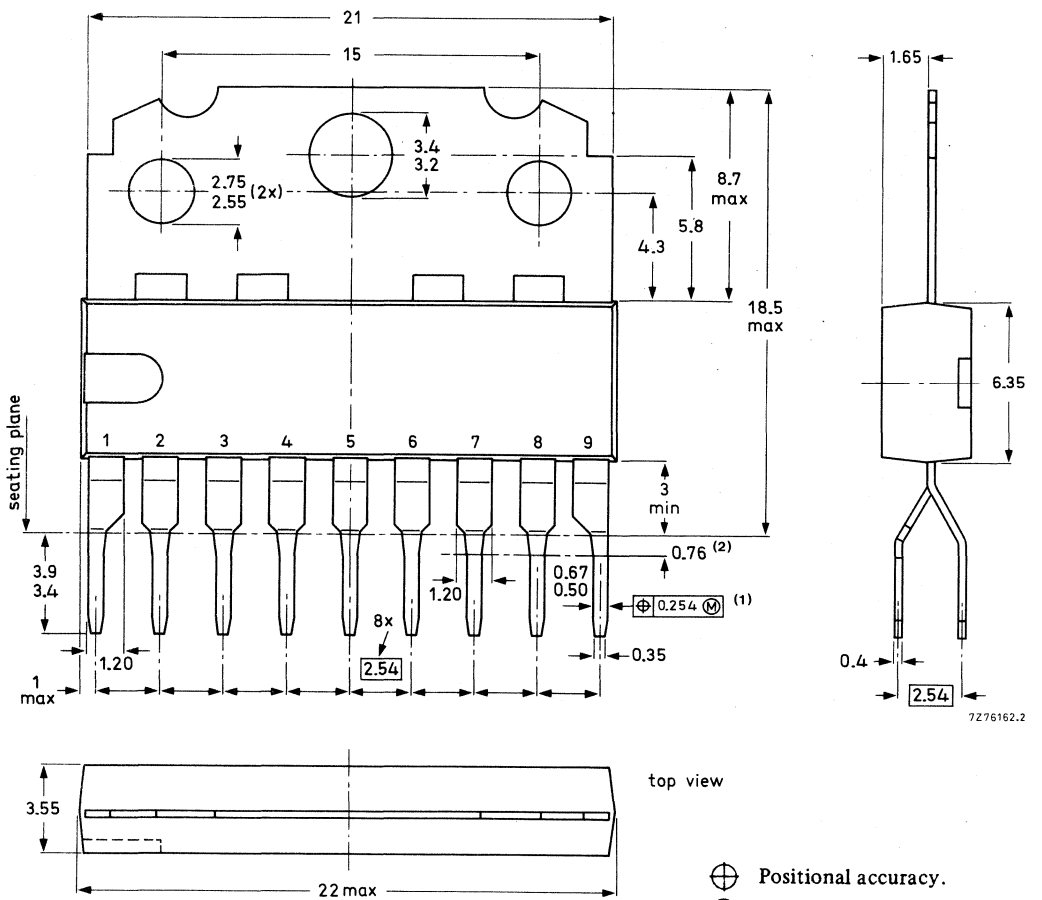
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SIL-BENT-TO-DIL; PLASTIC (SOT111B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

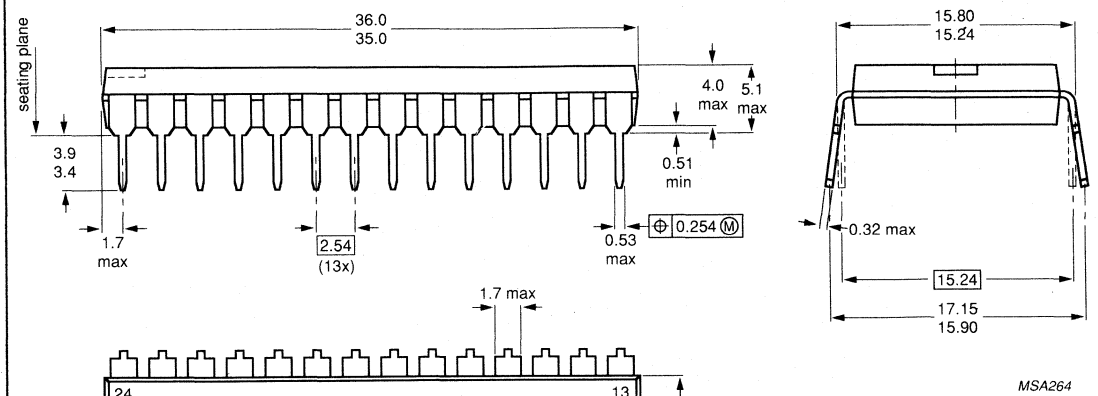
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

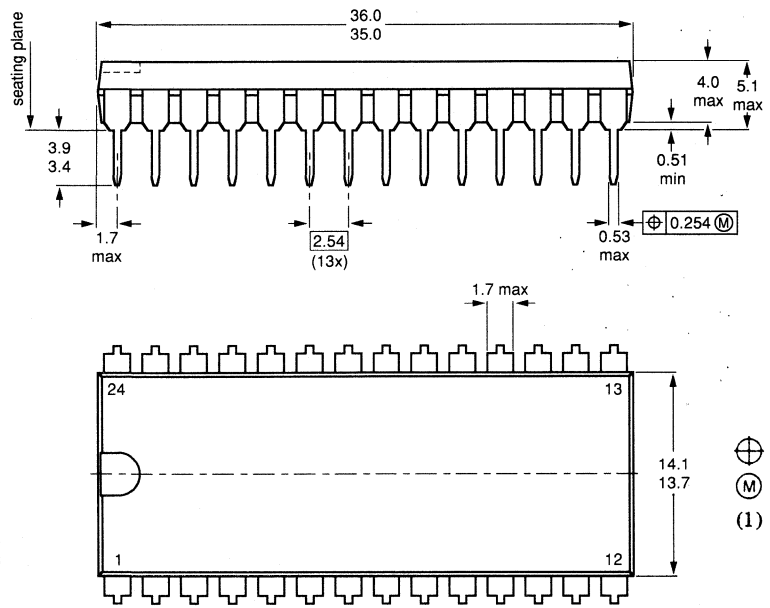
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

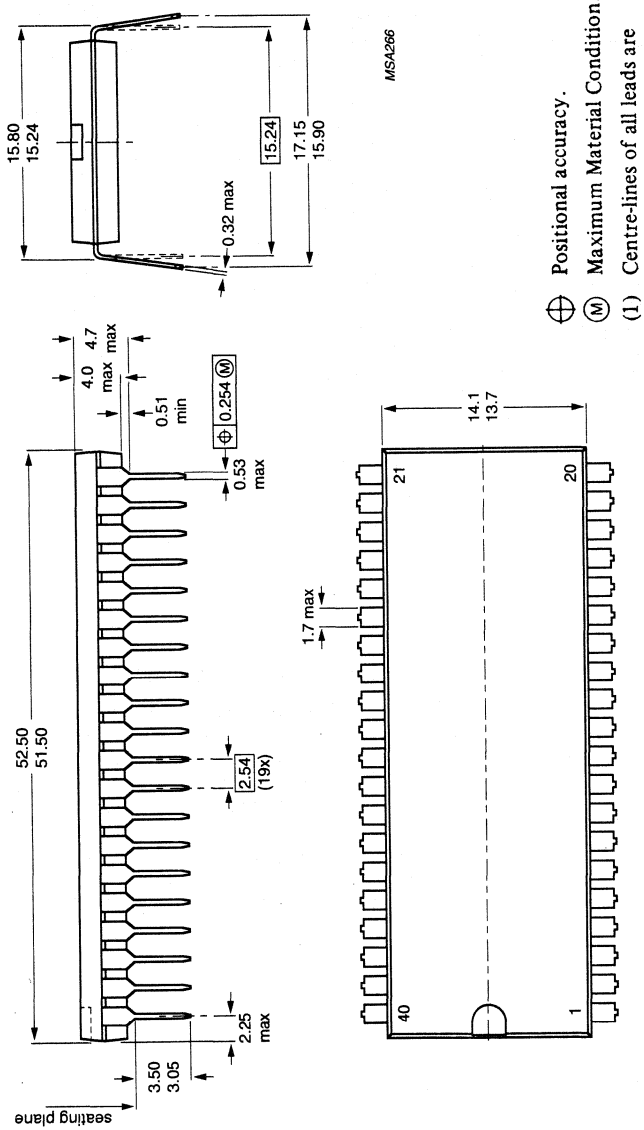
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

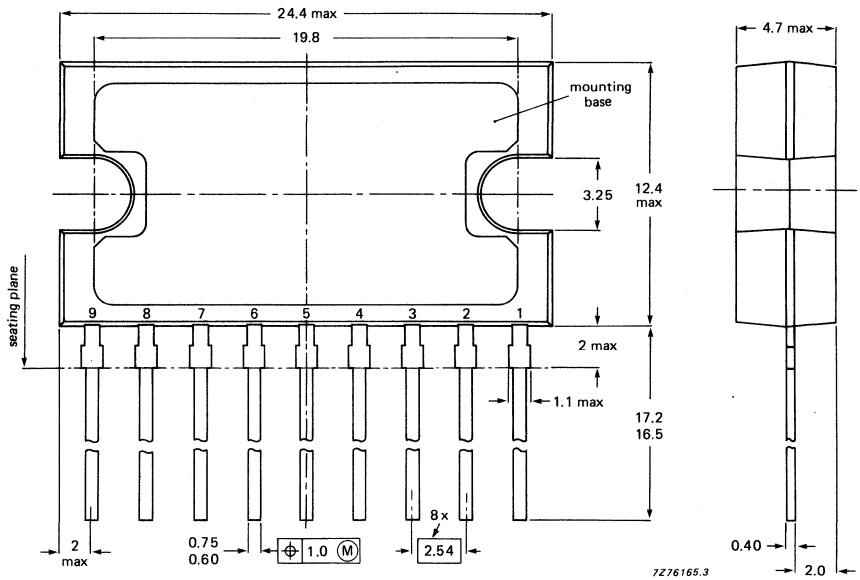
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT131)



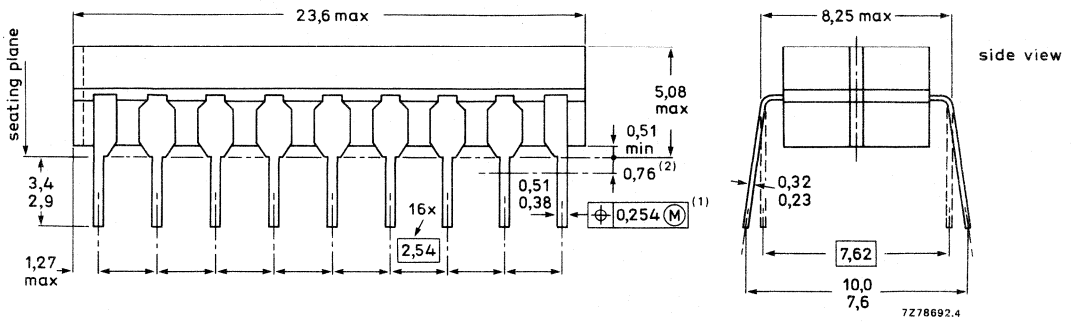
⊕ Positional accuracy.

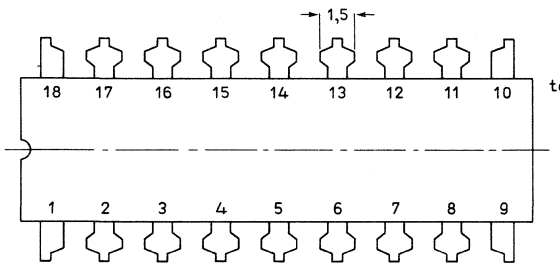
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT133B)





Dimensions in mm

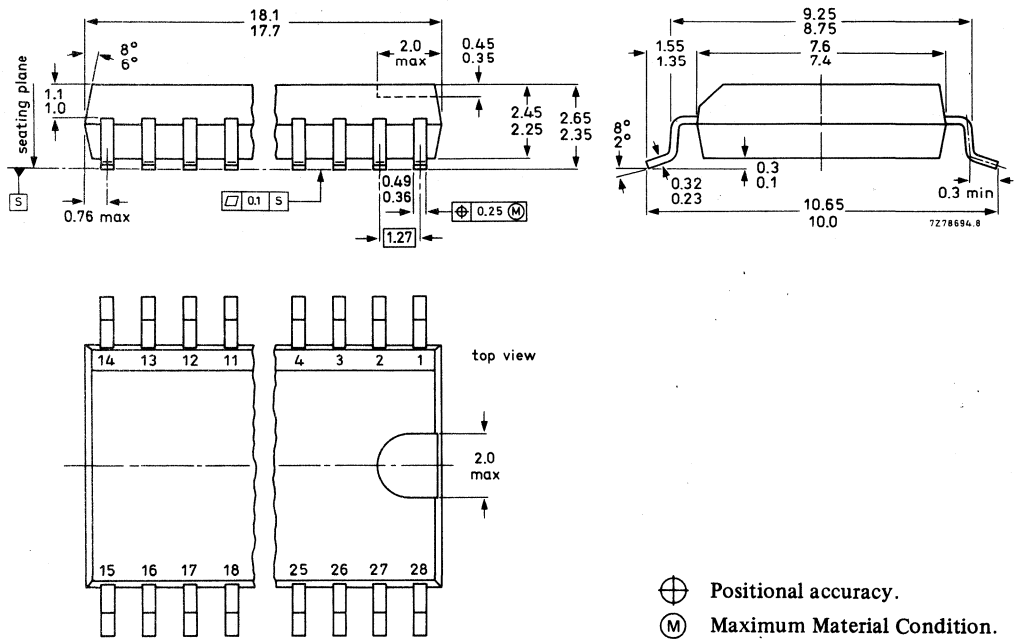
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

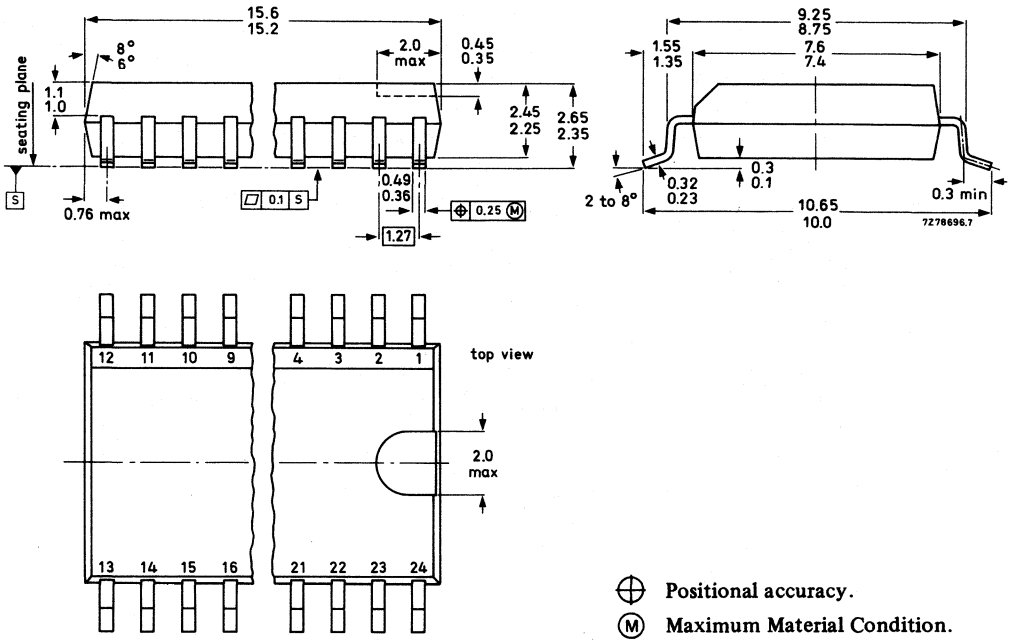


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

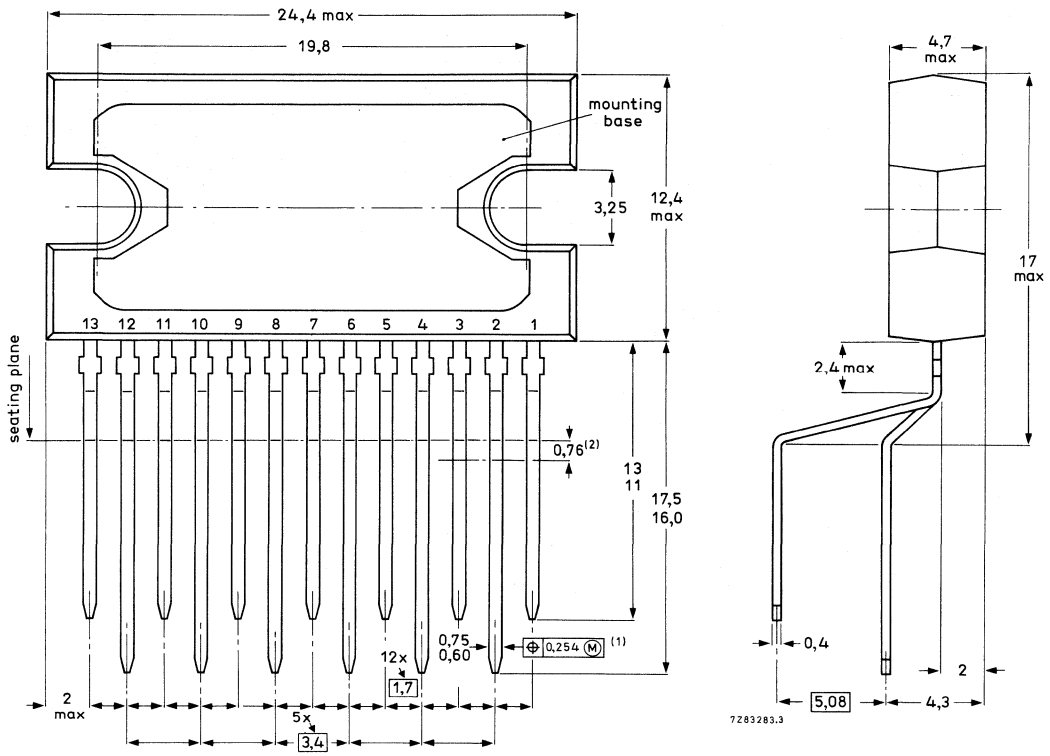
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT 141BE, CE)



⊕ Positional accuracy.

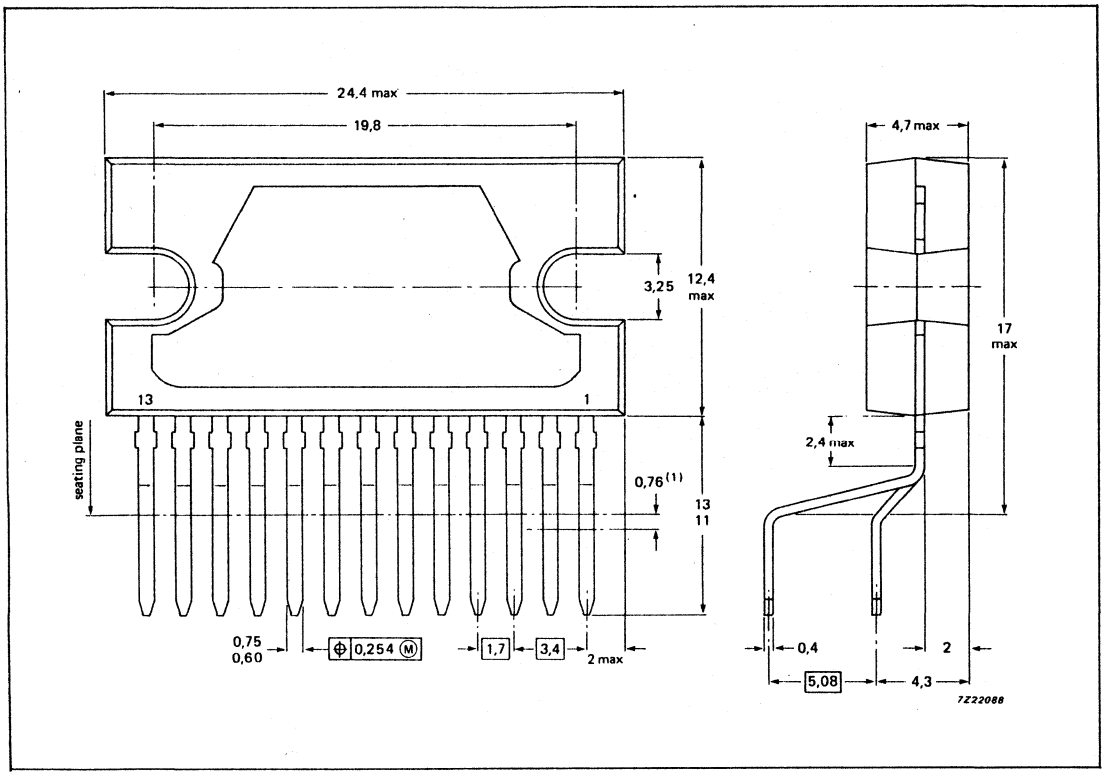
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

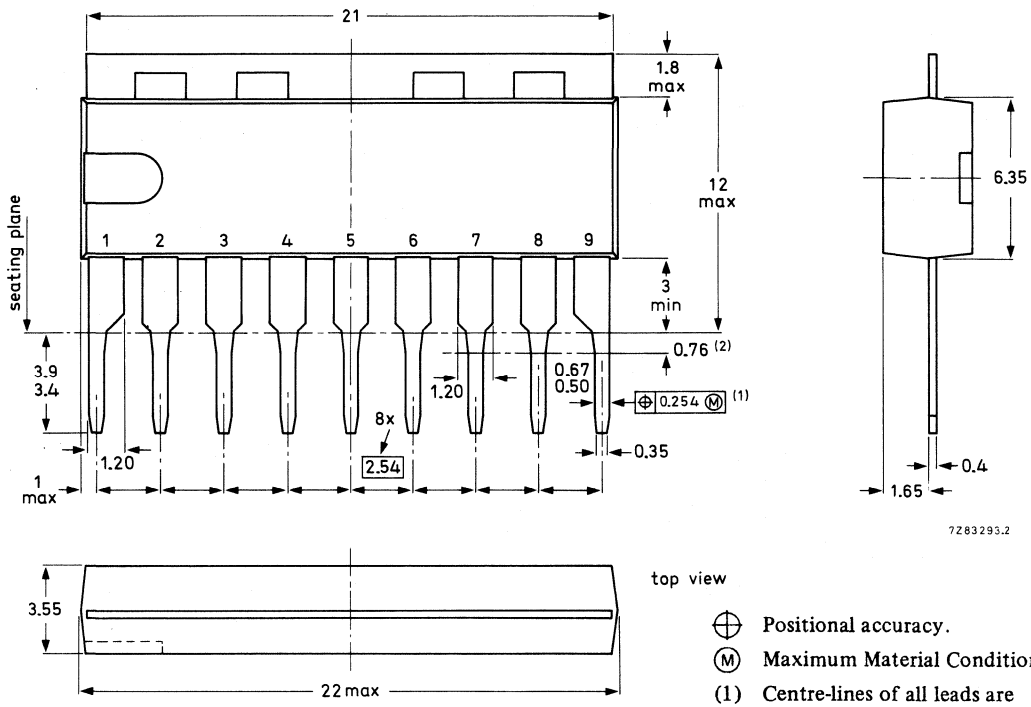
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT141RAA)



9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

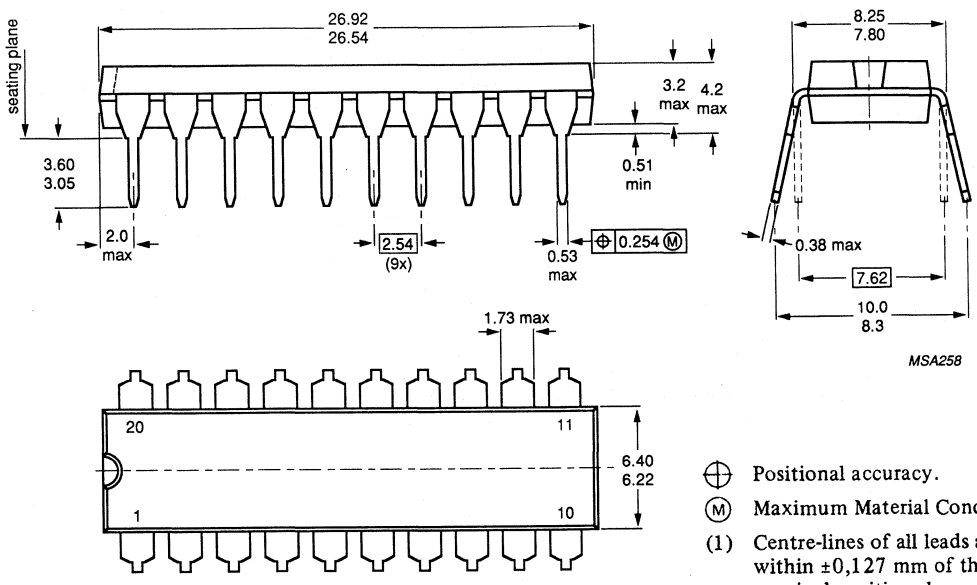
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

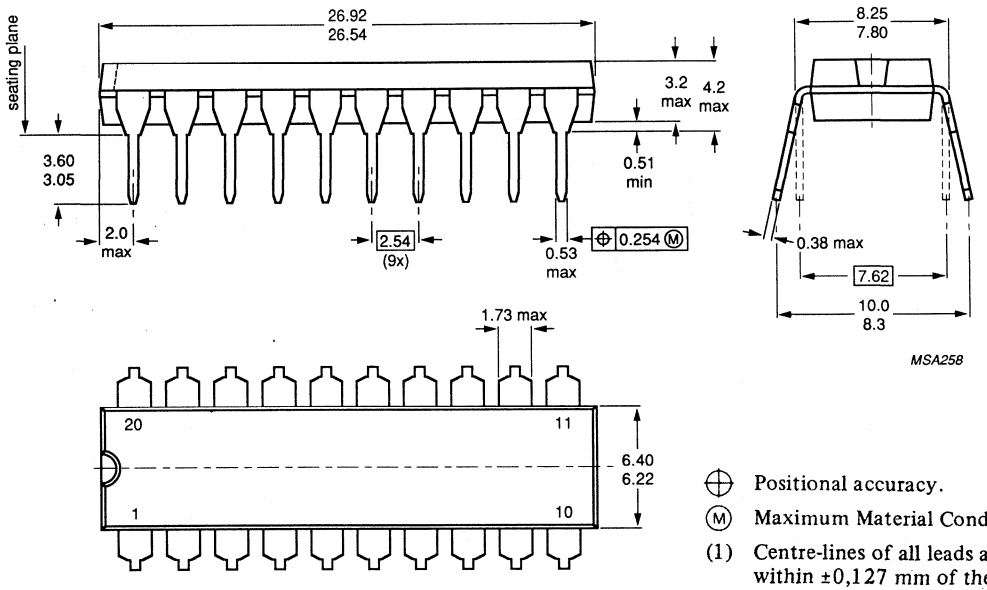
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUA IN LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT146EE7)



⊕ Positional accuracy.

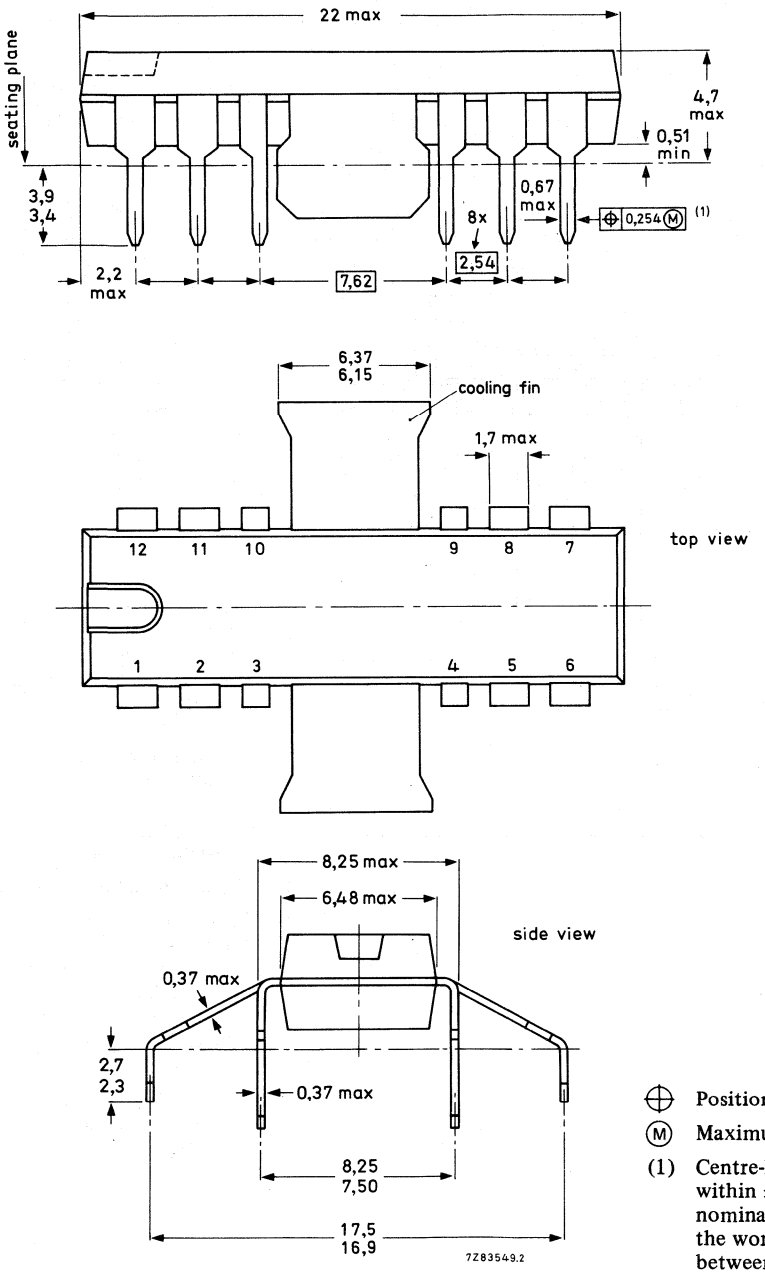
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT150)



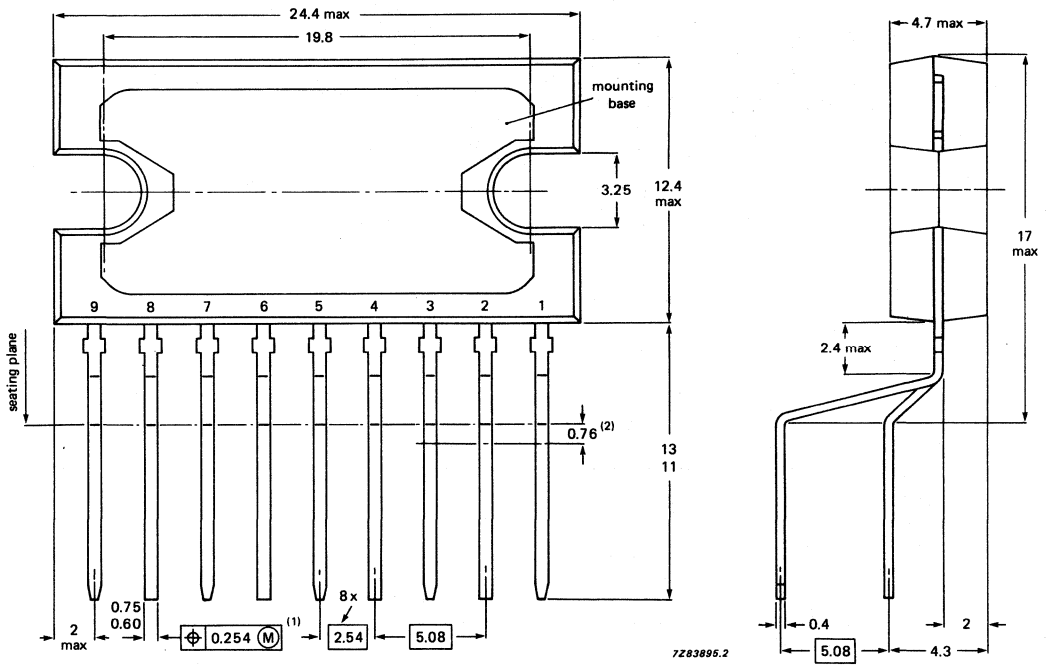
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT157)



⊕ Positional accuracy.

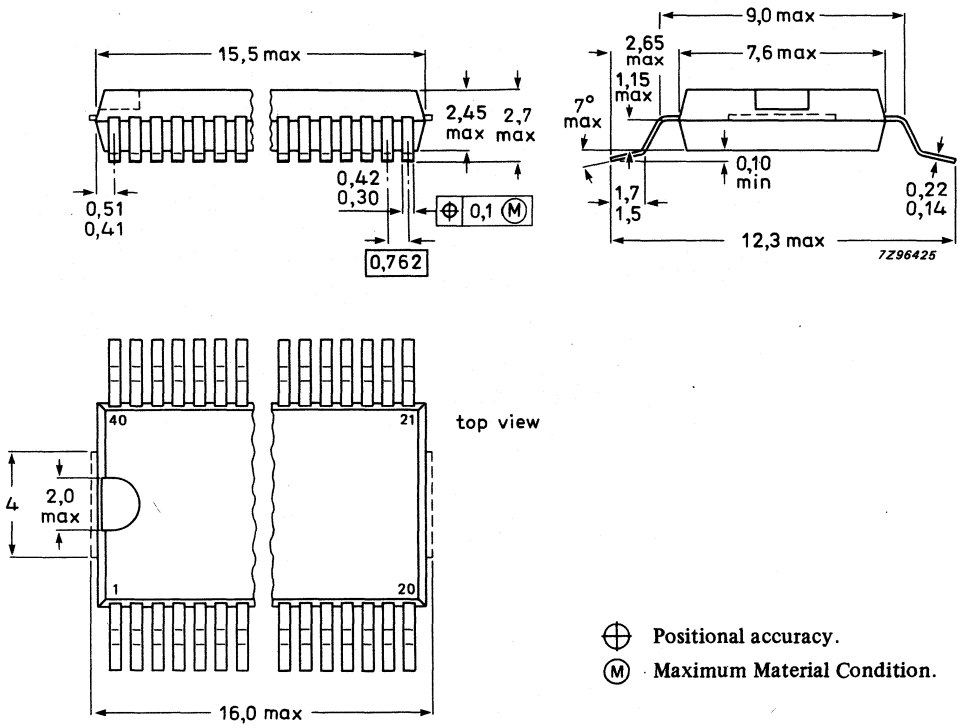
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

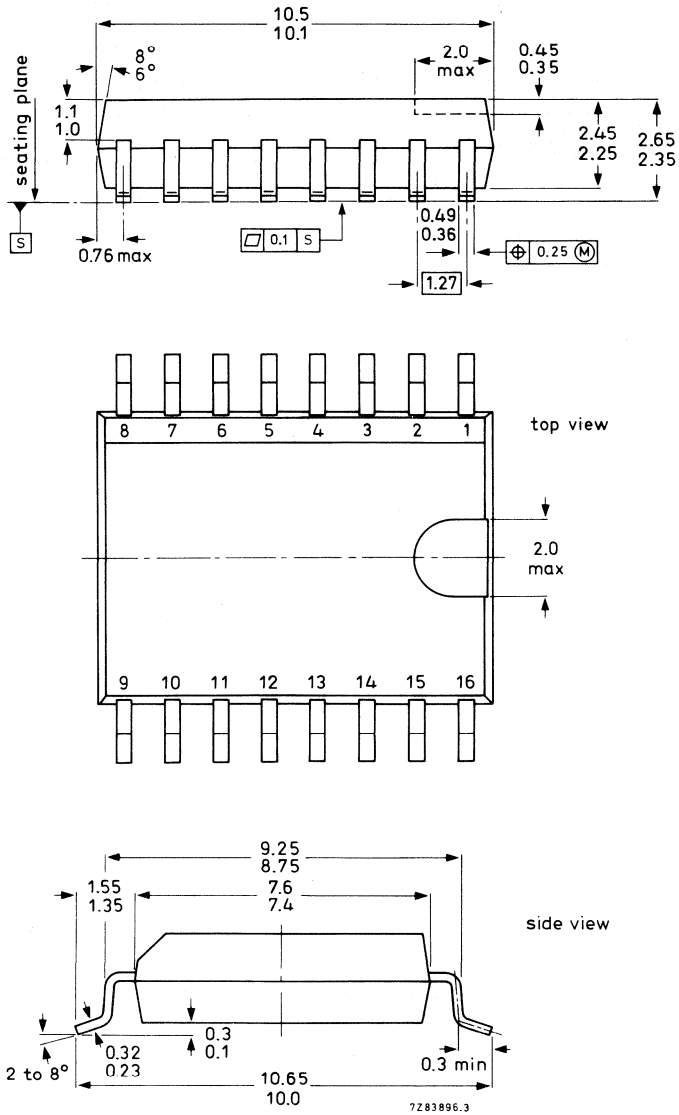
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

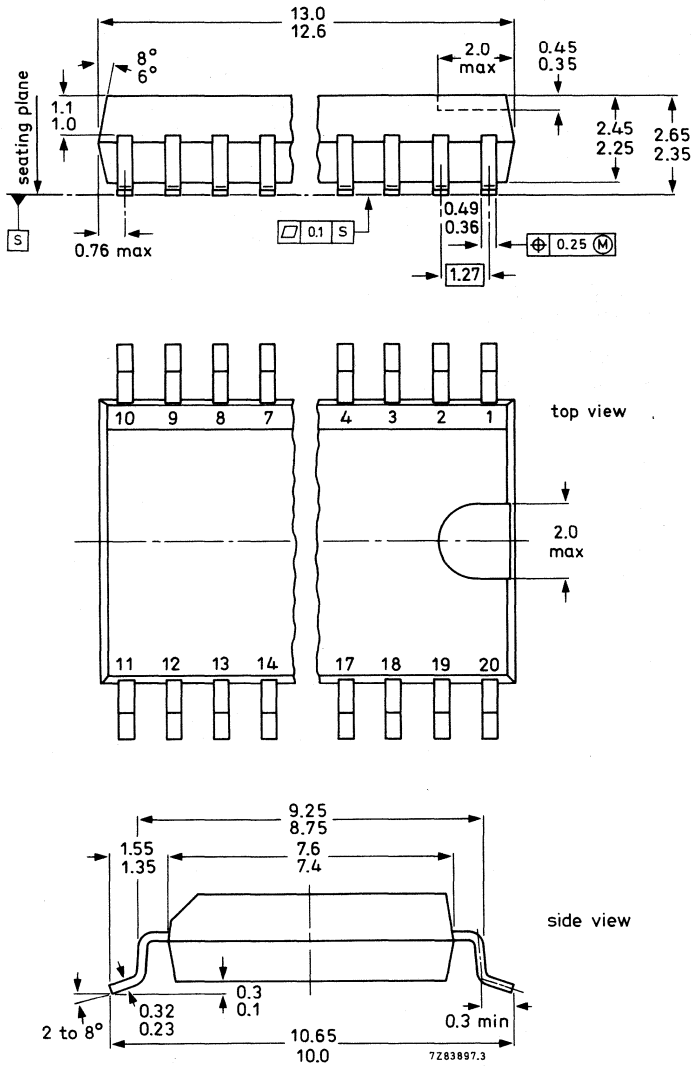


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

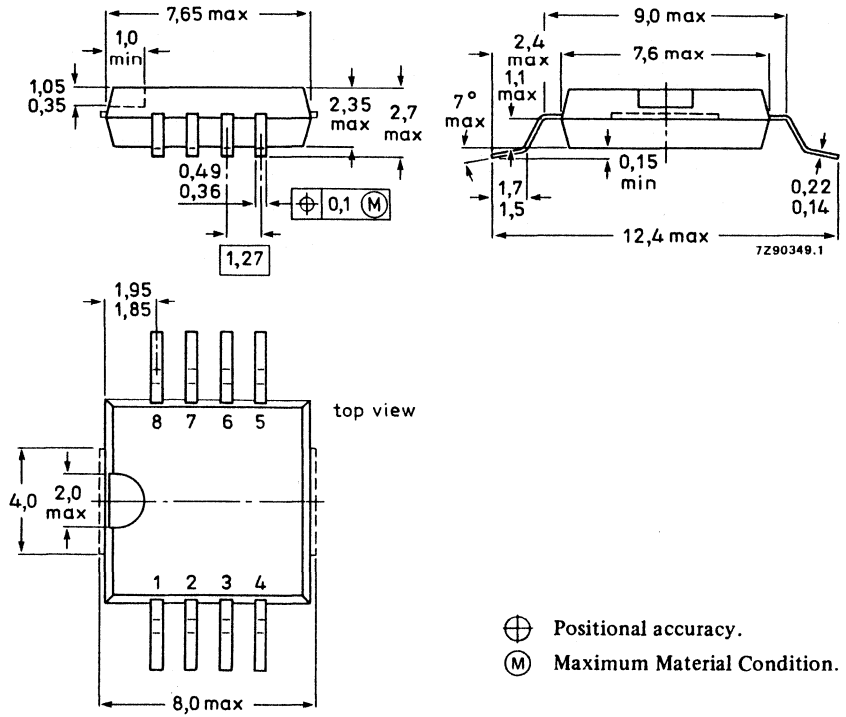


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

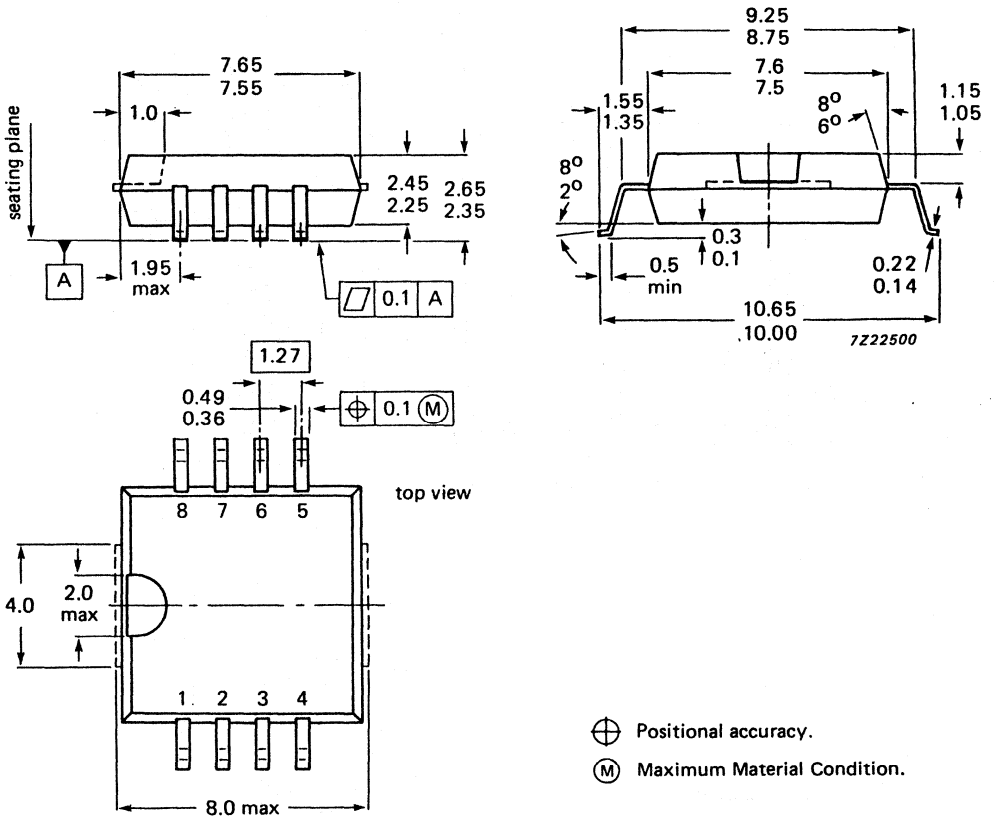
Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)



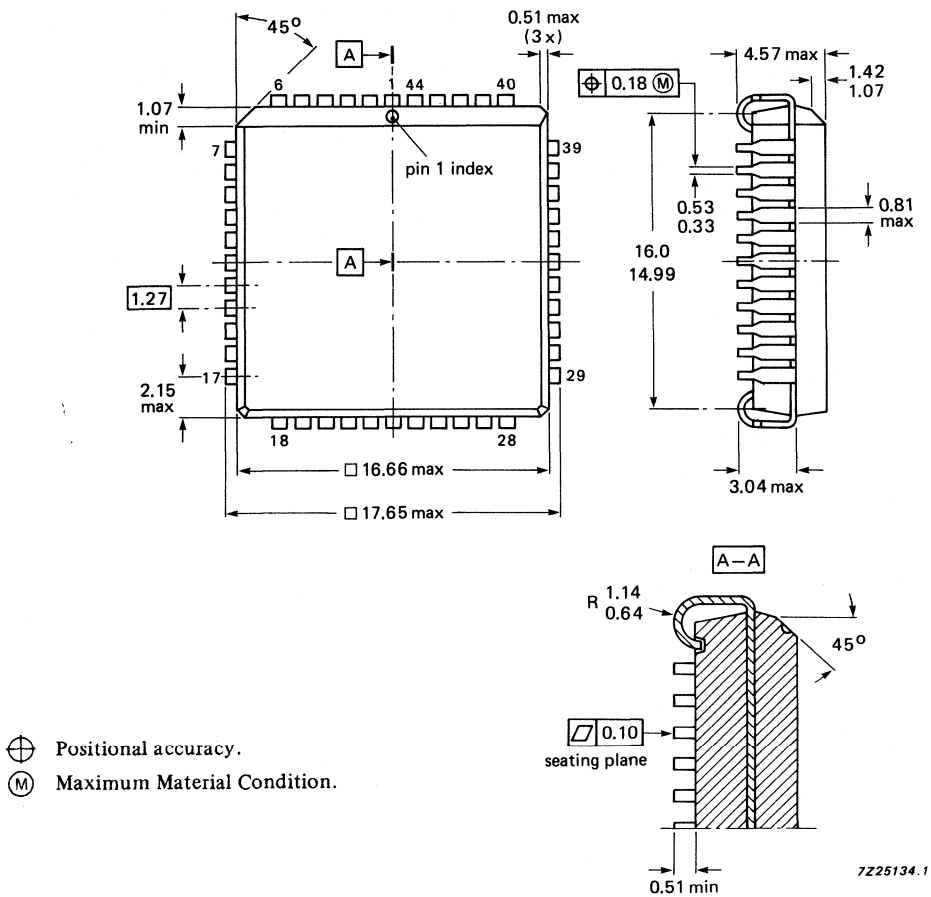
Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)



Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT187AGA, CG)

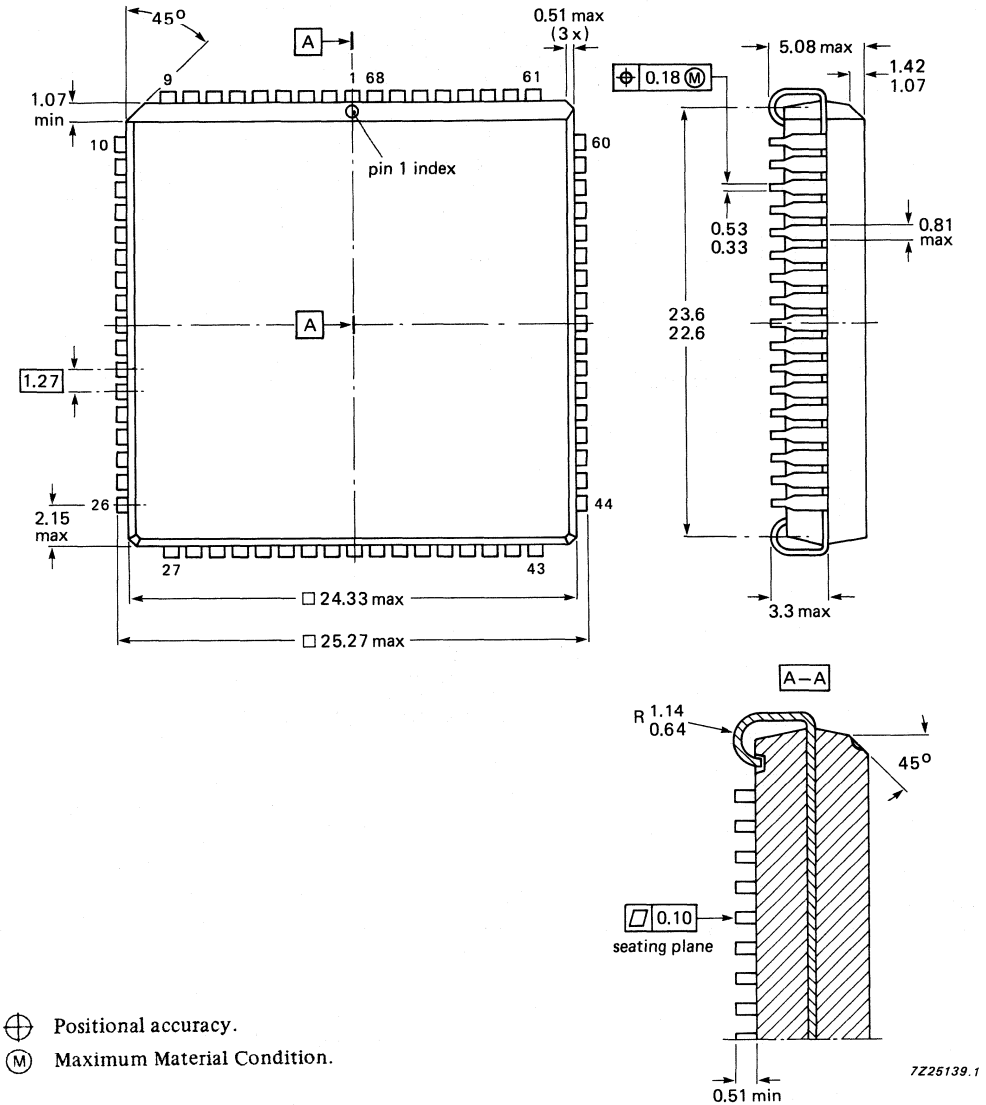


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT 188AGA, CG)

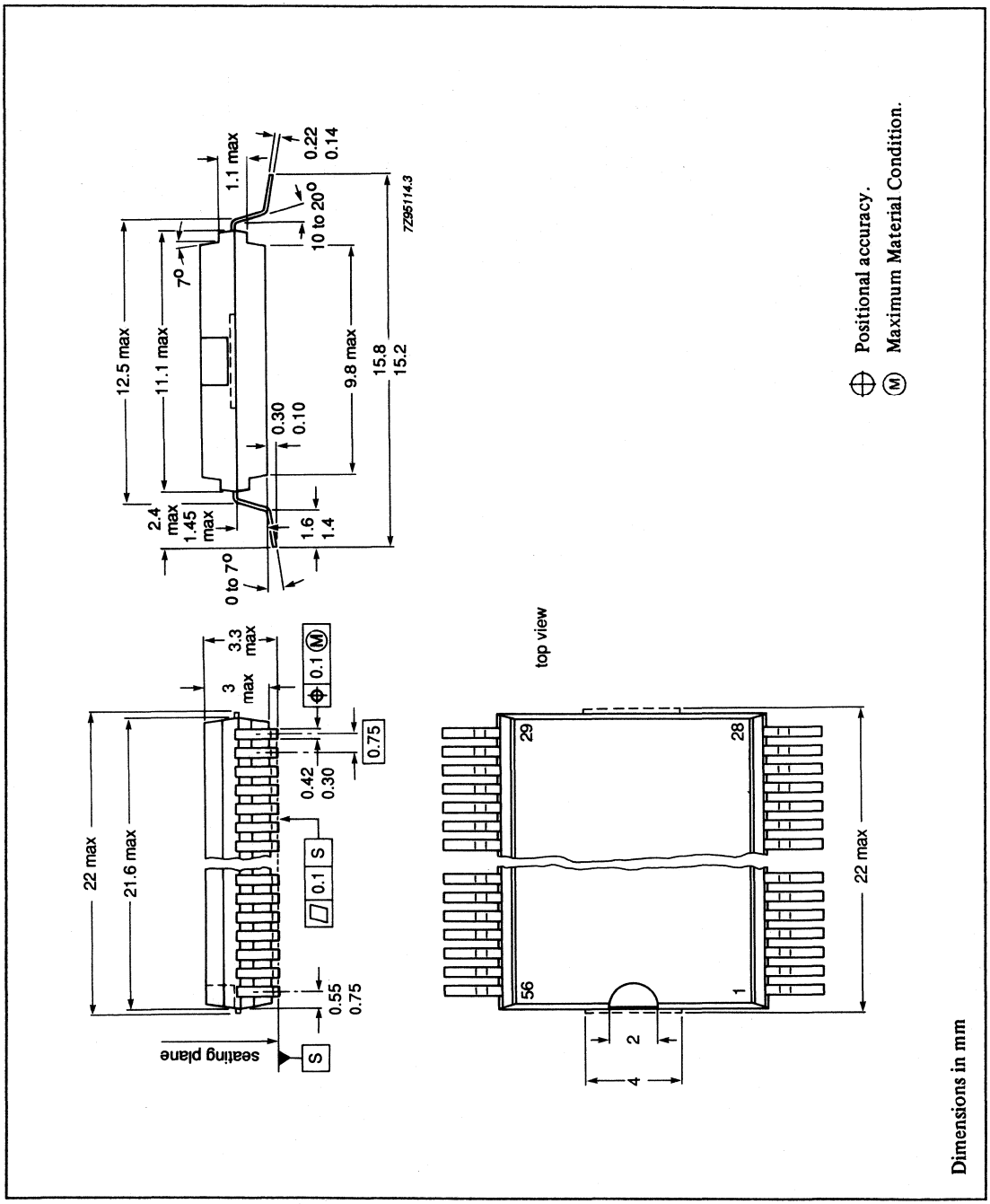


⊕ Positional accuracy.

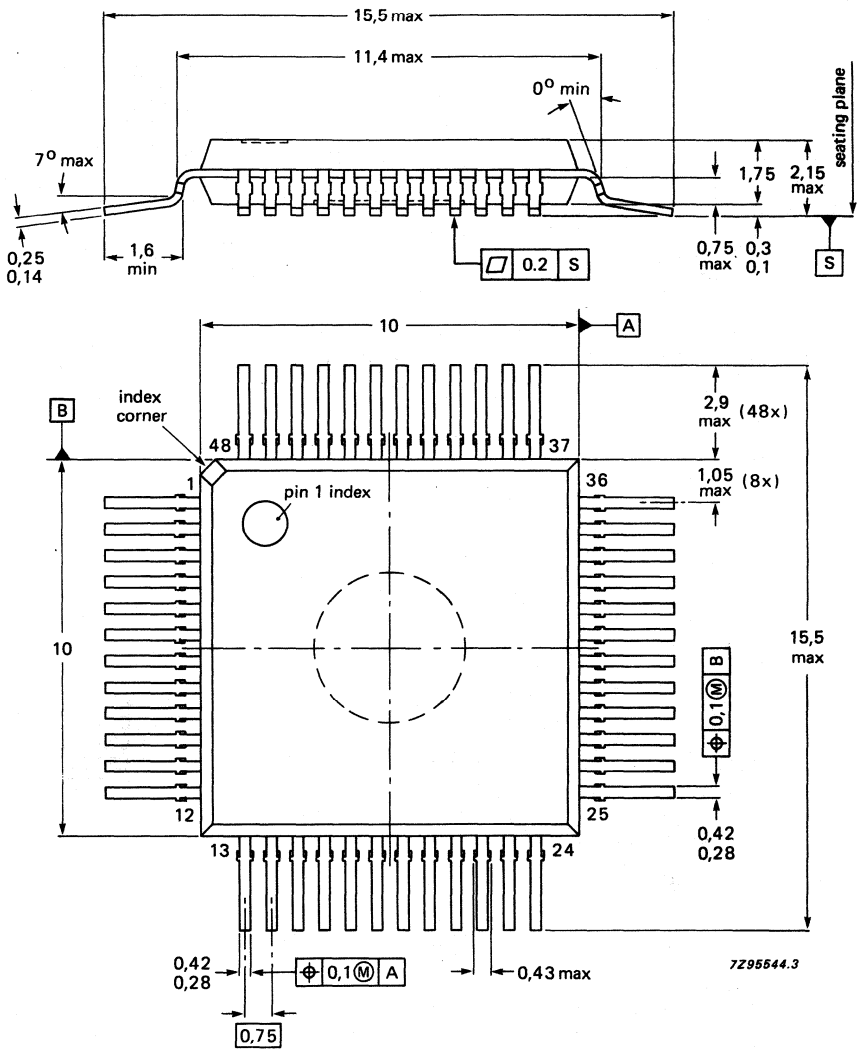
Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT 190)



48-LEAD QUAD FLAT-PACK; PLASTIC (SOT196AG)

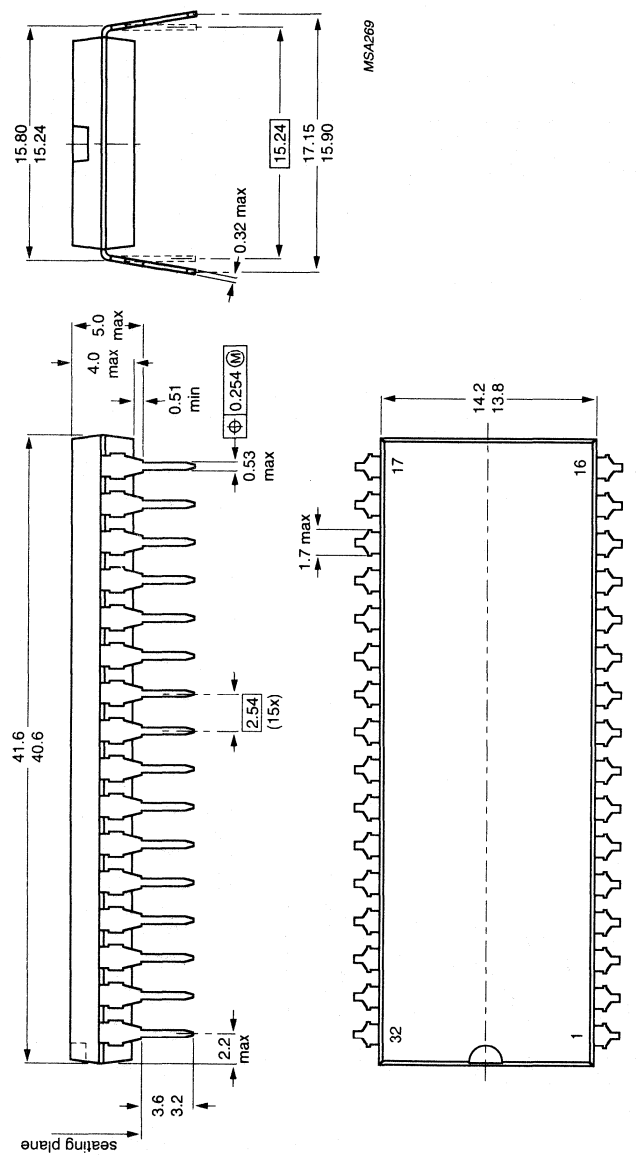


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

32-LEAD DUAL IN-LINE (SOT201)



⊕ Positional accuracy.

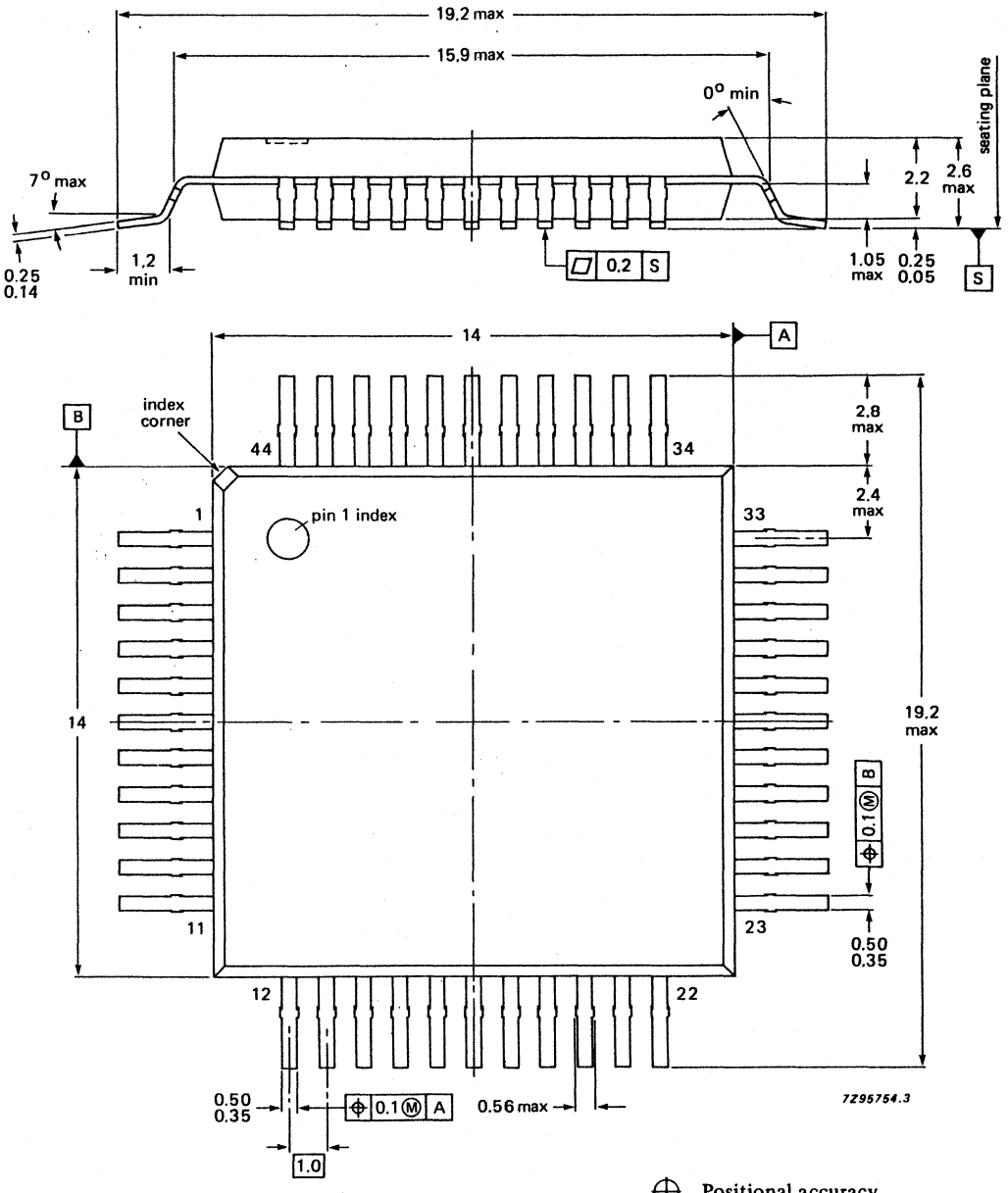
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205AG)

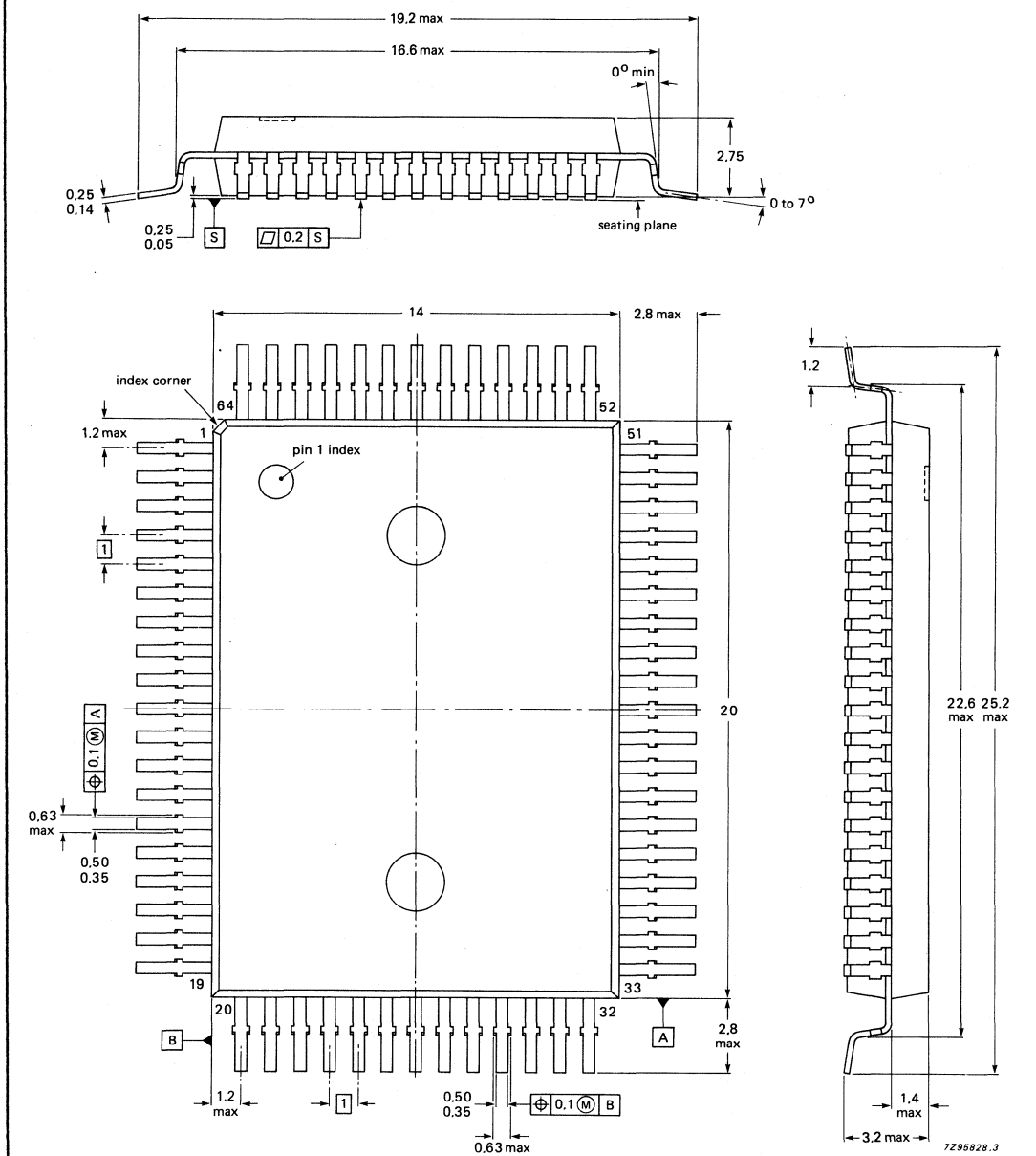


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

64-LEAD QUAD FLAT-PACK; PLASTIC (SOT208)

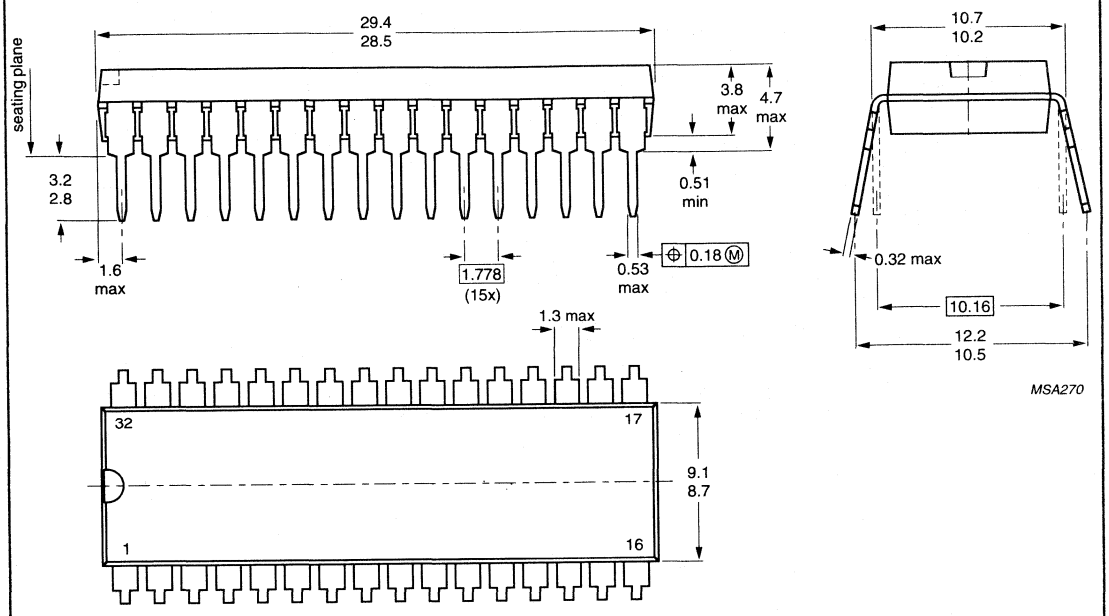


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

32-LEAD SHRINK DUAL IN-LINE; PLASTIC (SOT232)

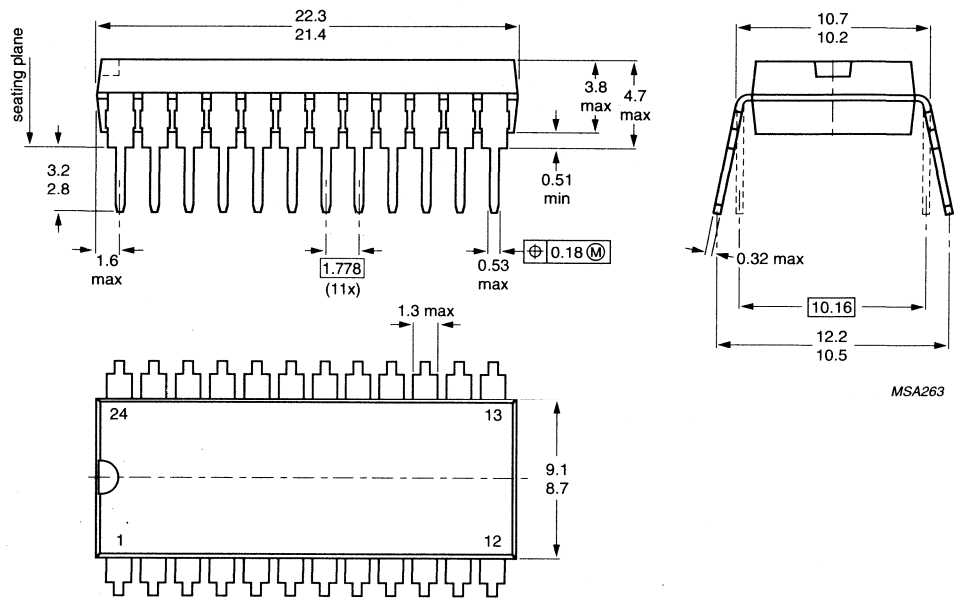


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

24-LEAD SHRINK DUAL IN-LINE; PLASTIC (SOT 234)

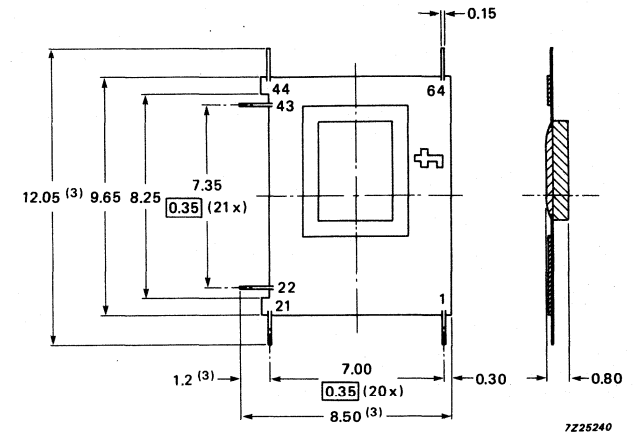


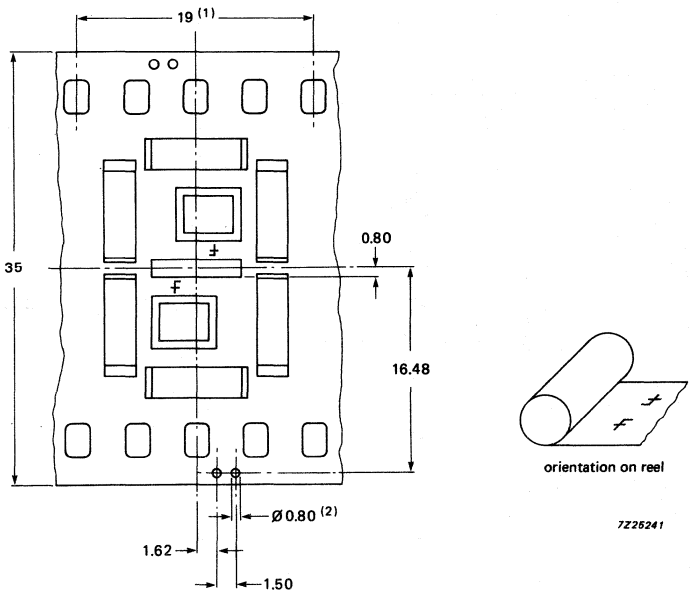
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT267A,C,D)

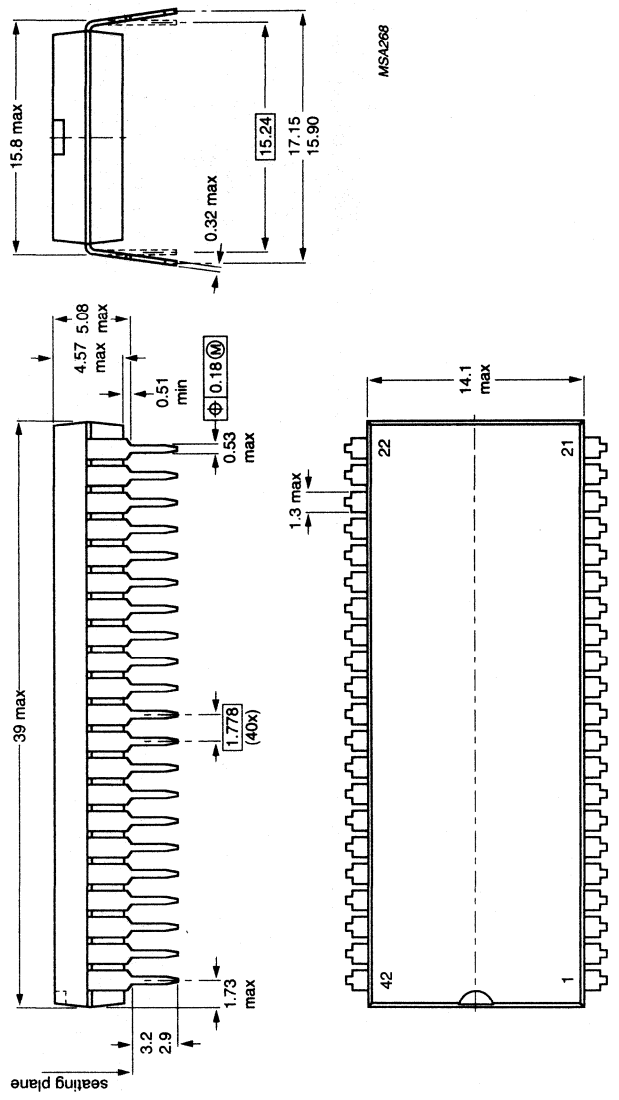




(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

Dimensions in mm

42-LEAD SHRINK DUAL IN-LINE; PLASTIC (SOT270)



SOLDERING

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING TAB MODULES

1. Fluxing

(a) a flux that does not have to be removed,
or
(b) a water-soluble flux.

2. Soldering

The reflow soldering method using a pulse-heated soldering tool is usually suitable. Limit the soldering operation to 3 seconds at 250 °C at the leads.

3. Cleaning

Avoid cleaning if possible.

If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

The contents of each series are listed on pages iii to ix.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where application is given it is advisory and does not form part of the product specification.

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* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

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This series of handbooks comprises:

code	handbook title
IC01a/b	**Radio, audio and associated systems**
IC02a/b	**Video and associated systems**
IC03	**ICs for Telecom;** Subscriber sets, Cordless Telephones, Mobile/Cellular, Radio Pagers
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; 74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
Supplement to IC07	**Advanced CMOS logic (ACL)**
IC08	**10/100K ECL Logic/Memory/PLD**
IC09	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
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current code	new code	handbook title
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S2b	**SC03**	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08a**	**RF power bipolar transistors**
	SC08b	**RF power MOS transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8b	**SC12**	**Optocouplers**
S9	**SC13**	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S13	**SC17**	**Semiconductor sensors**

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code	handbook title
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DC02	**Monochrome monitor tubes and deflection units**
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DC04	**Loudspeakers**
DC05	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

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current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02**	**Varistors, thermistors and sensors**
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C7	**PA04**	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06**	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**
	PA11	**Quartz Oscillators**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T3	**PC01**	**High-power klystrons and accessories**
T5	**PC02***	**Cathode-ray tubes**
T6	**PC03***	**Geiger-Müller tubes**
T9	**PC04**	**Photo multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09**	**Dry-reed switches**
	PC11	**Solid state image sensors and peripherals integrated circuits**
T9	**PC12***	**Electron multipliers**

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MAGNETIC PRODUCTS

This series of data handbooks comprises:

current code	new code	handbook title
C4 **C5**	**MA01**	**Soft Ferrites**
C16	**MA02**	**Permanent magnet materials**
C19	**MA03***	**Piezoelectric ceramics**

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